LH53259

CMOS 256K (32K × 8) Mask-Programmable ROM

FEATURES

- 32,768 × 8 bit organization
- Access time: 150 ns (MAX.)
- Low-power consumption:
  Operating: 110 mW (MAX.)
  Standby: 82.5 μW (MAX.)
- Programmable output enable
- Static operation (Internal sync. system)
- TTL compatible I/O
- Three-state outputs
- Single +5 V power supply
- Packages:
  28-pin, 600-mil DIP
  28-pin, 450-mil SOP
  44-pin, 10 × 10 mm^2 QFP
- JEDEC standard EPROM pinout (DIP)

DESCRIPTION

The LH53259 is a mask-programmable ROM organized as 32,768 × 8 bits. It is fabricated using silicon-gate CMOS process technology.

PIN CONNECTIONS

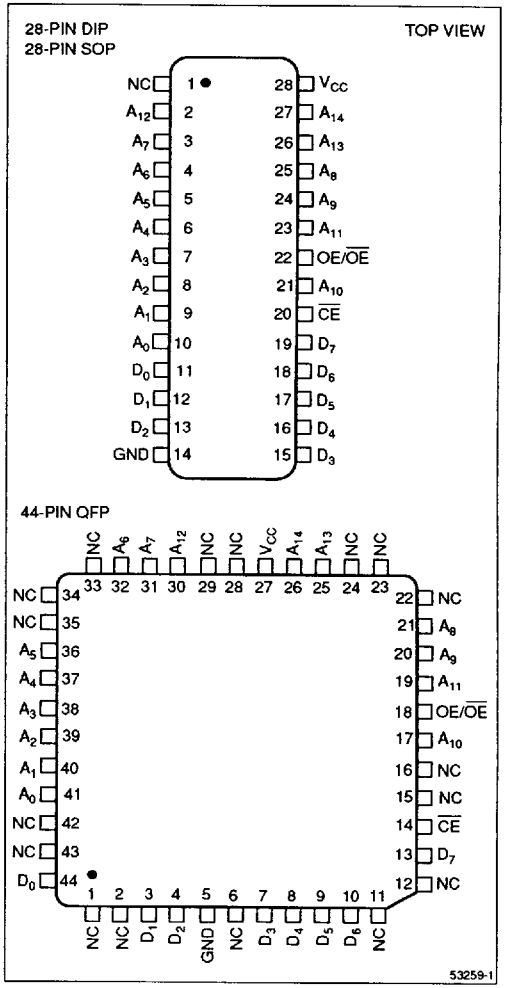


Figure 1. Pin Connections for DIP, SOP, and QFP Packages

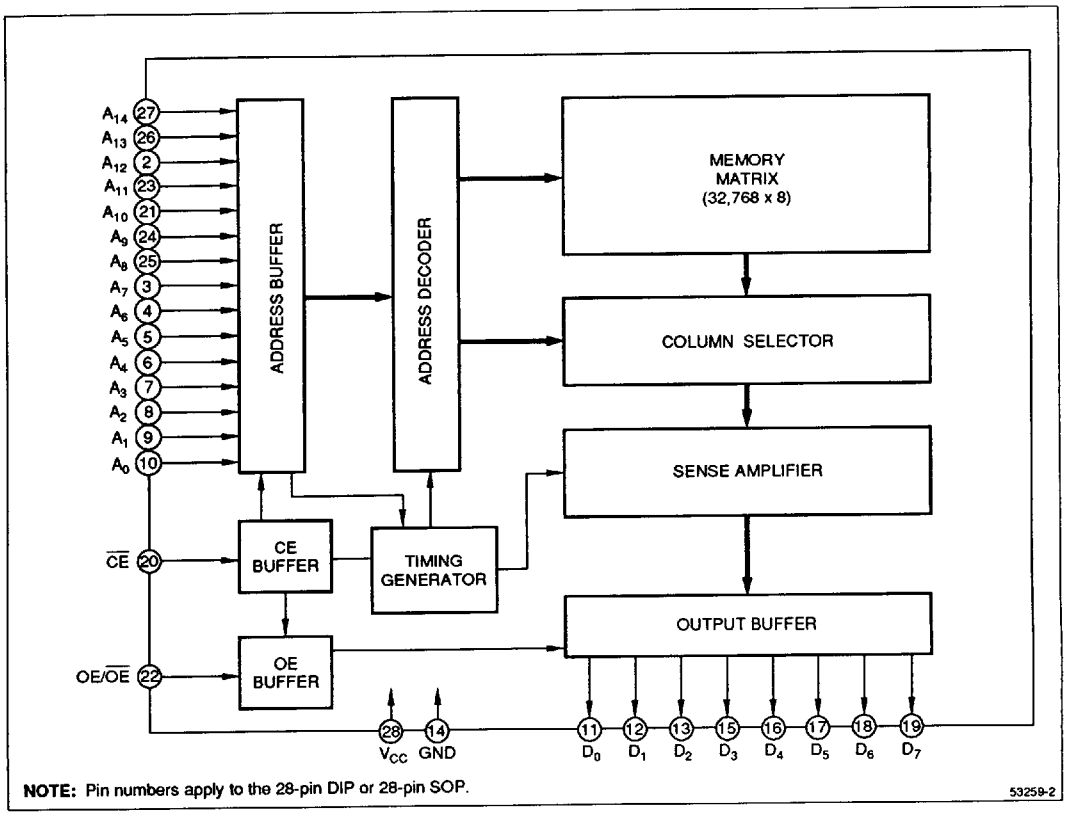


Figure 2. LH53259 Block Diagram

PIN DESCRIPTION

SIGNAL	PIN NAME	NOTE
A_0 - A_{14}	Address input	
D_0 - D_7	Data output	
$\overline{CE}$	Chip enable input	
OE/$\overline{OE}$	Output enable input	1

SIGNAL	PIN NAME	NOTE
V_{CC}	Power supply (+5 V)	
GND	Ground	
NC	Non connection	

NOTE:
1. The active level of OE/$\overline{OE}$ is mask-programmable.

TRUTH TABLE

$\overline{CE}$	OE/$\overline{OE}$	MODE	D_0 - D_7	SUPPLY CURRENT	NOTE
H	X	Non selected	High-Z	Standby	1
L	L/H			Operating	
	H/L	Selected	D_{OUT}		

NOTE:
1. X = H or L

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING	UNIT	NOTE
Supply voltage	V_{CC}	-0.3 to +7.0	V	1
Input voltage	V_{IN}	-0.3 to V_{CC} +0.3	V	
Output voltage	V_{OUT}	-0.3 to V_{CC} +0.3	V	
Operating temperature	Topr	0 to +70	°C	
Storage temperature	Tstg	-55 to +150	°C	

NOTE:
1. The maximum applicable voltage on any pin with respect to GND.

RECOMMENDED OPERATING CONDITIONS (T_A = 0 to +70°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply voltage	V_{CC}	4.5	5.0	5.5	V

DC CHARACTERISTICS (V_{CC} = 5 V ± 10%, T_A = 0 to +70°C)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT	NOTE
Input 'Low' voltage	V_{IL}		-0.3		0.8	V	
Input 'High' voltage	V_{IH}		2.2		V_{CC} +0.3	V	
Output 'Low' voltage	V_{OL}	I_{OL} = 1.6 mA			0.4	V	
Output 'High' voltage	V_{OH}	I_{OH} = -400 µA	2.4			V	
Input leakage current	$\|I_{LI}\|$	V_{IN} = 0 V to V_{CC}			10	µA	
Output leakage current	$\|I_{LO}\|$	V_{OUT} = 0 V to V_{CC}			10	µA	1
Operating current	I_{CC1}	t_{RC} = 150 ns			20	mA	2
	I_{CC2}	t_{RC} = 1 µs			15		
	I_{CC3}	t_{RC} = 150 ns			15	mA	3
	I_{CC4}	t_{RC} = 1 µs			10		
Standby current	I_{SB1}	$\overline{CE}$ = V_{IH}			2	mA	
	I_{SB2}	$\overline{CE}$ = V_{CC} - 0.2 V			15	µA	

NOTES:
1. $\overline{CE}/\overline{OE}$ = V_{IH} or OE = VIL
2. V_{IN} = V_{IH}/V_{IL}, $\overline{CE}$ = V_{IL}, outputs open
3. V_{IN} = (V_{CC} - 0.2 V) or 0.2 V, $\overline{CE}$ = 0.2 V, outputs open

AC CHARACTERISTICS (V_{CC} = 5 V ± 10%, T_A = 0 to +70°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	NOTE
Read cycle time	t_{RC}	150			ns	
Address access time	t_{AA}			150	ns	
Chip enable access time	t_{ACE}			150	ns	
Output enable time	t_{OE}	10		80	ns	
Output hold time	t_{OH}	5			ns	
$\overline{CE}$ to output in High-Z	t_{CHZ}			70	ns	1
OE to output in High-Z	t_{OHZ}			70	ns	

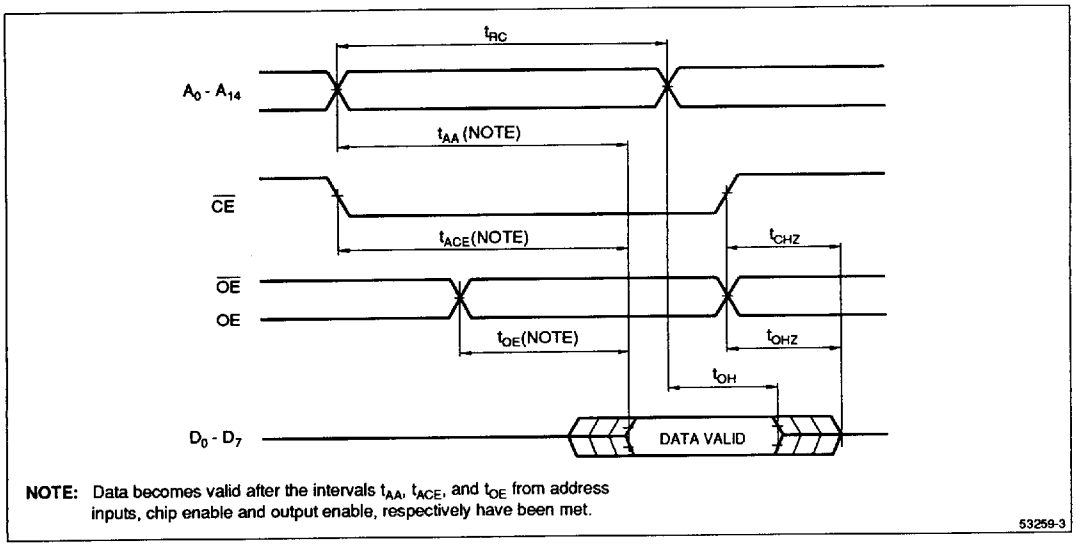
NOTE:
1. This is the time required for the output to become high impedance.

AC TEST CONDITIONS

PARAMETER	RATING
Input voltage amplitude	0.6 V to 2.4 V
Input rise/fall time	10 ns
Input reference level	1.5 V
Output reference level	0.8 V and 2.2 V
Output load condition	1TTL +100 pF

CAPACITANCE (V_{CC} = 5 V ± 10%, f = 1 MHz, T_A = 25°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Input capacitance	C_{IN}			10	pF
Output capacitance	C_{OUT}			10	pF



NOTE: Data becomes valid after the intervals t_{AA}, t_{ACE}, and t_{OE} from address inputs, chip enable and output enable, respectively have been met.

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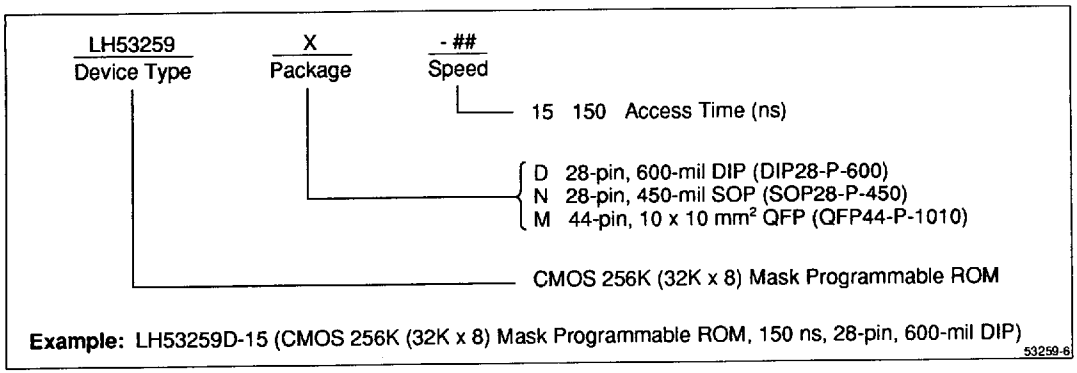
Figure 3. Timing Diagram

ORDERING INFORMATION



Example: LH53259D-15 (CMOS 256K (32K x 8) Mask Programmable ROM, 150 ns, 28-pin, 600-mil DIP)

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