SMC82C55AC-5

CMOS PROGRAMMABLE PERIPHERAL INTERFACE

- **24 Bit Input/Output**
- **Improved DC Driving Capability**
- **Low Power**

■DESCRIPTION

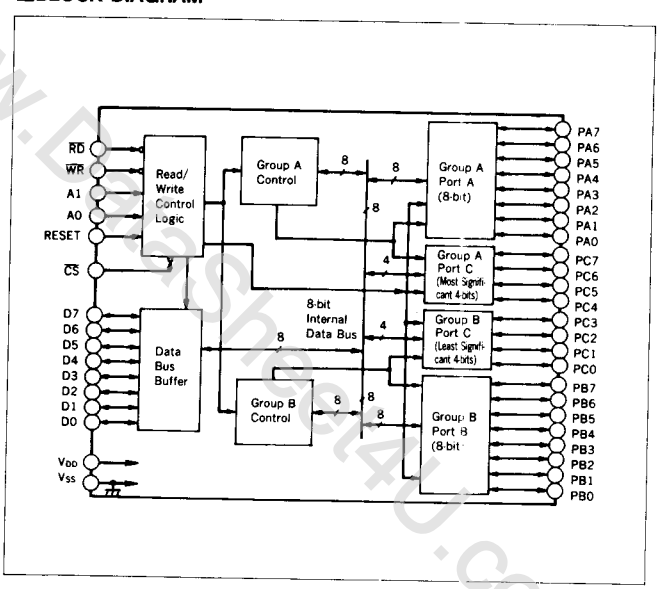
The SMC82C55AC-5 is a CMOS General Purpose Programmable I/O device designed for use with an 8/16 bit CPU. The device has 24 programmable I/O pins that can be individually programmed in two groups of 12.

■FEATURES

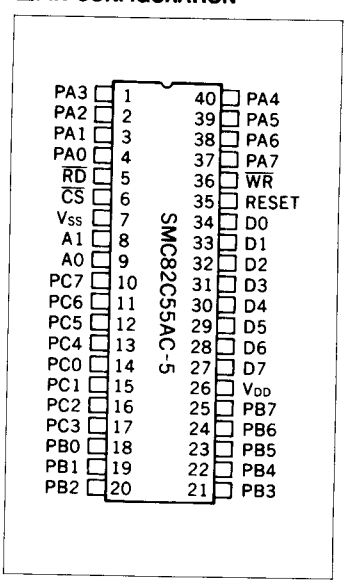
- 24 programmable I/O pins
- Compatible with 80XX series of microprocessors
- Direct bit set/reset capability
- Improved DC driving capability
- Single 5V (±10%) power supply
- TTL compatible
- Package·····40-pin DIP
  40-pin SOP*

*Under development

■BLOCK DIAGRAM



■PIN CONFIGURATION



■ABSOLUTE MAXIMUM RATINGS

(V_{SS}=0V, Ta=25°C)

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage	V_{DD}	With respect to V_{SS}	−0.3 to 7	V
Input voltage	V_I		−0.3 to V_{DD}+0.3	V
Output voltage	V_O		−0.3 to V_{DD}+0.3	V
Operating temperature	T_{opr}	—	−20 to 75	°C
Storage temperature	T_{stg}	—	−65 to 150	°C
Soldering temperature and time	T_{sol}	—	260°C, 10s (lead)	—

■RECOMMENDED OPERATING CONDITIONS

(Ta=−20 to 75°C, unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Supply voltage	V_{DD}	—	4.5	5	5.5	V
Supply voltage	V_{SS}	—	—	0	—	V

■ELECTRICAL CHARACTERISTICS

●DC Electrical Characteristics

(Ta=−20 to 75°C, V_{DD}=5V±10%, V_{SS}=0V, unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
High-level input voltage	V_{IH}	—	2.0	—	V_{DD}+0.3	V
Low-level input voltage	V_{IL}	—	−0.3	—	0.8	V
Output high voltage*2	V_{OH}	I_{OH}=−400μA	2.4	—	—	V
Output low voltage	V_{OL}	I_{OL}=2.5mA	—	—	0.45	V
Supply current from V_{DD}	I_{DD}	V_{SS}=0V. All input mode. RESET=0V. Other pins=V_{DD}	—	—	10	μA
Input leak current	I_{LI}	V_{SS}=0V, V_I=0V, V_{DD}	—	—	±10	μA
Off-state output current	I_{OZ}	V_{SS}=0V, V_I=0V, V_{DD}	—	—	±10	μA
Input capacitance	C_I	V_{IL}=V_{SS}, f=1MHz, 25mVrms Ta=25°C	—	—	10	pF
Input/output terminal capacitance	$C_{I/O}$	$V_{I/OL}$=V_{SS}, f=1MHz, 25mVrms, Ta=25°C	—	—	20	pF

*1 Current flowing into an IC is positive, out is negative.
*2 The sum total I_{OH} current must be less than −64mA on port B, C, and −32mA on Port A.

●AC Electrical Characteristics

○ Timing Requirements

(Ta=−20 to 75°C, V_{DD}=5V±10%, V_{SS}=0V, unless otherwise noted)

Parameter	Symbol	Alternative symbol	Conditions	Min	Typ	Max	Unit
Read pulse width	$t_{W(R)}$	t_{RR}		200	—	—	ns
Peripheral setup time before read	$t_{SU(PE-R)}$	t_{IR}		0	—	—	ns
Peripheral hold time after read	$t_{h(R-PE)}$	t_{HR}		0	—	—	ns
Address setup time before read	$t_{SU(A-R)}$	t_{AR}		0	—	—	ns
Address hold time after read	$t_{h(R-A)}$	t_{RA}		0	—	—	ns
Write pulse width	$t_{w(w)}$	t_{WW}		200	—	—	ns
Data setup time before write	$t_{SU(DQ-W)}$	t_{DW}		100	—	—	ns
Data hold time after write	$t_{h(W-DQ)}$	t_{WD}		0	—	—	ns
Address setup time before write	$t_{SU(A-W)}$	t_{AW}		0	—	—	ns
Address hold time after write	$t_{h(W-A)}$	t_{WA}		0	—	—	ns
Acknowledge pulse width	$t_{W(ACK)}$	t_{AK}		300	—	—	ns
Strobe pulse width	$t_{W(STB)}$	t_{ST}		350	—	—	ns
Peripheral setup time before strobe	$t_{SU(PE-STB)}$	t_{PS}		0	—	—	ns
Peripheral hold time after strobe	$t_{h(STB-PE)}$	t_{PH}		150	—	—	ns
Read/write cycle time	$t_{C(RW)}$	t_{RV}		850	—	—	ns

●Switching Characteristics

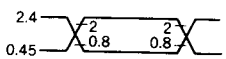
(Ta = −20 to 75°C, V_{DD} = 5V ± 10%, unless otherwise noted)

Parameter	Symbol	Alternative symbol	Conditions	Min	Typ	Max	Unit
Propagation time from read to data output	$t_{PZX(R-DQ)}$	t_{RD}	C_L = 150pF			170	ns
Propagation time from read to data floating *3	$t_{PXZ(R-DQ)}$	t_{DF}		10		100	ns
Propagation time from write to output	$t_{PHL(W-PE)}$ $t_{PLH(W-PE)}$	t_{WB}				350	ns
Propagation time from strobe to IBF flag	$t_{PLH(STB-IBF)}$	t_{SIB}				300	ns
Propagation time from strobe to interrupt	$t_{PLH(STB-INTR)}$	t_{SIT}				300	ns
Propagation time from read to interrupt	$t_{PHL(R-INTR)}$	t_{RIT}				400	ns
Propagation time from read to IBF flag	$t_{PHL(R-IBF)}$	t_{RIB}				300	ns
Propagation time from write to interrupt	$t_{PHL(W-INTR)}$	t_{WIT}				450	ns
Propagation time from write to $\overline{OBF}$ flag	$t_{PHL(W-OBF)}$	t_{WOB}				650	ns
Propagation time from acknowledge to $\overline{OBF}$ flag	$t_{PLH(ACK-OBF)}$	t_{AOB}				350	ns
Propagation time from acknowledge to interrupt	$t_{PLH(ACK-INTR)}$	t_{AIT}				350	ns
Propagation time from acknowledge to data output	$t_{PZX(ACK-PE)}$	t_{AD}				300	ns
Propagation time from acknowledge to data floating *3	$t_{PXZ(ACK-PE)}$	t_{KD}		20		250	ns

*3 Test conditions are not applied.

*4 A.C Testing waveform

Input pulse level	0.45 to 2.4V
Input pulse rise time	10ns
Input pulse fall time	10ns
Reference level input	V_{IH} = 2V, V_{IL} = 0.8V
Output	V_{OH} = 2V, V_{OL} = 0.8V



■FUNCTIONS

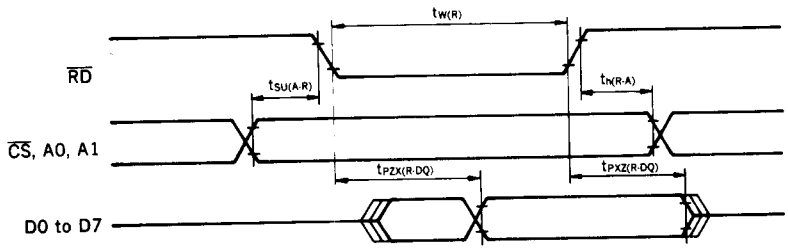
The SMC82C55AC-5 has programmable I/O pins that interface peripheral equipment to the CPU. The system software programs the functional configuration of the device.

The 24 programmable I/O pins may be individually configured in two groups of 12. Each group has three major modes of operation : 0, 1 and 2. In mode 0, each group of 12 I/O pins may be programmed in sets of four inputs or outputs. In mode 1, each group of 12 I/O pins may be grouped as one 8-bit I/O data port and one 4-bit control/status port. Mode 2 is used in Group A only, as one 8-bit bidirectional port and one 5-bit control /status port.

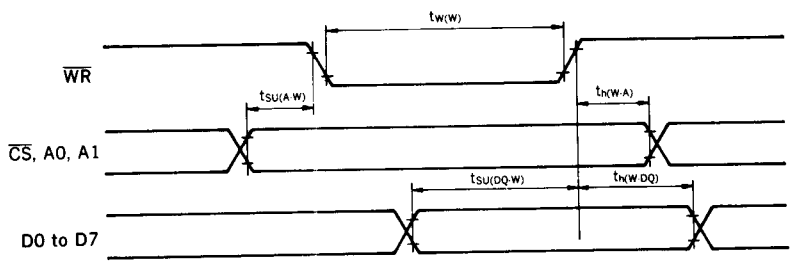
In mode 1 or 2, the control/status port bits can be set or reset by the CPU. A RESET pin is provided to clear all internal registers and set all ports to an input mode.

●Timing Chart

○Data bus read operation

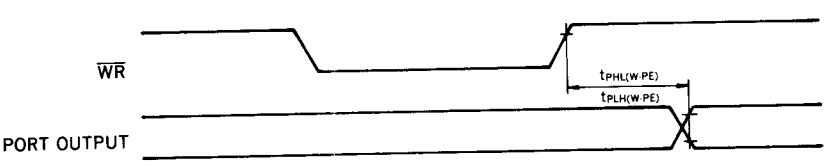


○Data bus write operation

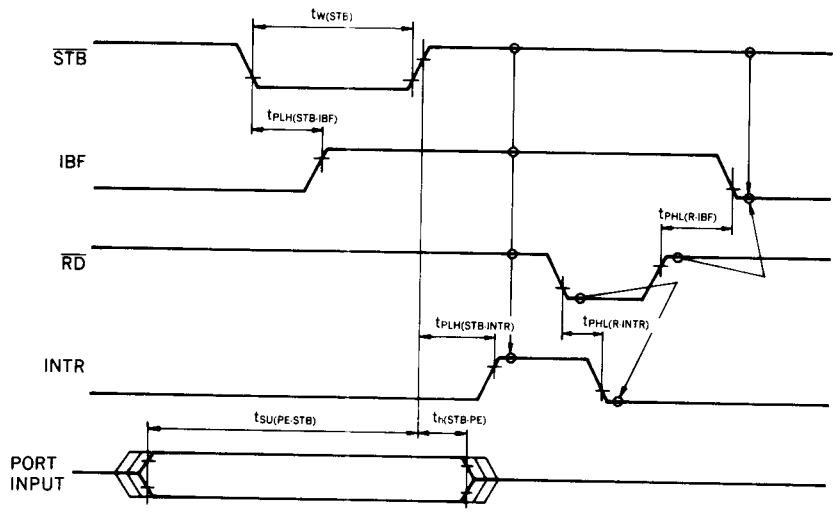


○Mode 0 Port input

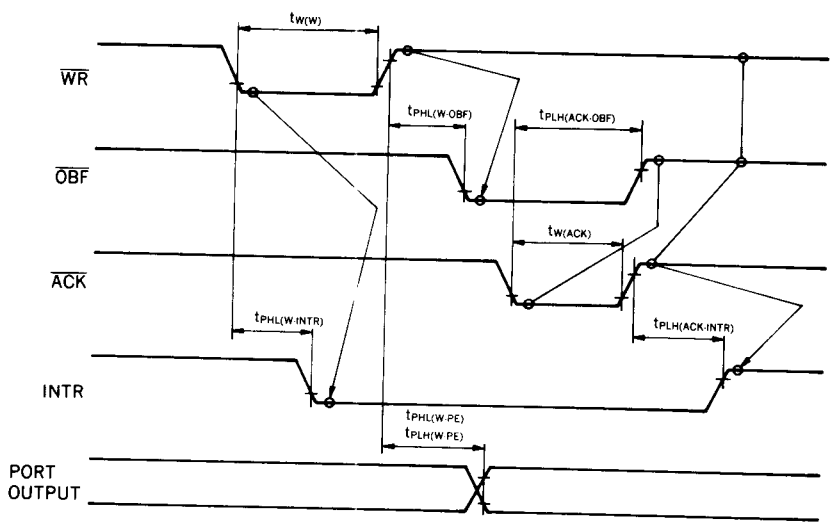
○Mode 0, 1 Port output



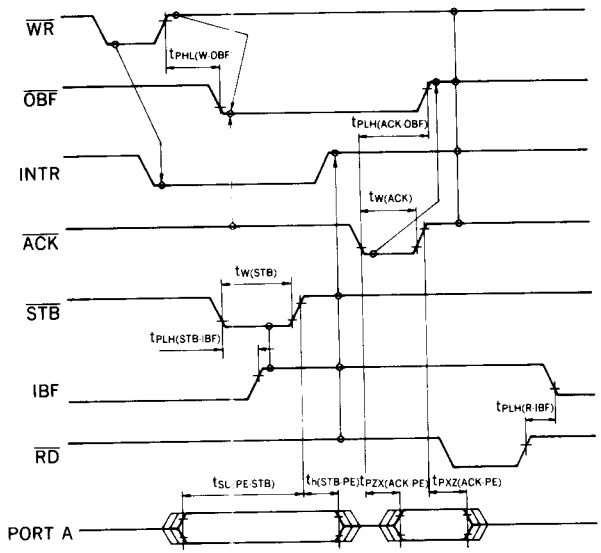
○ Mode 1 Strobed input



○ Mode 1 Strobed output



○Mode 2 Bidirectional



*5 $INTR = IBF \cdot \overline{MASK} \cdot \overline{STB} \cdot \overline{RD} + \overline{OBF} \cdot \overline{MASK} \cdot \overline{ACK} \cdot \overline{WR}$

■APPLICATION

The SMC 82C55AC-5 is used as a general purpose programmable I/O device designed to interface peripheral equipment to the 80XX series of microprocessors.

■PACKAGE DIMENSIONS