

# SN74LS299

## 8-Bit Shift/Storage Register with 3-State Outputs

The SN74LS299 is an 8-Bit Universal Shift/Storage Register with 3-state outputs. Four modes of operation are possible: hold (store), shift left, shift right and load data.

The parallel load inputs and flip-flop outputs are multiplexed to reduce the total number of package pins. Separate outputs are provided for flip-flops Q<sub>0</sub> and Q<sub>7</sub> to allow easy cascading. A separate active LOW Master Reset is used to reset the register.

- Common I/O for Reduced Pin Count
- Four Operation Modes: Shift Left, Shift Right, Load and Store
- Separate Shift Right Serial Input and Shift Left Serial Input for Easy Cascading
- 3-State Outputs for Bus Oriented Applications
- Input Clamp Diodes Limit High-Speed Termination Effects
- ESD > 3500 Volts

### GUARANTEED OPERATING RANGES

Symbol	Parameter	Min	Typ	Max	Unit
V <sub>CC</sub>	Supply Voltage	4.75	5.0	5.25	V
T <sub>A</sub>	Operating Ambient Temperature Range	0	25	70	°C
I <sub>OH</sub>	Output Current – High Q <sub>0</sub> , Q <sub>7</sub>			-0.4	mA
I <sub>OL</sub>	Output Current – Low Q <sub>0</sub> , Q <sub>7</sub>			8.0	mA
I <sub>OH</sub>	Output Current – High I/O <sub>0</sub> – I/O <sub>7</sub>			-2.6	mA
I <sub>OL</sub>	Output Current – Low I/O <sub>0</sub> – I/O <sub>7</sub>			24	mA

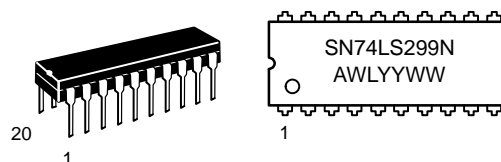


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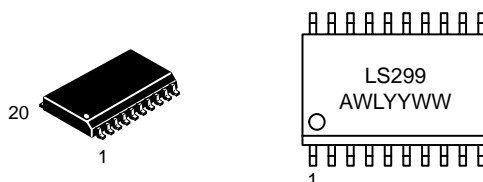
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**LOW  
POWER  
SCHOTTKY**

### MARKING DIAGRAMS



**PDIP-20  
N SUFFIX  
CASE 738**



**SOIC-20  
DW SUFFIX  
CASE 751D**

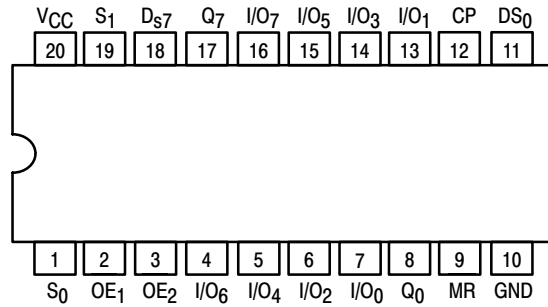
A = Assembly Location  
WL = Wafer Lot  
YY = Year  
WW = Work Week

### ORDERING INFORMATION

Device	Package	Shipping
SN74LS299N	PDIP-20	1440 Units/Box
SN74LS299DW	SOIC-WIDE	38 Units/Rail
SN74LS299DWR2	SOIC-WIDE	2500/Tape & Reel

# SN74LS299

CONNECTION DIAGRAM DIP (TOP VIEW)

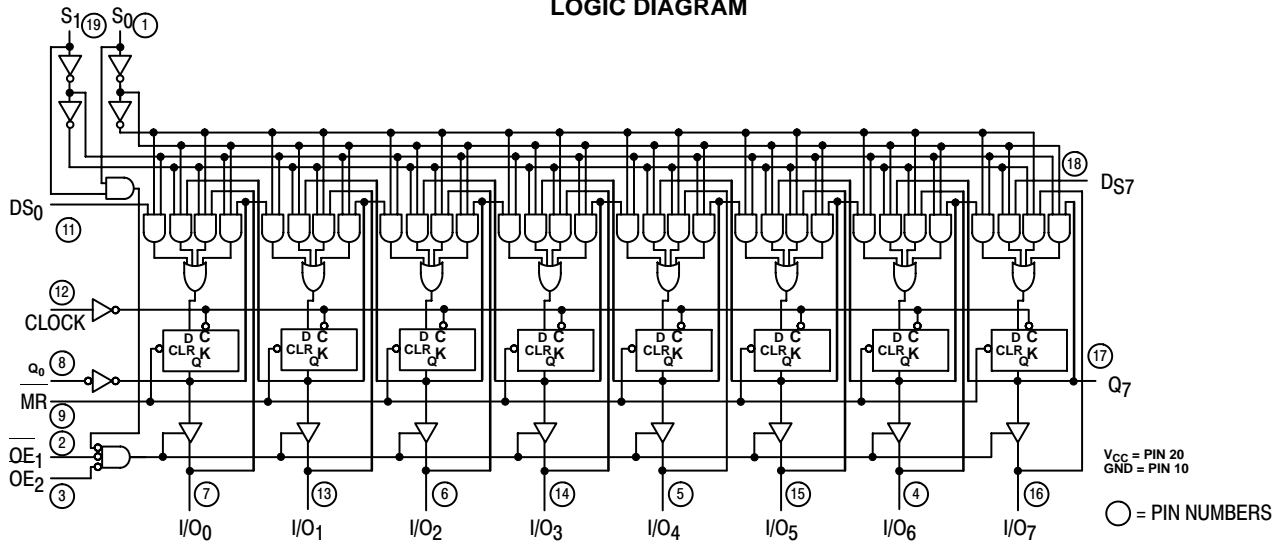


NOTE:  
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

PIN NAMES		LOADING (Note a)	
		HIGH	LOW
CP	Clock Pulse (Active Positive-Going Edge) Input	0.5 U.L.	0.25 U.L.
DS0	Serial Data Input for Right Shift	0.5 U.L.	0.25 U.L.
DS7	Serial Data Input for Left Shift	0.5 U.L.	0.25 U.L.
I/O <sub>n</sub>	Parallel Data Input or Parallel Output (3-State)	0.5 U.L.	0.25 U.L.
OE <sub>1</sub> , OE <sub>2</sub>	3-State Output Enable (Active LOW) Inputs	65 U.L.	15 U.L.
Q <sub>0</sub> , Q <sub>7</sub>	Serial Outputs	0.5 U.L.	0.25 U.L.
MR	Asynchronous Master Reset (Active LOW) Input	10 U.L.	5 U.L.
S <sub>0</sub> , S <sub>1</sub>	Mode Select Inputs	0.5 U.L.	0.25 U.L.
		1 U.L.	0.5 U.L.

NOTES:  
a) 1 TTL Unit Load (U.L.) = 40  $\mu$ A HIGH/1.6 mA LOW.

## LOGIC DIAGRAM



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## FUNCTION TABLE

INPUTS								RESPONSE
MR	S <sub>1</sub>	S <sub>0</sub>	OE <sub>1</sub>	OE <sub>2</sub>	CP	DS <sub>0</sub>	DS <sub>7</sub>	
L	X	X	H	X	X	X	X	Asynchronous Reset; Q <sub>0</sub> = Q <sub>7</sub> = LOW I/O Voltage Undetermined
L	X	X	X	H	X	X	X	
L	H	H	X	X	X	X	X	
L	L	X	L	L	X	X	X	Asynchronous Reset; Q <sub>0</sub> = Q <sub>7</sub> = LOW I/O Voltage LOW
L	X	L	L	L	X	X	X	
H	L	H	X	X	┐	D	X	Shift Right; D→Q <sub>0</sub> ; Q <sub>0</sub> →Q <sub>1</sub> ; etc. Shift Right; D→Q <sub>0</sub> & I/O <sub>0</sub> ; Q <sub>0</sub> →O <sub>1</sub> & I/O <sub>1</sub> ; etc.
H	L	H	L	L	┐	D	X	
H	H	L	X	X	┐	X	D	Shift Left; D→Q <sub>7</sub> ; Q <sub>7</sub> →Q <sub>6</sub> ; etc. Shift Left; D→Q <sub>7</sub> & I/O <sub>7</sub> ; Q <sub>7</sub> →Q <sub>6</sub> & I/O <sub>6</sub> ; etc.
H	H	L	L	L	┐	X	D	
H	H	H	X	X	┐	X	X	Parallel Load; I/O <sub>n</sub> →Q <sub>n</sub>
H	L	L	H	X	X	X	X	Hold: I/O Voltage undetermined
H	L	L	X	H	X	X	X	
H	L	L	L	L	X	X	X	Hold: I/O <sub>n</sub> = Q <sub>n</sub>

H = HIGH Voltage Level  
L = LOW Voltage Level  
X = Immaterial

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## DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter		Limits			Unit	Test Conditions	
			Min	Typ	Max			
V <sub>IH</sub>	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs	
V <sub>IL</sub>	Input LOW Voltage				0.8	V	Guaranteed Input LOW Voltage for All Inputs	
V <sub>IK</sub>	Input Clamp Diode Voltage			-0.65	-1.5	V	V <sub>CC</sub> = MIN, I <sub>IN</sub> = -18 mA	
V <sub>OH</sub>	Output HIGH Voltage I/O <sub>0</sub> -I/O <sub>7</sub>		2.4	3.1		V	V <sub>CC</sub> = MIN, I <sub>OH</sub> = MAX	
V <sub>OH</sub>	Output HIGH Voltage Q <sub>0</sub> , Q <sub>7</sub>		2.7	3.4		V	V <sub>CC</sub> = MIN, I <sub>OH</sub> = MAX	
V <sub>OL</sub>	Output LOW Voltage I/O <sub>0</sub> -I/O <sub>7</sub>			0.25	0.4	V	I <sub>OL</sub> = 12 mA	V <sub>CC</sub> = V <sub>CC</sub> MIN, V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub> per Truth Table
				0.35	0.5	V	I <sub>OL</sub> = 24 mA	
V <sub>OL</sub>	Output LOW Voltage I/O <sub>0</sub> -I/O <sub>7</sub>				0.4	V	I <sub>OL</sub> = 4.0 mA	V <sub>CC</sub> = V <sub>CC</sub> MIN, V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub> per Truth Table
					0.5	V	I <sub>OL</sub> = 8.0 mA	
I <sub>OZH</sub>	Output Off Current HIGH I/O <sub>0</sub> -I/O <sub>7</sub>				40	μA	V <sub>CC</sub> = MAX, V <sub>OUT</sub> = 2.7 V	
I <sub>OZL</sub>	Output Off Current LOW I/O <sub>0</sub> -I/O <sub>7</sub>				-400	μA	V <sub>CC</sub> = MAX, V <sub>OUT</sub> = 0.4 V	
I <sub>IH</sub>	Input HIGH Current		Others		20	μA	V <sub>CC</sub> = MAX, V <sub>IN</sub> = 2.7 V	
			S <sub>0</sub> , S <sub>1</sub> , I/O <sub>0</sub> -I/O <sub>7</sub>		40	μA		
			Others		0.1	mA	V <sub>CC</sub> = MAX, V <sub>IN</sub> = 7.0 V	
			S <sub>0</sub> , S <sub>1</sub> I/O <sub>0</sub> -I/O <sub>7</sub>		0.2	mA		
					0.1	mA	V <sub>CC</sub> = MAX, V <sub>IN</sub> = 5.5 V	
I <sub>IL</sub>	Input LOW Current		Others		-0.4	mA	V <sub>CC</sub> = MAX, V <sub>IN</sub> = 0.4 V	
			S <sub>0</sub> , S <sub>1</sub>		-0.8	mA		
I <sub>OS</sub>	Short Circuit Current (Note 1.)		Q <sub>0</sub> , Q <sub>7</sub>	-20	-100	mA	V <sub>CC</sub> = MAX	
			I/O <sub>0</sub> -I/O <sub>7</sub>	-30	-130	mA	V <sub>CC</sub> = MAX	
I <sub>CC</sub>	Power Supply Current				53	mA	V <sub>CC</sub> = MAX	

1. Not more than one output should be shorted at a time, nor for more than 1 second.

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## AC CHARACTERISTICS ( $T_A = 25^\circ\text{C}$ , $V_{CC} = 5.0\text{ V}$ )

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
$f_{\text{MAX}}$	Maximum Clock Frequency	25	35		MHz	$C_L = 15\text{ pF}$
$t_{\text{PHL}}$ $t_{\text{PLH}}$	Propagation Delay, Clock to $Q_0$ or $Q_7$		26 22	39 33	ns	
$t_{\text{PHL}}$	Propagation Delay, Clear to $Q_0$ or $Q_7$		27	40	ns	
$t_{\text{PHL}}$ $t_{\text{PLH}}$	Propagation Delay, Clock to $I/O_0$ – $I/O_7$		26 17	39 25	ns	$C_L = 45\text{ pF}$ , $R_L = 667\ \Omega$
$t_{\text{PHL}}$	Propagation Delay, Clear to $I/O_0$ – $I/O_7$		26	40	ns	
$t_{\text{PZH}}$ $t_{\text{PZL}}$	Output Enable Time		13 19	21 30	ns	
$t_{\text{PHZ}}$ $t_{\text{PLZ}}$	Output Disable Time		10 10	15 15	ns	$C_L = 5.0\text{ pF}$

## AC SETUP REQUIREMENTS ( $T_A = 25^\circ\text{C}$ , $V_{CC} = 5.0\text{ V}$ )

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
$t_W$	Clock Pulse Width HIGH	25			ns	$V_{CC} = 5.0\text{ V}$
$t_W$	Clock Pulse Width LOW	13			ns	
$t_W$	Clear Pulse Width LOW	20			ns	
$t_s$	Data Setup Time	20			ns	
$t_s$	Select Setup Time	35			ns	
$t_h$	Data Hold Time	0			ns	
$t_h$	Select Hold Time	10			ns	
$t_{\text{rec}}$	Recovery Time	20			ns	

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## 3-STATE WAVEFORMS

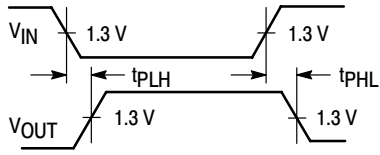


Figure 1.

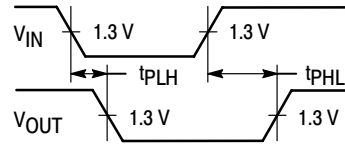


Figure 2.

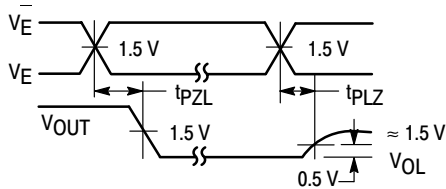


Figure 3.

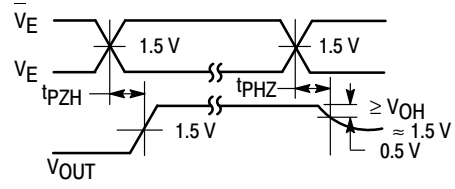
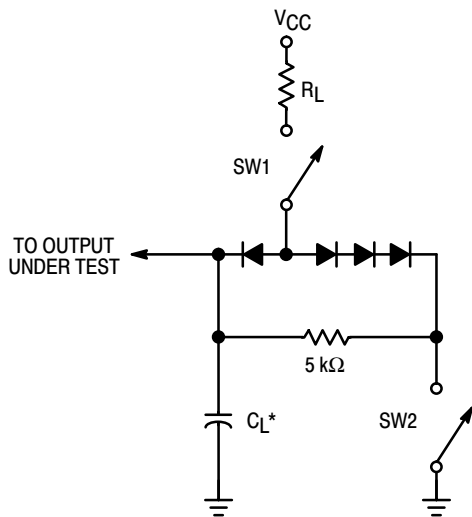


Figure 4.

## AC LOAD CIRCUIT



\* Includes Jig and Probe Capacitance.

Figure 5.

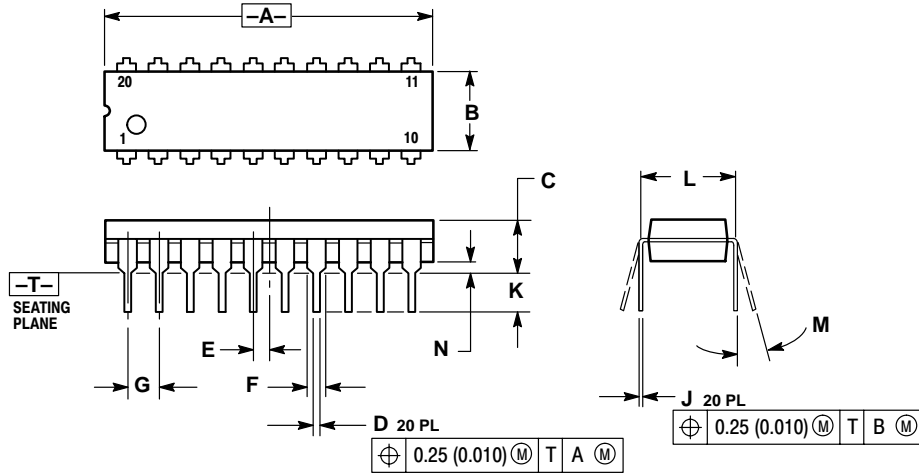
## SWITCH POSITIONS

SYMBOL	SW1	SW2
t <sub>PZH</sub>	Open	Closed
t <sub>PZL</sub>	Closed	Open
t <sub>PLZ</sub>	Closed	Closed
t <sub>PHZ</sub>	Closed	Closed

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## PACKAGE DIMENSIONS

### N SUFFIX PLASTIC PACKAGE CASE 738-03 ISSUE E

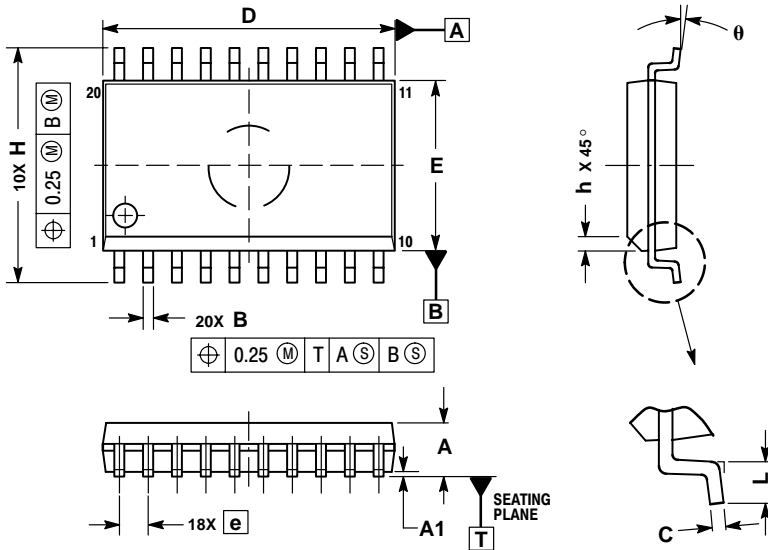


**NOTES:**

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	1.010	1.070	25.66	27.17
B	0.240	0.260	6.10	6.60
C	0.150	0.180	3.81	4.57
D	0.015	0.022	0.39	0.55
E	0.050 BSC		1.27 BSC	
F	0.050	0.070	1.27	1.77
G	0.100 BSC		2.54 BSC	
J	0.008	0.015	0.21	0.38
K	0.110	0.140	2.80	3.55
L	0.300 BSC		7.62 BSC	
M	0°	15°	0°	15°
N	0.020	0.040	0.51	1.01

### DW SUFFIX PLASTIC SOIC PACKAGE CASE 751D-05 ISSUE F



**NOTES:**

1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
5. DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF B DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS	
	MIN	MAX
A	2.35	2.65
A1	0.10	0.25
B	0.35	0.49
C	0.23	0.32
D	12.65	12.95
E	7.40	7.60
e	1.27 BSC	
H	10.05	10.55
h	0.25	0.75
L	0.50	0.90
theta	0°	7°

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