FAIRCHILD
SEMICONDUCTOR®

November 2007

74OL6000, 74OL6001, 74OL6010, 74OL6011
Optoplanar® High-Speed Logic-to-Logic Optocouplers

LSTTL to	
TTL Buffer	**74OL6000**
TTL Inverter	**74OL6001**
CMOS Buffer	**74OL6010**
CMOS Inverter	**74OL6011**

Features

- Industry first LSTTL to TTL and LSTTL to CMOS complete logic-to-logic optocoupler
- Incorporates LED drive circuitry — use as a logic gate
- Very high speed
- Choice of buffer or inverter
- Choice of TTL or CMOS compatible output up to 15 volts
- Fan-out of 10 TTL loads, fan-in 1 LSTTL load
- Internal noise shield — very high CMR of ±15kV/μS
- UL recognized (File #E90700)
- Same noise immunity as LSTTL/TTL.

Applications

- Transmission line interface — receiver and driver
- Excellent as bridged receiver in fast LAN highways
- Bus interface
- Logic family interface with ground loop noise elimination
- High speed AC/DC voltage sensing
- Driver for power semiconductor devices
- Level shifting
- Replaces fast pulse transformers

Description

OPTOLOGIC™ is the first family of truly logic compatible optically coupled logic interface gates.

The family consists of four device types offering LSTTL to TTL and LSTTL to CMOS interfacing. Each of these interfacing functions is available as a buffer (A = B), or as an inverter (A = $\overline{B}$).

The LSTTL input compatibility is provided by an input integrated circuit, with industry standard logic levels. This input amplifier IC switches a temperature compensated current source driving a high speed 850nm AlGaAs LED emitter. This novel integration scheme eliminates CTR degradation over time and temperature.

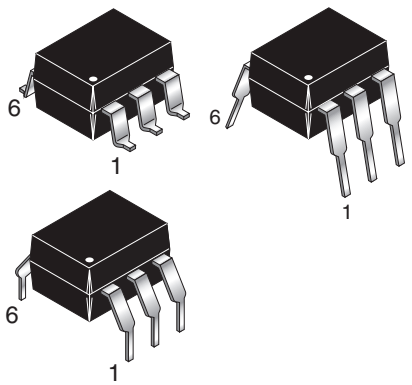
The emitter is optically coupled to an integrated photodetector/high-gain, high-speed output amplifier IC. The superior 15kV/μS common-mode noise rejection is ensured through the use of an optically transparent noise shield.

The TTL compatible output has a totem-pole with a fan-out of 10. The CMOS compatible output has an open collector Schottky-clamped transistor that interfaces to any CMOS logic between 4.5 and 15 volts. The 74OL6010/11 may also by used to drive power MOSFETs or transistors up to 15 volts.

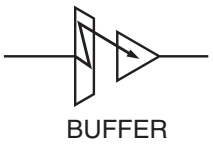
The Optologic coupler family typically offers propagation of delays of 60 ns and can support 15 MBaud data communication.

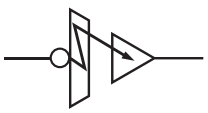
The two input chips and the output chip are assembled in a 6-pin DIP high insulation voltage plastic package. Fairchild's proprietary OPTOPLANAR® construction provides a withstand test voltage of 5300 VRMS (1 minute).

Package

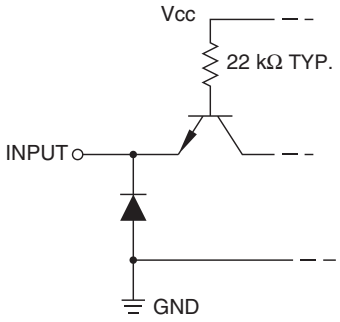


Symbol

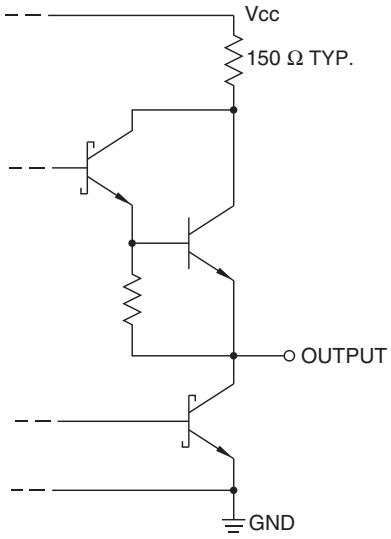

BUFFER


INVERTER

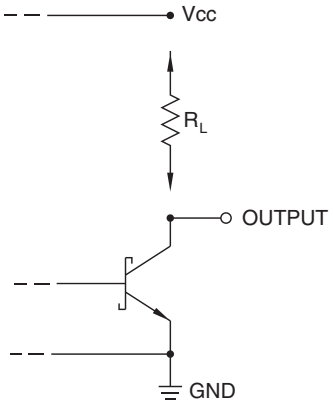
Circuit Diagrams



LSTTL INPUT CIRCUIT



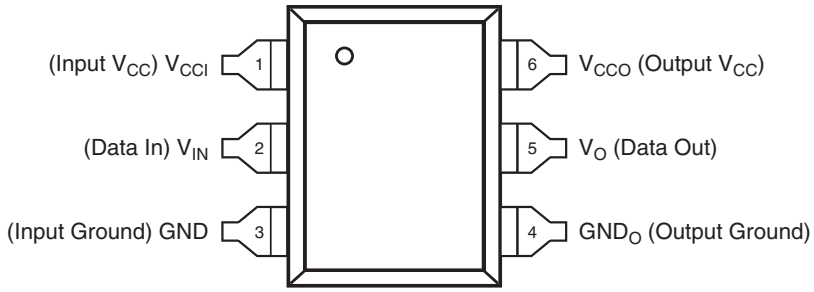
TTL OUTPUT CIRCUIT



CMOS OUTPUT CIRCUIT

All Inputs | **74OL6000/01 Output** | **74OL6010/11 Output**

Pin Configuration

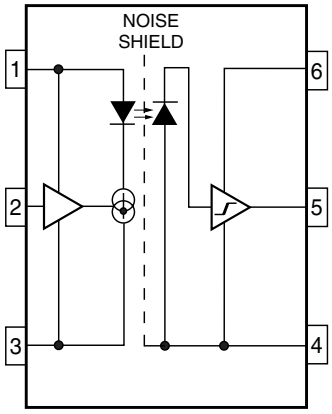


Device Configuration

Part Number	Logic Compatibility		Logic Function	Output Configuration
	Input	Output		
74OL6000	LSTTL	TTL	Buffer	Totem Pole
74OL6001	LSTTL	TTL	Inverter	Totem Pole
74OL6010	LSTTL	CMOS	Buffer	Open Collector
74OL6011	LSTTL	CMOS	Inverter	Open Collector

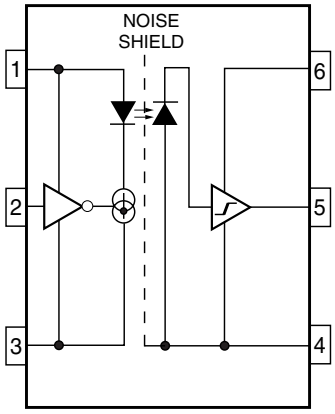
Schematics

74OL6000



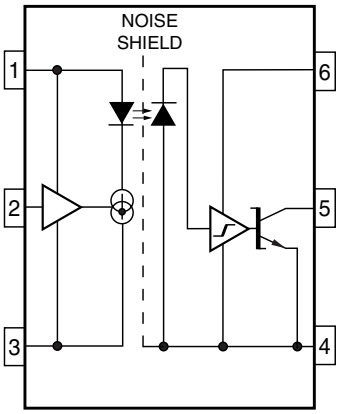
LSTLL to TTL Buffer

74OL6001



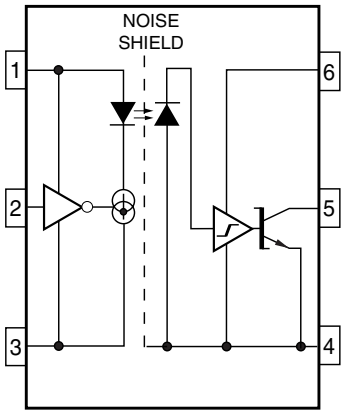
LSTLL to TTL Inverter

74OL6010



LSTLL to CMOS Buffer

74OL6011



LSTLL to CMOS Inverter

Absolute Maximum Ratings (T_A = 25°C unless otherwise specified)

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter	Device	Value	Units
TOTAL DEVICE				
T_{STG}	Storage Temperature	All	-55 to +125	°C
T_{OPR}	Operating Temperature	All	0 to +70	°C
T_{SOL}	Lead Solder Temperature	All	260 for 10 sec	°C
P_D	Power Dissipation	All	350	mW
EMITTER				
V_{CCI}	Input Supply Voltage	All	7	V
V_{IN}	Input Voltage	All	7	V
DETECTOR				
$I_{O\ (avg)}$	Average Output Current	All	40	mA
V_{CCO}	Output Supply Voltage	74OL6000/01	7	V
		74OL6010/11	18	
V_O	Output Voltage	74OL6000/01	7	V
		74OL6010/11	18	

Electrical Characteristics (T_A = 0°C to 70°C unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units	Fig.
CM_H	Common Mode Transient Immunity at Logic High Level Output	V_{CCI} = 5V, V_{CCO} = 5V, V_{CM} = 50 Vp-p	5000	15000		V/µS	16, 19
CM_L	Common Mode Transient Immunity at Logic Low Level Output	V_{CCI} = 5V, V_{CCO} = 5V, V_{CM} = 50 Vp-p	-5000	-15000		V/µS	16, 19
C_{CM}	Common Mode Coupling Capacitance			0.005		pF	
C_{I-O}	Capacitance (input-output)(1)	V_{I-O} = 0, f = 1MHz		0.7		pF	
V_{ISO}	Withstand Insulation Test Voltage(1)	T_A = 25°C, t = 1 min, $I_{I-O} \leq$ 2mA	5300			VRMS	
R_{ISO}	Insulation Resistance(1)	V_{I-O} = 500 VDC		10^{11}		Ω	

Note:

1. Device considered a two-terminal device. Pins 1, 2 and 3 shorted together, and Pins 4, 5 and 6 shorted together.

Electrical Characteristics (T_A = 0°C to 70°C unless otherwise specified)

TTL Output 74OL6000, 74OL6001(2)

Symbol	Parameter	Test Conditions			Min.	Typ.*	Max.	Units
		74OL6000	74OL6001	74OL6000/01				
V_{CCI}	Input Supply Voltage				4.5	5.0	5.5	V
V_{CCO}	Output Supply Voltage				4.5	5.0	5.5	V
V_{IH}	High-Level Input Voltage				2.0			V
V_{IL}	Low-Level Input Voltage						0.8	V
V_{IK}	Input Clamp Voltage			V_{CCI} = 4.5V, I_I = -18mA			-1.2	V
I_{IH}	High-Level Input Current			V_{CCI} = 5.5V, V_{IH} = 4.5V		1.0	40.0	µA
I_{IL}	Low-Level Input Current			V_{CCI} = 5.5V, V_{IL} = 0.4V		-200.0	-400.0	µA
I_{CCIH}	Input Supply Current (HIGH)			V_{CCI} = 5.5V, V_{IN} = V_{IH}		10.0	14.0	mA
I_{CCIL}	Input Supply Current (LOW)			V_{CCI} = 5.5V, V_{IN} = V_{IL}		10.0	14.0	mA
V_{OH}	High-Level Output Voltage	V_{IN} = 2.0V	V_{IN} = 0.8V	V_{CCI} = 4.5V, V_{CCO} = 4.5V, I_{OH} = -400µA	2.4	3.0		V
V_{OL}	Low-Level Output Voltage	V_{IN} = 0.8V	V_{IN} = 2.0V	V_{CCI} = 4.5V, V_{CCO} = 4.5V, I_{OL} = 16mA		0.3	0.6	V
				V_{CCI} = 4.5V, V_{CCO} = 4.5V, I_{OL} = 4mA			0.5	
I_{OH}	High-Level Output Current	V_{IN} = V_{IH}	V_{IN} = V_{IL}	V_{CCI} = 4.5V, V_{CCO} = 4.5V, V_{OH} = 2.4V		-8.0	-10.0	mA
I_{OL}	Low-Level Output Current	V_{IN} = 0.8 V	V_{IN} = 2.0V	V_{CCI} = 4.5V, V_{CCO} = 4.5V, V_{OL} = 0.6V	16.0			mA
I_{OS}	Short-Circuit Output Current	V_{IN} = V_{IH}	V_{IN} = V_{IL}	V_{CCI} = 5.5V, V_{CCO} = 5.5V,	-5.0	-25.0	-40.0	mA
I_{CCOH}	Output Supply Current (HIGH)	V_{IN} = V_{IH}	V_{IN} = V_{IL}	V_{CCI} = 5.5V, V_O = V_{OH}, V_{CCO}= 5.5V		9.0	15.0	mA
I_{CCOL}	Output Supply Current (LOW)	V_{IN} = V_{IL}	V_{IN} = V_{IH}	V_{CCI} = 5.5V, V_O = V_{OL}, V_{CCO} = 5.5V		8.0	12.0	mA

*All typical values are at T_A=25°C

Switching Characteristics (T_A = 25°C unless otherwise specified)

TTL Output 74OL6000, 74OL6001(2)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units	Fig.
t_{PHL}	Propagation Delay Time For Output Low Level	V_{CCI} = 5V, V_{CCO} = 5V		60	100	ns	15, 17
t_{PLH}	Propagation Delay Time For Output High Level			70	100	ns	15, 17
t_r	Output Rise Time For Output High Level			45		ns	15, 17
t_f	Output Fall Time For Output Low Level			5		ns	15, 17

Note:

2. The V_{CCO} and V_{CCI} supply voltages to the device must each be bypassed by a 0.1µF capacitor or larger. This can be either a ceramic or solid tantalum capacitor with good high frequency characteristics. Its purpose is to stabilize the operation of the high-gain amplifiers. Failure to provide the bypass will impair the DC and switching properties. The total lead length between capacitor and optocoupler should not exceed 1.5mm. See Fig. 20.

Electrical Characteristics (T_A = 0°C to 70°C Unless otherwise specified)

CMOS Output 74OL6010 and 74OL6011[3]

Symbol	Parameter	Test Conditions			Min.	Typ.*	Max.	Units
		74OL6010	74OL6011	74OL6010/11				
V_{CCI}	Input Supply Voltage				4.5	5.0	5.5	V
V_{CCO}	Output Supply Voltage[4]				4.5		15.0	V
V_{IH}	High-Level Input Voltage				2.0			V
V_{IL}	Low-Level Input Voltage						0.8	V
V_{IK}	Input Clamp Voltage			V_{CCI} = 4.5V, I_I = -18mA			-1.2	V
I_{IH}	High-Level Input Current			V_{CCI} = 5.5V, V_{IH} = 4.5V		1.0	40.0	µA
I_{IL}	Low-Level Input Current			V_{CCI} = 5.5V, V_{IL} = -0.4V		-200.0	-400.0	µA
I_{CCIH}	Input Supply Current (HIGH)			V_{CCI} = 5.5V, V_{IN} = V_{IH}		10.0	14.0	mA
I_{CCIL}	Input Supply Current (LOW)			V_{CCI} = 5.5V, V_{IN} = V_{IL}		10.0	14.0	mA
V_{OL}	Low-Level Output Voltage	V_{IN} = 0.8V	V_{IN} = 2.0V	V_{CCI} = 4.5V, V_{CCO} = 4.5V, I_{OL} = 16mA		0.4	0.6	V
				V_{CCI} = 4.5V, V_{CCO} = 4.5V, I_{OL} = 4mA			0.5	
I_{OH}	High-Level Output Current	V_{IN} = V_{IH}	V_{IN} = V_{IL}	V_{CCI} = 4.5V, V_{OH} = 15V, V_{CCO} = 4.5–15V		1.0	100.0	µA
I_{OL}	Low-Level Output Current	V_{IN} = 0.8V	V_{IN} = 2.0V	V_{CCI} = 4.5V, V_{OL} = 0.6V, V_{CCO} = 4.5–15V	16.0			mA
I_{CCOH}	Output Supply Current (HIGH)	V_{IN} = V_{IH}	V_{IN} = V_{IL}	V_{CCI} = 5.5V, V_O = V_{OH}, V_{CCO} = 4.5V		9.0	12.0	mA
				V_{CCI} = 5.5V, V_O = V_{OL}, V_{CCO} = 15V		11.0	18.0	
I_{CCOL}	Output Supply Current (LOW)	V_{IN} = V_{IL}	V_{IN} = V_{IH}	V_{CCI} = 5.5V, V_O = V_{OL}, V_{CCO} = 4.5V		8.0	12.0	mA
				V_{CCI} = 5.5V, V_O = V_{OL}, V_{CCO} = 15V		11.0	18.0	

*All typical values are at T_A=25°C

Switching Characteristics (T_A = 25°C Unless otherwise specified)

TTL Output 74OL6010 and 74OL6011[3]

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units	Fig.
t_{PHL}	Propagation Delay Time For Output Low Level	V_{CCI} = 5V, V_{CCO} = 5V, R_L = 470Ω		60	120	ns	15, 18
t_{PLH}	Propagation Delay Time For Output High Level			100	180	ns	15, 18
t_r	Output Rise Time For Output High Level			50		ns	15, 18
t_f	Output Fail Time For Output Low Level			5		ns	15, 18

Notes:

3. The V_{CCO} and V_{CCI} supply voltages to the device must each be bypassed by a 0.1µF capacitor or larger. This can be either a ceramic or solid tantalum capacitor with good high frequency characteristics. Its purpose is to stabilize the operation of the high-gain amplifiers. Failure to provide the bypass will impair the DC and switching properties. The total lead length between capacitor and optocoupler should not exceed 1.5mm. See Fig. 20.
4. For example, assuming a V_{CCI} of 5.0V, and an ambient temperature of 70°C, the maximum allowable V_{CCO} is 12.1V.

Typical Performance Curves

Figure 1. Input Current vs. Ambient Temperature

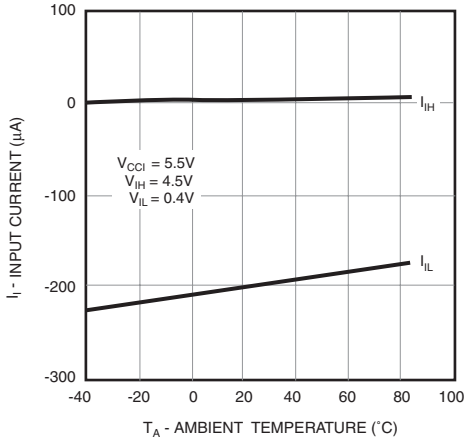


Figure 2. Input Supply Current vs. Ambient Temperature

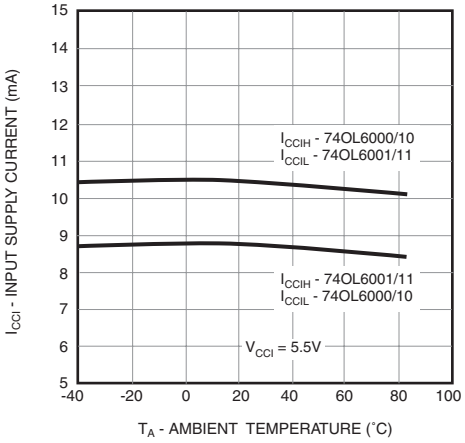


Figure 3. Output Supply Current vs. Ambient Temperature

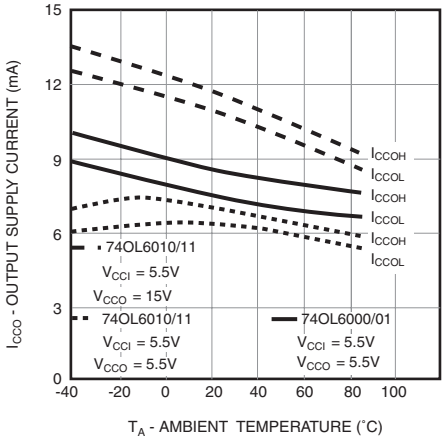


Figure 4. Output Current vs. Ambient Temperature

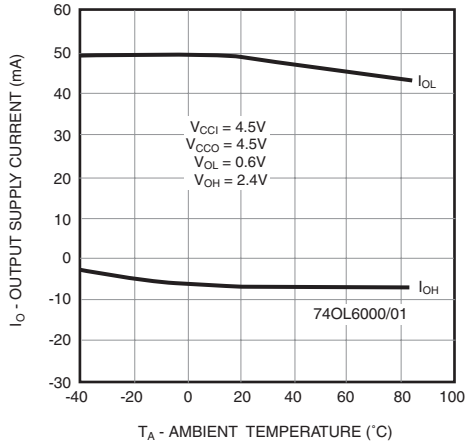


Figure 5. High-Level Output Voltage vs. Ambient Temperature

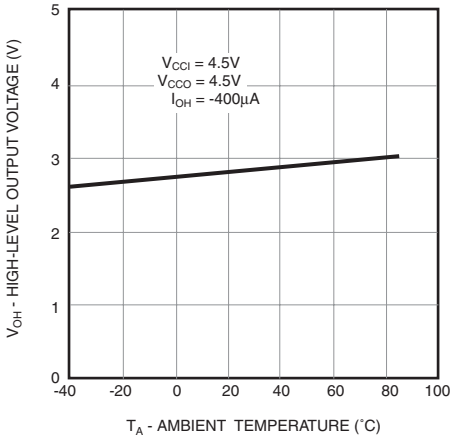
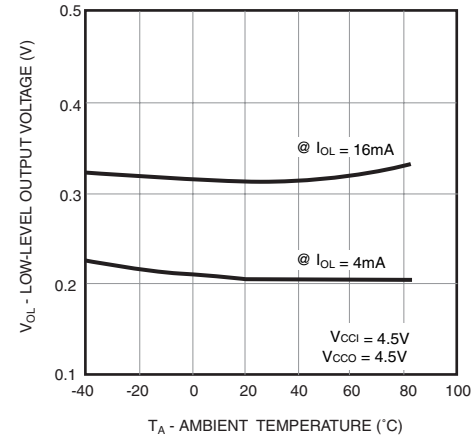


Figure 6. Low-Level Output Voltage vs. Ambient Temperature



Typical Performance Curves (Continued)

Figure 7. 74OL6010/11 Leakage Current vs. Ambient Temperature

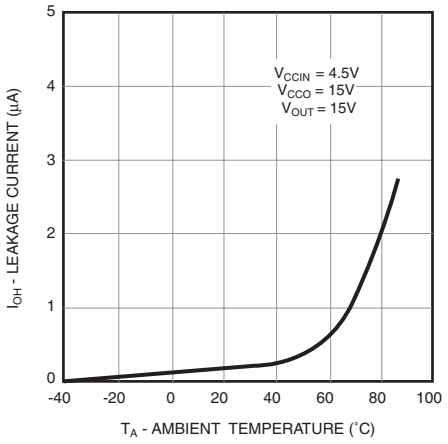


Figure 8. 74OL6000/01 Switching Times vs. Ambient Temperature

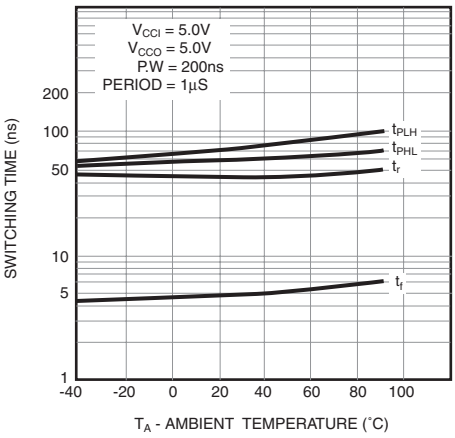


Figure 9. 74OL6010/11 Switching Times vs. Ambient Temperature

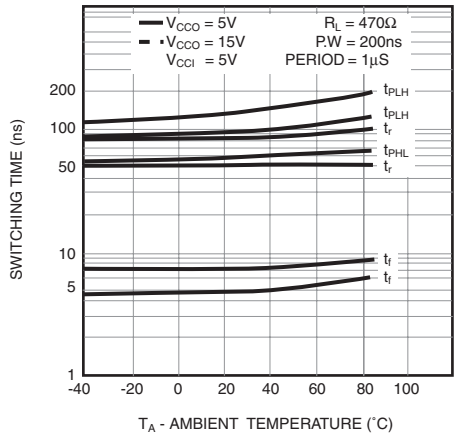


Figure 10. Common Mode Rejection vs. Common Mode Voltage

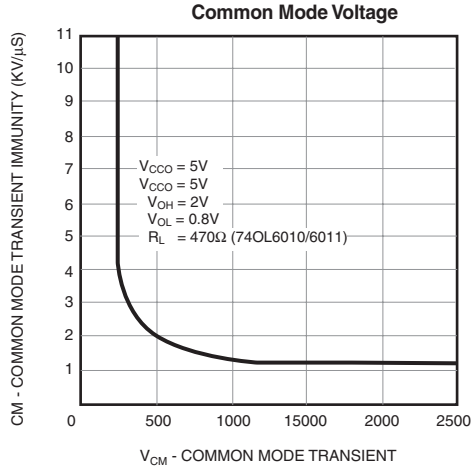


Figure 11. Supply Current vs. Supply Voltage

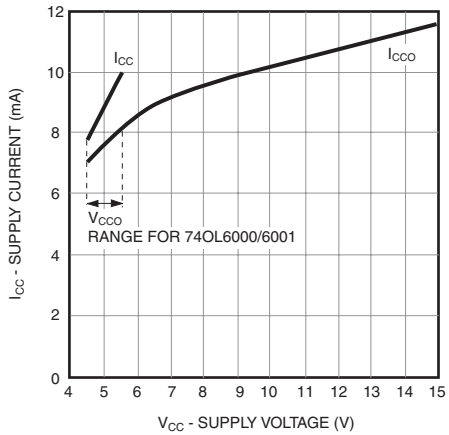
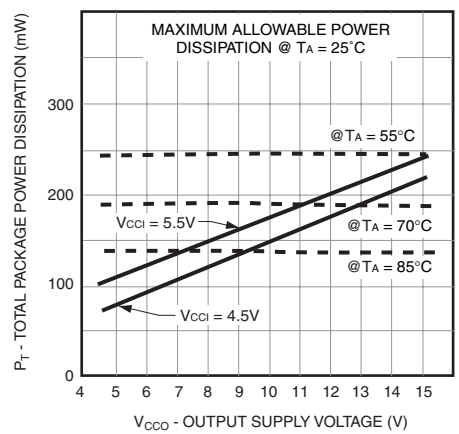


Figure 12. Power Dissipation vs. Ambient Temperature



Typical Performance Curves (Continued)

Figure 13. Input Threshold Voltage vs. Ambient Temperature

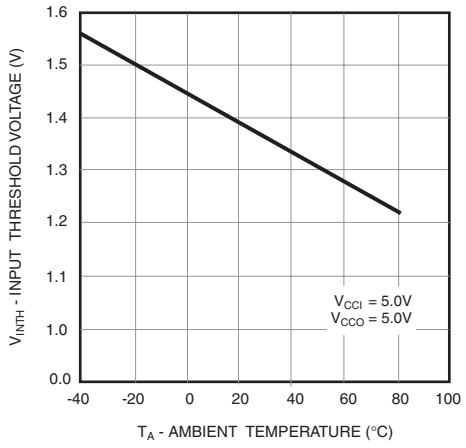
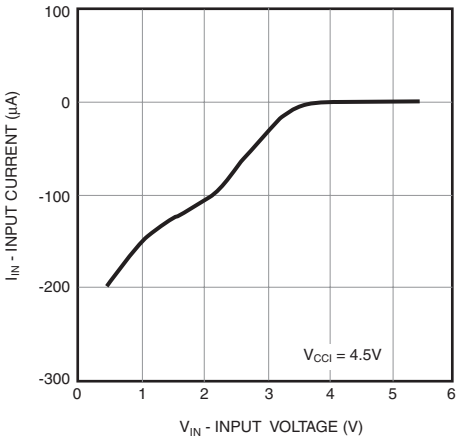


Figure 14. Input Current vs. Input Voltage



Test Circuits

Figure 15. Switching Time Test Circuit

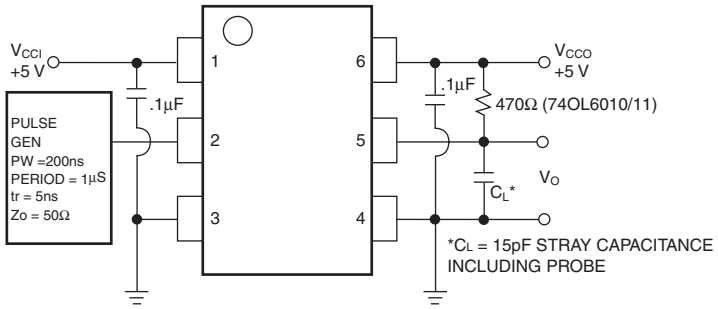
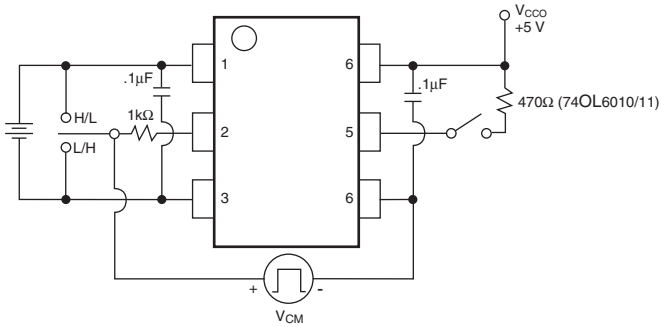


Figure 16. Common Mode Rejection Test Circuit



Switching and Rejection Waveforms

Figure 17. 74OL6000/01 Switching Times vs. Ambient Temperature

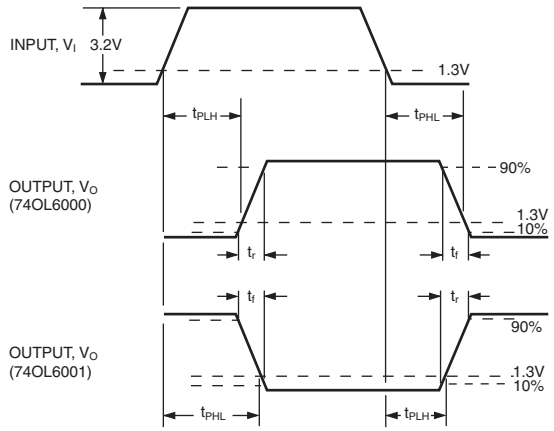


Figure 18. Switching Parameters 74OL6010/11

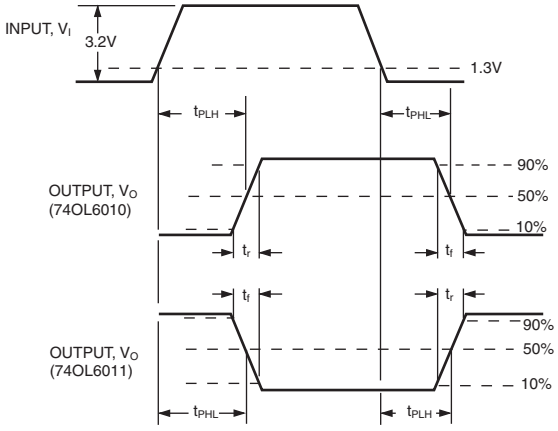
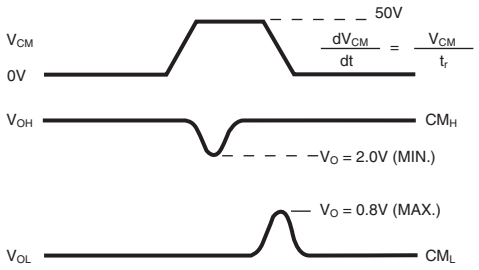
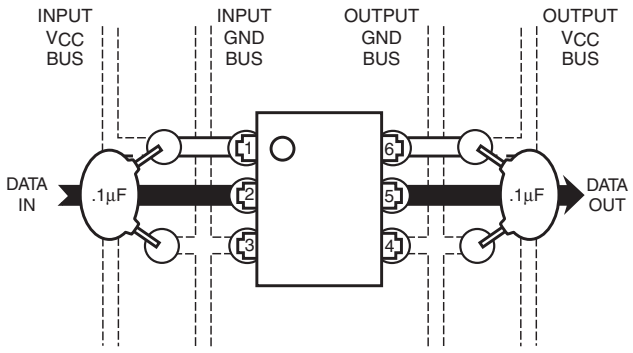


Figure 19. Common Mode Rejection Waveforms



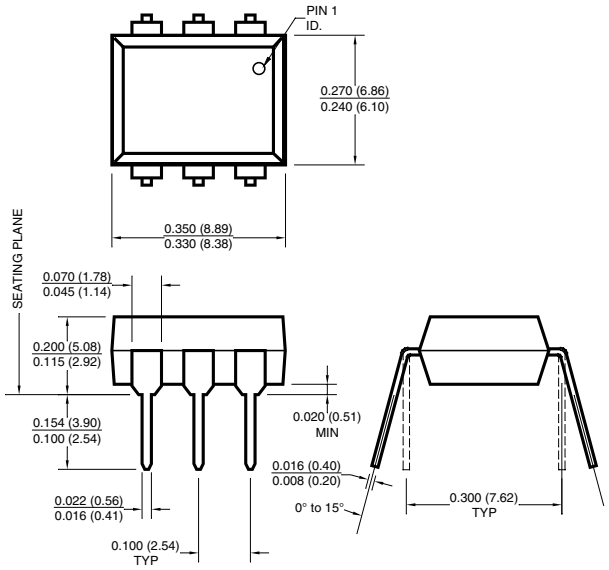
PCB Layout

Figure 20. Suggested PCB Layout

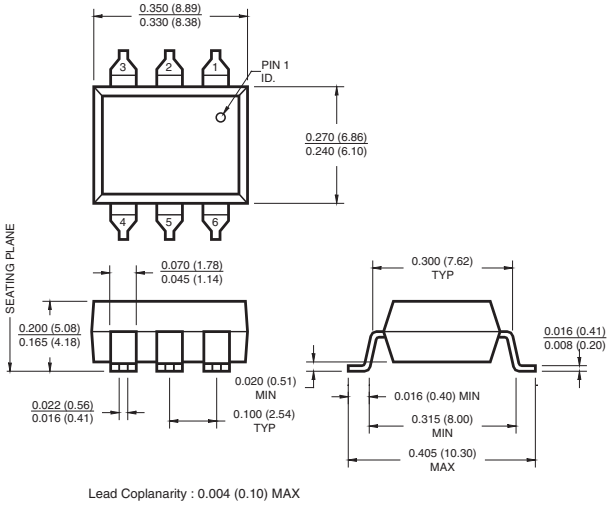


Package Dimensions

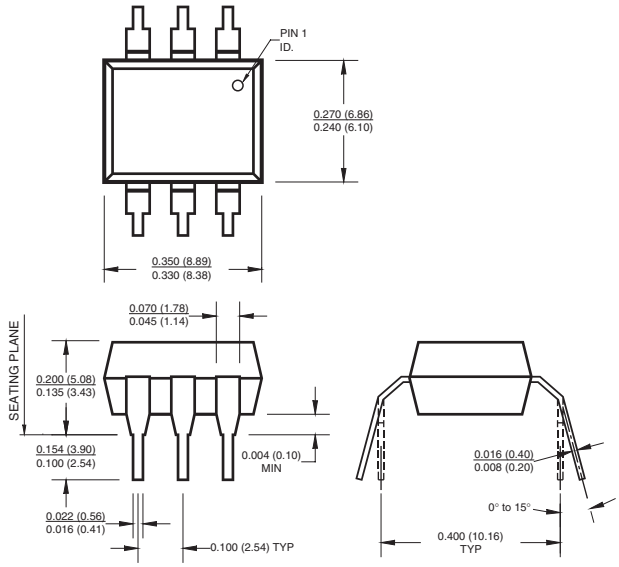
Through Hole



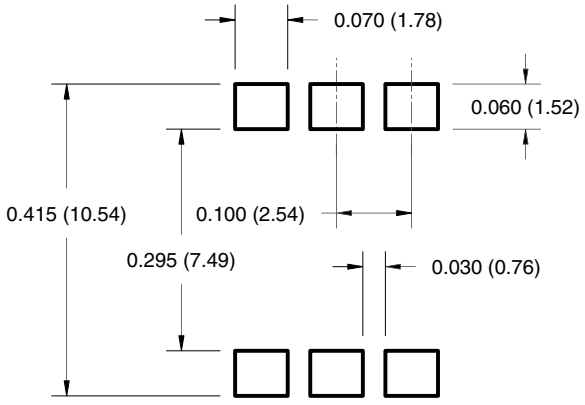
Surface Mount



0.4" Lead Spacing



Recommended Pad Layout for Surface Mount Leadform

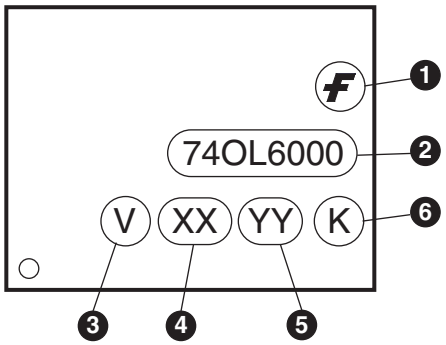


Note:
All dimensions are in inches (millimeters).

Ordering Information

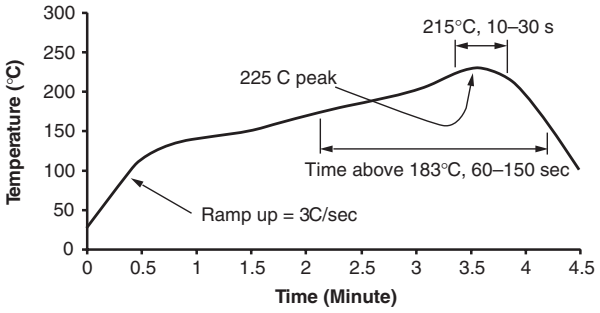
Option	Order Entry Identifier	Description
S	.S	Surface Mount Lead Bend
SD	.SD	Surface Mount; Tape and Reel
W	.W	0.4" Lead Spacing
300	.300	VDE 0884
300W	.300W	VDE 0884, 0.4" Lead Spacing
3S	.3S	VDE 0884, Surface Mount
3SD	.3SD	VDE 0884, Surface Mount, Tape and Reel

Marking Information



Definitions	
1	Fairchild logo
2	Device number
3	VDE mark (Note: Only appears on parts ordered with VDE option – See order entry table)
4	Two digit year code, e.g., ‘03’
5	Two digit work week ranging from ‘01’ to ‘53’
6	Assembly package code

Reflow Profile



- Peak reflow temperature: 225°C (package surface temperature)
- Time of temperature higher than 183°C for 60–150 seconds
- One time soldering reflow is recommended

Application

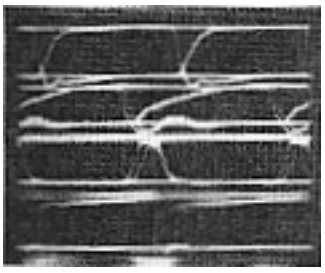
Local area data communication systems can greately improve their noise immunity by including OPOTOLOGIC gates in the design.

The Optologic input amplifier offers the feature of very high input impedance that permits their use as bridged line receivers. The system show above illustrates an optically isolated transmitter and multidrop receiver system. The network uses a 74OL6000 and buffer (Figure D) to isolate the transmitter and drive the 75Ω coax cable. This application uses a 1000 ft. aerial suspension 75Ω CATV coax cable with data taps at 250 ft. intervals. The 74OL6001s function as bridged receivers, and as many as 30 receivers could be placed along the line with minimal signal degradation. The communication cable is terminated with a single 75Ω load at the far end of the line.

Signal quality "Eye Pattern" is shown in Figures A, B and C with a 10MBaud NRZ Psuedo-Random Sequence (PRS). Traces 1-3 in Figure A describes the transmitter section. Traces 4-7 in Figure B show the output of the four Optologic bridged terminations. Traces 8-11 in Figure C illustrate "Eye Pattern" as seen at the output of a 74LS04 logic gate. The data quality is well preserved in that only a 30% Eye closure is seen at the receiver located 1000 ft. from the transmitter.

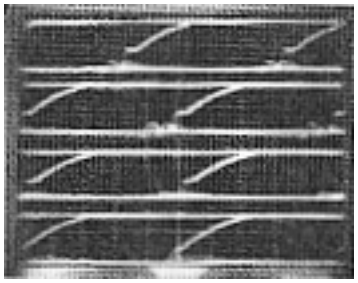
The data communication system is completely optically isolated from all of the terminal equipments. Power for the transmitter (V_{CCO}) and receiver (V_{CCI}) is taken from an isolated power supply and distributed through a drain or messenger wire.

Figure A



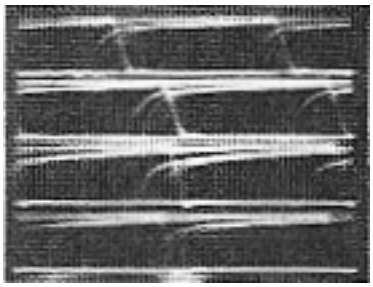
HORIZONTAL = 20ns/DIV 42-11
VERTICAL = 2V/DIV

Figure B

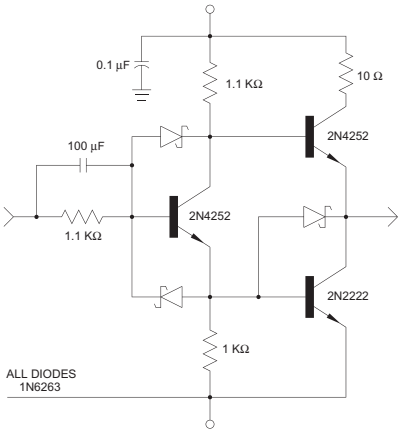


HORIZONTAL = 20ns/DIV 42-12, 02
VERTICAL = 2V/DIV

Figure C



HORIZONTAL = 20ns/DIV 42-13/03
VERTICAL = 2V/DIV



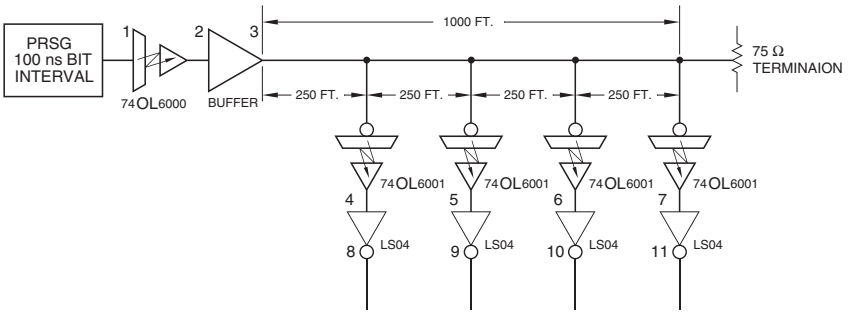


Figure D Buffer

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QS™
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Quiet Series™
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SMART START™
SPM®
STEALTH™
SuperFET™
SuperSOT™-3
SuperSOT™-6
SuperSOT™-8
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Preliminary	First Production	This datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
No Identification Needed	Full Production	This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
Obsolete	Not In Production	This datasheet contains specifications on a product that has been discontinued by Fairchild Semiconductor. The datasheet is printed for reference information only.

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