# 8-Bit Latch

Description

CXQ71082 and CXQ71083 are CMOS 8-bit transparent latches with three-state output buffers. They are used as bus buffers or bus multiplexers in microprocessor systems. Their high-drive capability makes them suitable for data latch, buffer or I/O port applications.

Features

- Transparent operation
- 8-bit parallel data register
- Three-state output buffer
- High drive capability output buffer ($I_{OL}=12$ mA)
- 8086, 8088, CXQ70108 and CXQ70116 CPU bus compatible
- CXQ71082: non-inverted output
  CXQ71083: inverted output
- CMOS technology
- +5V single power supply
- 20-pin plastic DIP (300 mil)
- NEC μPD71082, μPD71083 compatible

Pin Configulation (Top View)

Block Diagram

CXQ71082

CXQ71083

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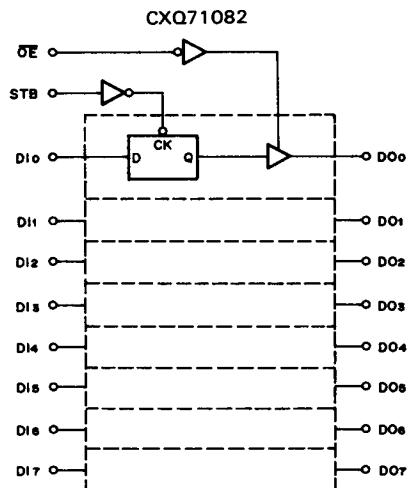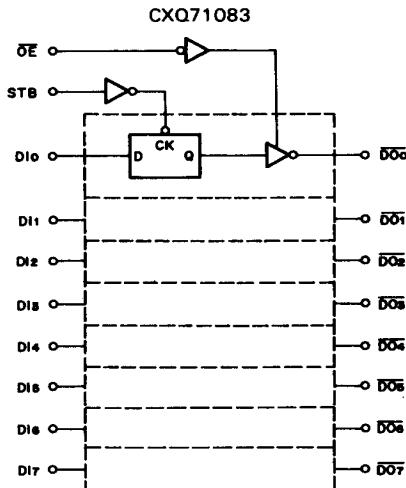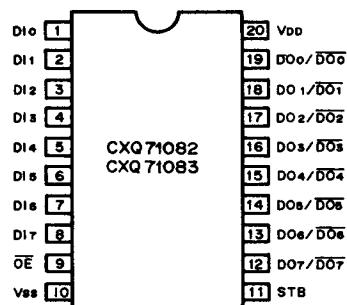
Pin Identification

No.	Symbol	Direction	Function
1	DI$_0$	In	Data input, bit 0
2	DI$_1$	In	Data input, bit 1
3	DI$_2$	In	Data input, bit 2
4	DI$_3$	In	Data input, bit 3
5	DI$_4$	In	Data input, bit 4
6	DI$_5$	In	Data input, bit 5
7	DI$_6$	In	Data input, bit 6
8	DI$_7$	In	Data input, bit 7
9	$\overline{OE}$	In	Output enable input
10	V$_{SS}$		Ground
11	STB	In	Strobe input
12	DO$_7$/$\overline{DO_7}$	Out	Data output, bit 7
13	DO$_6$/$\overline{DO_6}$	Out	Data output, bit 6
14	DO$_5$/$\overline{DO_5}$	Out	Data output, bit 5
15	DO$_4$/$\overline{DO_4}$	Out	Data output, bit 4
16	DO$_3$/$\overline{DO_3}$	Out	Data output, bit 3
17	DO$_2$/$\overline{DO_2}$	Out	Data output, bit 2
18	DO$_1$/$\overline{DO_1}$	Out	Data output, bit 1
19	DO$_0$/$\overline{DO_0}$	Out	Data output, bit 0
20	V$_{DD}$		Power supply

Pin Functions

DI$_7$-DI$_0$ [Data Input]

DI$_7$-DI$_0$ are data input lines to the 8-bit data latch. Data on DI lines are latched with the trailing edge of STB (high to low). The data passes through the latch while STB is high.

DO$_7$-DO$_0$/$\overline{DO_7}$-$\overline{DO_0}$ [Data Output]

DO$_7$-DO$_0$/$\overline{DO_7}$-$\overline{DO_0}$ are data output lines from the 8-bit data latch. When $\overline{OE}$ is high, these lines float to the high-impedance state. When $\overline{OE}$ is low, data from the latch is output, either non-inverted (CXQ71082) or inverted (CXQ71083).

STB [Strobe]

STB is the strobe signal for the 8-bit latch. When STB is high, data on the DI lines passes through the 8-bit latch. Data is latched on the trailing edge of STB (high to low). When STB is low, latched data is stable.

$\overline{OE}$ [Output Enable]

$\overline{OE}$ is the output enable signal for the DO lines. When $\overline{OE}$ is high, DO lines are high impedance. When $\overline{OE}$ is low, data from the 8-bit latch is output to DO$_7$-DO$_0$.

STB	OE̅	DO₇-DO₀	8-Bit Data Latch
Low	Low	Latched data from 8-bit data latch	DI line data has been latched with trailing edge of STB (high→low)
	High	High impedance	
High	Low	Data on DI₇-DI₀	Pass through
	High	High impedance	

Absolute Maximum Ratings   (Ta=25°C, Vss=0V)

Parameter	Symbol	Rating Value	Unit
Power supply voltage	V$_{DD}$	−0.5 to +7.0	V
Input voltage	V$_I$	−1.0 to V$_{DD}$+1.0	V
Output voltage	V$_O$	−0.5 to V$_{DD}$+0.5	V
Power dissipation	P$_{DMAX}$	500	mW
Operating temperature	Topr	−40 to +85	°C
Storage temperature	Tstg	−65 to +150	°C

Comment: Exposing the device to stresses above those listed in the absolute maximum ratings could cause permanent damage. Exposure to absolute maximum ratings for extended periods may affect device reliability.

DC Characteristics   (Ta=−40 to +85°C, V$_{DD}$=5V±10%)

Parameter	Symbol	Min.	Max.	Unit	Test Conditions
Input voltage high	V$_{IH}$	2.2		V	
Input voltage low	V$_{IL}$		0.8	V	
Output voltage high	V$_{OH}$	V$_{DD}$−0.8		V	I$_{OH}$=−4 mA
Output voltage low	V$_{OL}$		0.45	V	I$_{OL}$=12 mA
Input current	I$_I$	−1.0	1.0	μA	V$_I$=V$_{DD}$, Vss
Leakage current at high impedance	I$_{OFF}$	−10	10	μA	OE̅=V$_{DD}$
Power supply current (static)	I$_{DD}$		80	μA	V$_I$=V$_{DD}$, Vss
Power supply current (dynamic)	I$_{DDdyn}$		20	mA	f$_{IN}$=1 MHz C=200 pF

Capacitance   (Ta=25°C, V$_{DD}$=+5V)

Parameter	Symbol	Min.	Max.	Unit	Test Conditions
Input capacitance	C$_{IN}$		12	pF	fc=1 MHz

AC Characteristics

(Ta=−40 to +85°C, V$_{DD}$=5V±10%)

| Parameter	Symbol	Min.	Max.	Unit	Test Conditions
Input to output delay	t$_{DIO}$	5	40	ns	Load circuit [a]
STB to output delay	t$_{DSTBO}$	10	60	ns	Load circuit [a]
Data float time from $\overline{OE}$ high	t$_{FCTO}$	5	30	ns	Load circuit [b]
Data output delay from $\overline{OE}$ low	t$_{DCTO}$	10	40	ns	Load circuit [b]
Input to STB setup time	t$_{SISTB}$	0		ns	Load circuit [a]
Input to STB hold time	t$_{HSTBI}$	25		ns	Load circuit [a]
STB high time	t$_{STB}$	20		ns	Load circuit [a]
Signal rise time	t$_{LH}$		20	ns	0.8V to 2.0V
Signal fall time	t$_{HL}$		12	ns	2.0V to 0.8V

Timing Diagram
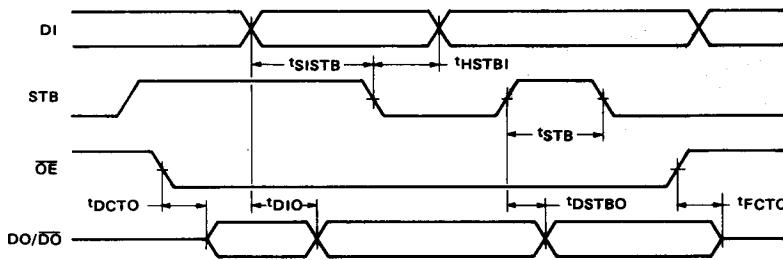
AC Testing Waveform

Loading Circuits for AC Testing

[a] V$_{OL}$, V$_{OH}$ Outputs
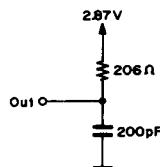
[b] Three-State Outputs
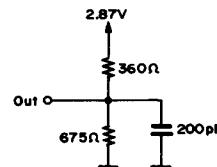
Loading Conditions: I$_{OL}$ = 12 mA, I$_{OH}$ = −4 mA, C$_L$ = 200 pF

Functional Description

The CXQ71082 and CXQ71083 are 8-bit data latches strobed by the STB signal with high-drive capability output buffers controlled by the $\overline{OE}$ signal. Data on the DI lines latched by the trailing edge of STB (high to low). When STB is high, data passes through the latch. When $\overline{OE}$ is high, DO lines are high impedance. When $\overline{OE}$ is low, the contents of the latches are output on DO_7-DO_0. The DO lines are isolated from $\overline{OE}$ switching noise.

Package Outline   Unit: mm

20 pin DIP