HD74LV2GT241A

Dual Bus Buffer Noninverted with 3–state Output

HITACHI

ADE-205-679 (Z)

Rev. 0
Mar. 2002

Description

The HD74LV2GT241A has dual bus buffer noninverted with 3–state output in a 8 pin package. Two noninverters are included in one circuit. Each circuit can be independently controlled by the enable signal $\overline{OE}$ or OE, which enables outputs when receiving a low or high level signal, respectively. Low voltage and high speed operation is suitable for the battery powered products (e.g., notebook computers), and the low power consumption extends the battery life.

Features

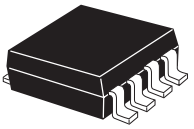
- The basic gate function is lined up as hitachi uni logic series.
- Supplied on emboss taping for high speed automatic mounting.
- TTL compatible input level.
  Supply voltage range : 4.5 to 5.5 V
  Operating temperature range : –40 to +85°C
- All inputs V_{IH} (Max.) = 5.5 V (@V_{CC} = 0 V to 5.5 V)
  All outputs V_O (Max.) = 5.5 V (@V_{CC} = 0 V, Output : Z)
- Output current ±12 mA (@V_{CC} = 4.5 V to 5.5 V)
- All the logical input has hysteresis voltage for the slow transition.
- Package type

Package type	Package code	Package suffix	Taping code
SSOP-8 pin	TTP-8DB	US	E (3,000 pcs / Reel)

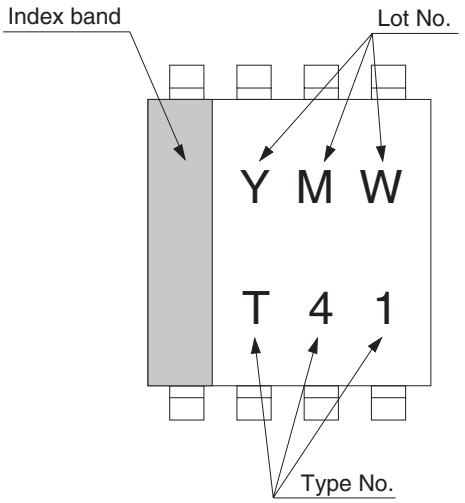
Hitachi semiconductor

Outline and Article Indication

• HD74LV2GT241A



SSOP–8



Y : Year code
(the last digit of year)
M : Month code
W : Week code

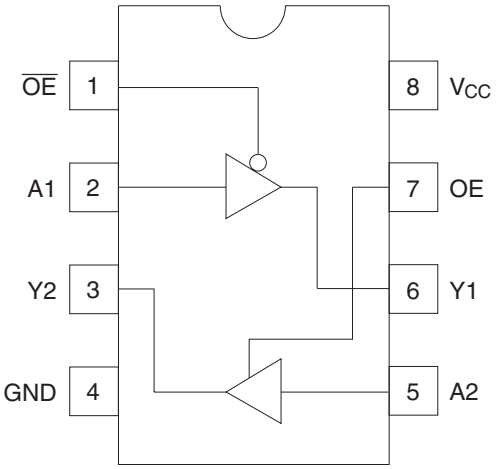
Function Table

Inputs		Output Y
$\overline{OE}$	A	
L	L	L
L	H	H
H	X	Z

Inputs		Output Y
OE	A	
H	L	L
H	H	H
L	X	Z

H : High level
L : Low level
X : Immaterial
Z : High impedance

Pin Arrangement



(Top view)

Absolute Maximum Ratings

Item	Symbol	Ratings	Unit	Test Conditions
Supply voltage range	V_{CC}	–0.5 to 7.0	V	
Input voltage range [*1]	V_I	–0.5 to 7.0	V	
Output voltage range [*1, 2]	V_O	–0.5 to V_{CC} + 0.5	V	Output : H or L
		–0.5 to 7.0		V_{CC} : OFF or output : Z
Input clamp current	I_{IK}	–20	mA	$V_I < 0$
Output clamp current	I_{OK}	±50	mA	$V_O < 0$ or $V_O > V_{CC}$
Continuous output current	I_O	±25	mA	V_O = 0 to V_{CC}
Continuous current through V_{CC} or GND	I_{CC} or I_{GND}	±50	mA	
Maximum power dissipation at Ta = 25°C (in still air) [*3]	P_T	200	mW	
Storage temperature	Tstg	–65 to 150	°C	

Notes: The absolute maximum ratings are values which must not individually be exceeded, and furthermore no two of which may be realized at the same time.

1. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This value is limited to 5.5 V maximum.
3. The maximum package power dissipation was calculated using a junction temperature of 150°C.

Recommended Operating Conditions

Item	Symbol	Ratings	Unit	Test Conditions
Supply voltage	V_{CC}	4.5 to 5.5	V	
Input voltage	V_{IN}	0 to 5.5	V	
Output voltage	V_{OUT}	0 to V_{CC}	V	
		0 to 5.5		Output : Z
Operating temperature	T_{opr}	–40 to +85	°C	
Input rise / fall time	t_r, t_f	0 to 20 (V_{CC} = 4.5 to 5.5 V)	ns	

Electrical Characteristics

- Ta = –40 to 85°C

Item	Symbol	V_{CC} (V) *	Min	Typ	Max	Unit	Test condition
Input voltage	V_{IH}	4.5 to 5.5	2.0	—	—	V	
	V_{IL}	4.5 to 5.5	—	—	0.8		
Hysteresis voltage	V_H	5.0	—	0.15	—	V	$V_T^+ - V_T^-$
Output voltage	V_{OH}	Min to Max	V_{CC}–0.1	—	—	V	I_{OH} = –50 µA
		4.5	3.8	—	—		I_{OH} = –12 mA
	V_{OL}	Min to Max	—	—	0.1		I_{OL} = 50 µA
		4.5	—	—	0.55		I_{OL} = 12 mA
Input current	I_{IN}	0 to 5.5	—	—	±1	µA	V_{IN} = 5.5 V or GND
Off state output current	I_{OZ}	Min to Max	—	—	±5	µA	V_O = 5.5 V or GND
Quiescent supply current	I_{CC}	5.5	—	—	10	µA	V_{IN} = V_{CC} or GND, I_O = 0
	ΔI_{CC}	5.5	—	—	1.5	mA	One input V_{IN} = 3.4 V, other input V_{CC} or GND
Output leakage current	I_{OFF}	0	—	—	5	µA	V_O = 5.5 V
Input capacitance	C_{IN}	5.0	—	3.0	—	pF	V_{IN} = V_{CC} or GND

Note: For conditions shown as Min or Max, use the appropriate values under recommended operating conditions.

Switching Characteristics

- V_{CC} = 5.0 ± 0.5 V

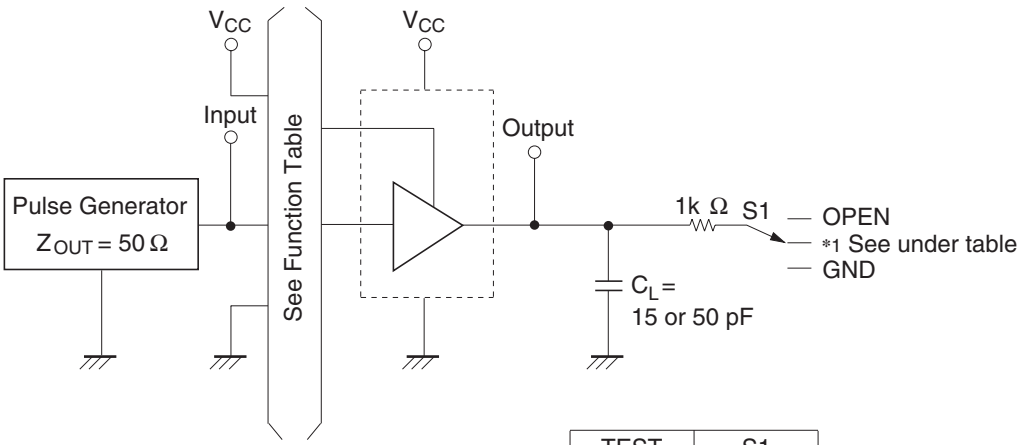
Item	Symbol	T_a = 25°C			T_a = –40 to 85°C		Unit	Test Conditions	FROM (Input)	TO (Output)
		Min	Typ	Max	Min	Max				
Propagation delay time	t_{PLH}	—	3.4	5.5	1.0	6.5	ns	C_L = 15 pF	A	Y
	t_{PHL}	—	4.3	7.5	1.0	8.5		C_L = 50 pF		
Enable time	t_{ZH}	—	3.4	5.1	1.0	6.0	ns	C_L = 15 pF	$\overline{OE}$ or OE	Y
	t_{ZL}	—	4.4	7.1	1.0	8.0		C_L = 50 pF		
Disable time	t_{HZ}	—	3.2	6.8	1.0	8.0	ns	C_L = 15 pF	$\overline{OE}$ or OE	Y
	t_{LZ}	—	4.0	8.8	1.0	10.0		C_L = 50 pF		

Operating Characteristics

- C_L = 50 pF

Item	Symbol	V_{CC} (V)	T_a = 25°C			Unit	Test Conditions
			Min	Typ	Max		
Power dissipation capacitance	C_{PD}	5.0	—	11.5	—	pF	f = 10 MHz

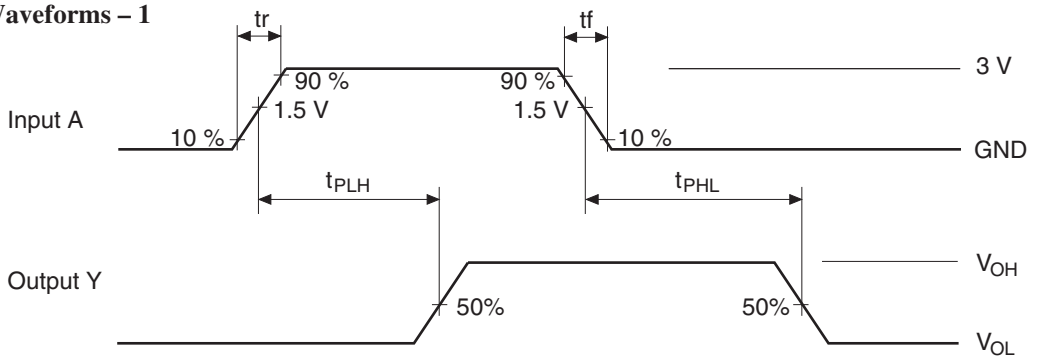
Test Circuit



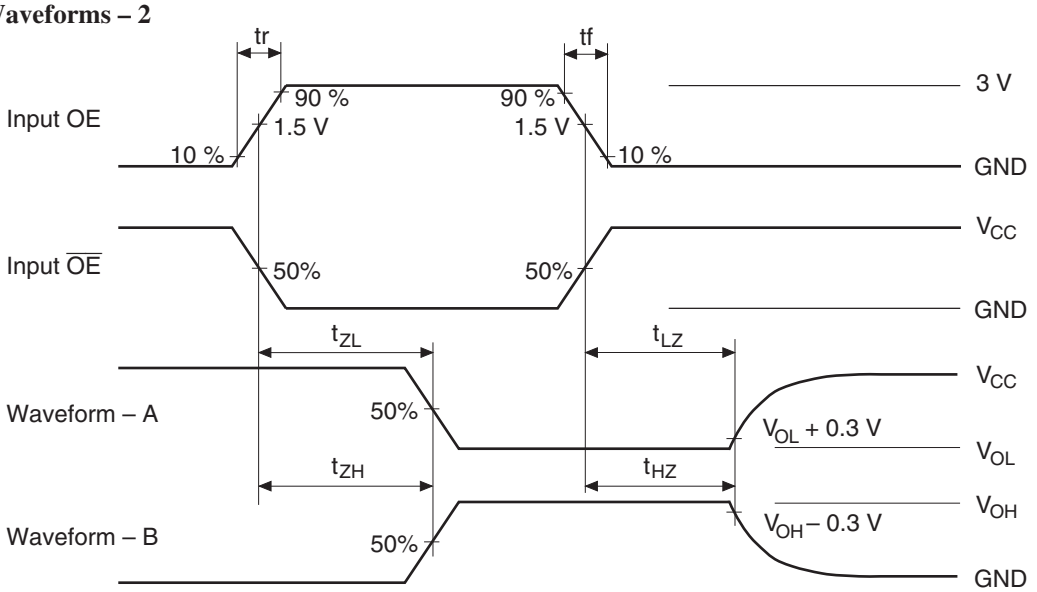
TEST	S1
t_{PLH} / t_{PHL}	OPEN
t_{ZH} / t_{HZ}	GND
t_{ZL} / t_{LZ}	V_{CC}

Note: 1. C_L includes probe and jig capacitance.

• **Waveforms – 1**



• **Waveforms – 2**

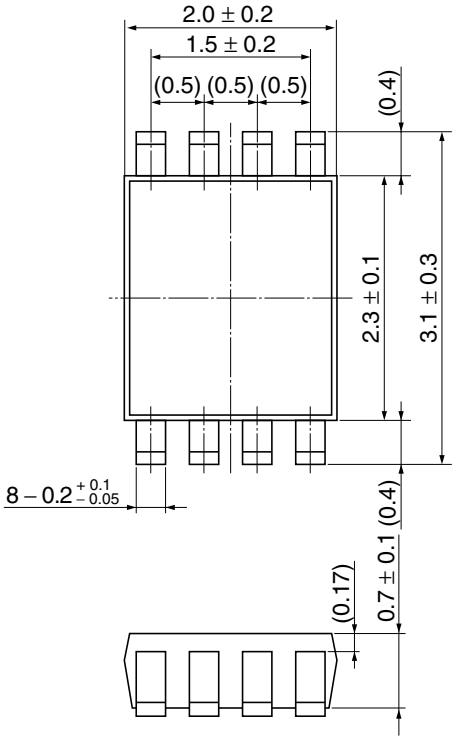


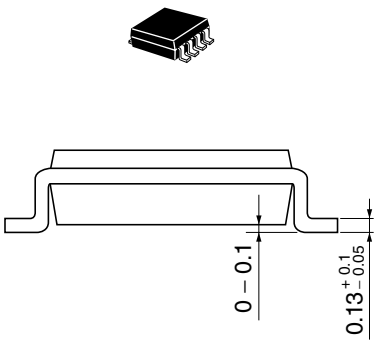
Notes: 1. Input waveform : PRR ≤ 1 MHz, Zo = 50 Ω, t_r ≤ 3 ns, t_f ≤ 3 ns.
2. Waveform – A is for an output with internal conditions such that the output is low except when disabled by the output control.
3. Waveform – B is for an output with internal conditions such that the output is high except when disabled by the output control.
4. The output are measured one at a time with one transition per measurement.

Package Dimensions

As of July, 2001

Unit: mm





Hitachi Code	TTP-8DB
JEDEC	—
JEITA	—
Mass (reference value)	0.010 g

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