1 PRODUCT OVERVIEW

KS88-SERIES MICROCONTROLLERS

Samsung's KS88 series of 8-bit single-chip CMOS microcontrollers offers a fast and efficient CPU with a wide range of integrated peripheral, in various mask-programmable ROM sizes. Among its major CPU features are:

— Efficient register-oriented architecture
— Selectable CPU clock sources
— Idle and Stop power-down mode release by interrupt
— Built-in basic timer with watchdog function

The sophisticated interrupt structure recognizes up to eight interrupt levels. Each level can have one or more interrupt sources and vectors. Fast interrupt processing (within a minimum of six CPU clocks) can be assigned to specific interrupt levels.

KS88C0416/C0424 MICROCONTROLLER

The KS88C0416/C0424 single-chip CMOS microcontrollers are fabricated using a highly advanced CMOS process, based on Samsung' s newest CPU architecture.

The KS88C0416/C0424 are microcontrollers containing a 16/24-Kbyte mask-programmable ROM. The KS88P0416/P0424 are microcontroller containing a 16/24-Kbyte one-time-programmable EPROM.

Using a proven modular design approach, Samsung engineers have successfully developed the KS88C0416/C0424 by integrating the following peripheral modules with the powerful SAM87 core:

— Four programmable I/O ports, including three 8-bit ports and one 2-bit port, for a total of 26 pins.
— Twelve bit-programmable pins for external interrupts.
— One 8-bit basic timer for oscillation stabilization and watchdog functions (system reset).
— One 8-bit timer/counter and one 16-bit timer/counter with selectable operating modes.
— One 8-bit counter with auto-reload function and one-shot or repeat control.

The KS88C0416/C0424 are versatile general-purpose microcontrollers especially suitable for use as a unified remote transmitter controller.

OTP

The KS88P0416/P0424 is an OTP (One Time Programmable) version of the KS88C0416/C0424 microcontroller. The KS88P0416/P0424 microcontroller has an on-chip 16/24-Kbyte one-time-programmable EPROM instead of a masked ROM. The KS88P0416/P0424 is comparable to the KS88C0416/C0424, both in function and in pin configuration.

FEATURES

CPU

- SAM87 CPU core

Memory

- 16-Kbyte internal program memory (ROM): KS88C0416
- 24-Kbyte internal program memory (ROM): KS88C0424
- Data memory: 317-byte internal register file

Instruction Set

- 78 instructions
- IDLE and STOP instructions added for power-down modes

Instruction Execution Time

- 750 ns at 8 MHz f_{OSC} (minimum)

Interrupts

- Six interrupt levels and 18 interrupt sources
- 15 vectors (14 sources have a dedicated vector address and four sources share a single vector)
- Fast interrupt processing feature (for one selected interrupt level)

I/O Ports

- Three 8-bit I/O ports (P0–P2) and one 2-bit port (P3) for a total of 26 bit-programmable pins
- Twelve input pins for external interrupts

Timers and Timer/Counters

- One programmable 8-bit basic timer (BT) for oscillation stabilization control or watchdog timer (software reset) function
- One 8-bit timer/counter (Timer 0) with three operating modes; Interval, Capture, and PWM
- One 16-bit timer/counter (Timer 1) with two operating modes; Interval and Capture

Carrier Frequency Generator

- One 8-bit counter with auto-reload function and one-shot or repeat control (Counter A)

Stop Error Detection and Recovery (SED and R)

- Special logic in relation to P0 and P1 to prevent abnormal-stop status
- Releasing stop mode by level switching detection in P0 and P1

Back-up mode by reset input

- When reset pin is low, the chip enters back-up mode to reduce current

Operating Temperature Range

- – 40°C to + 85°C

Operating Voltage Range

- 2.0 V to 5.5 V at 4 MHz f_{OSC}
- 2.2 V to 5.5 V at 8 MHz f_{OSC}

Package Type

- 32-pin SOP
- 32-pin SDIP
- 40-pin DIP (KS88C0424 only)

BLOCK DIAGRAM

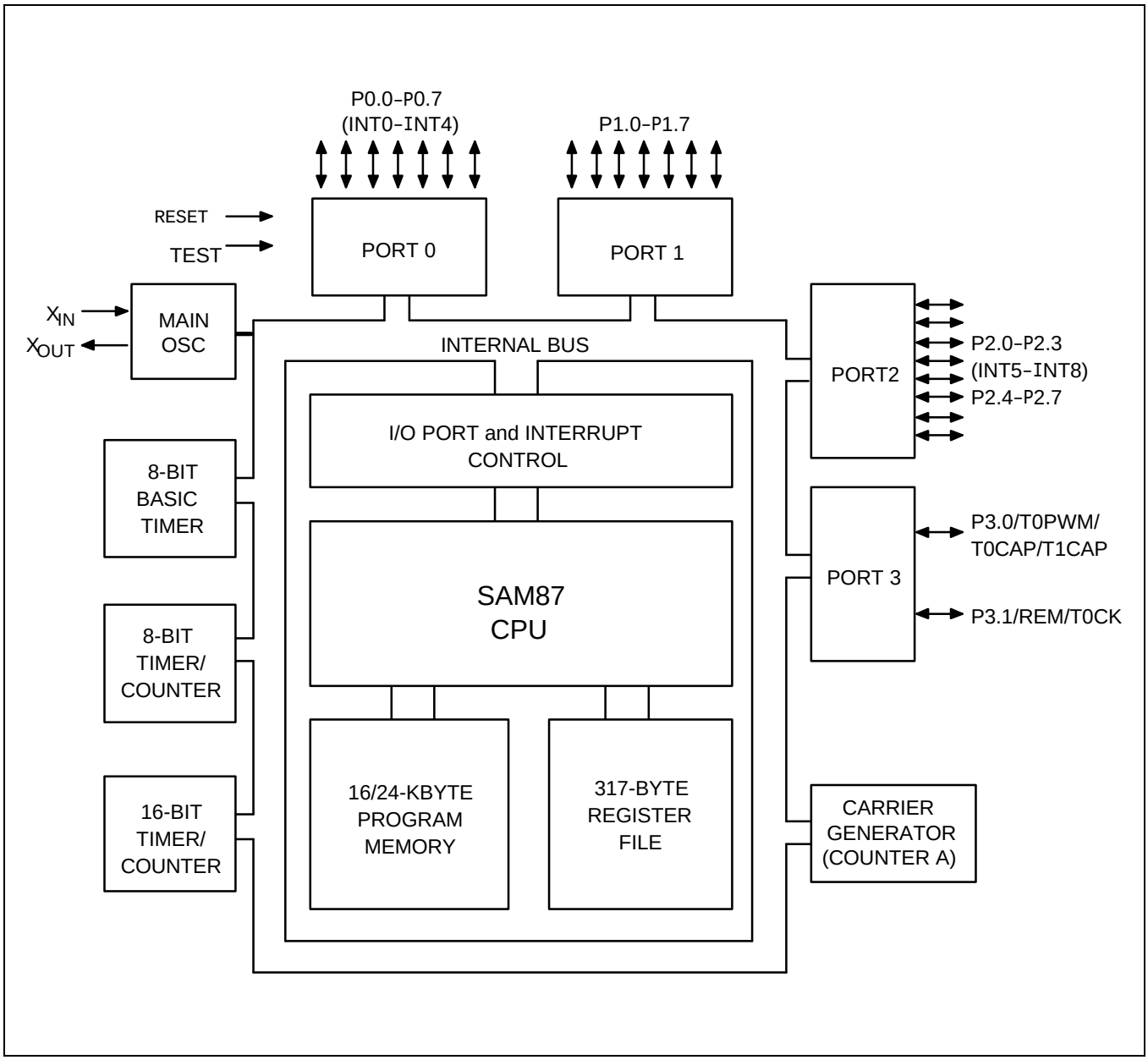

Figure 1-1. Block Diagram

PIN ASSIGNMENTS

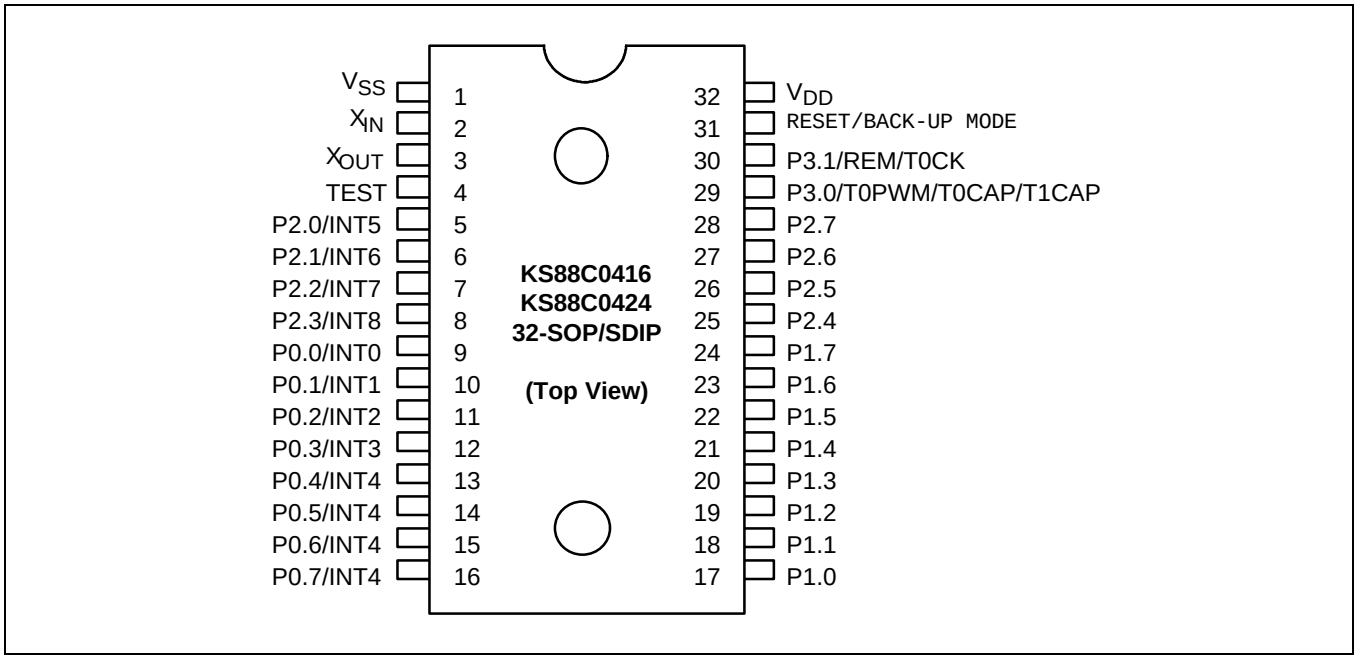

Figure 1-2. Pin Assignment (32-Pin SOP/SDIP Package)

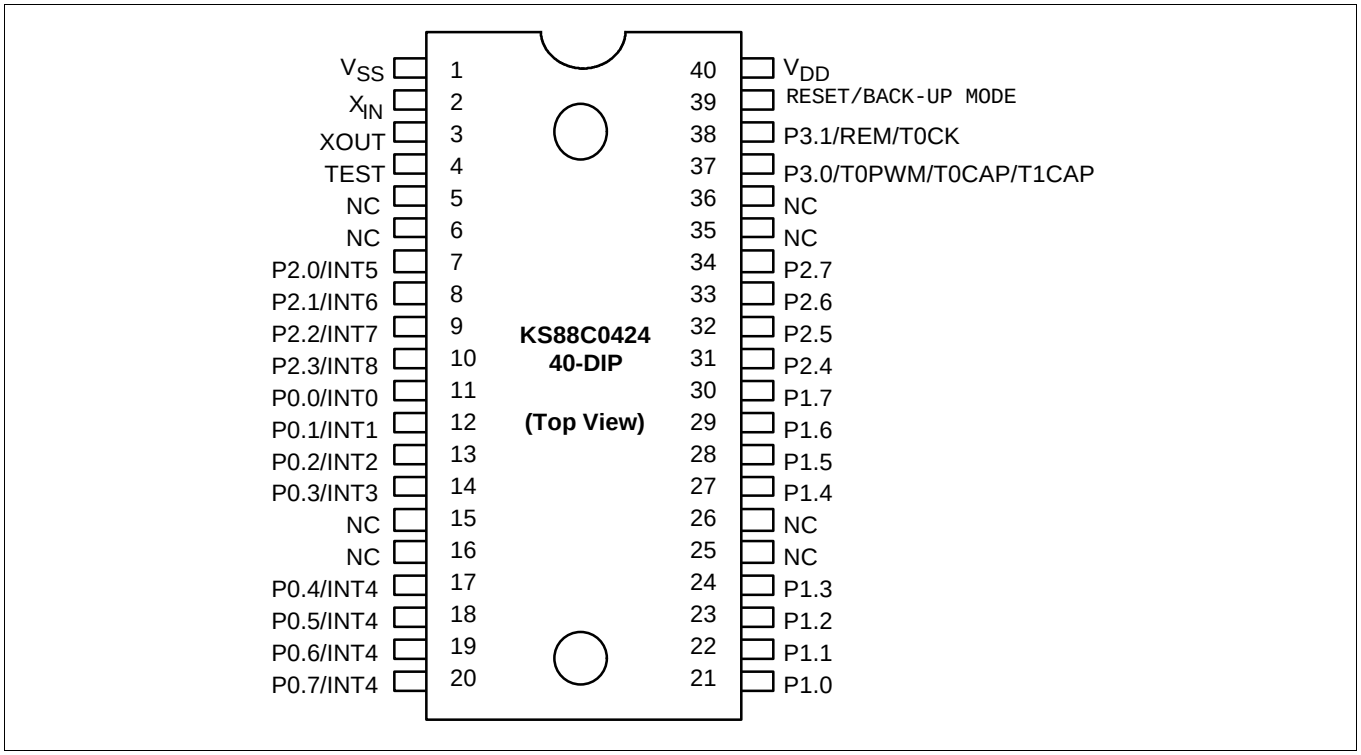

Figure 1-3. Pin Assignment (40-Pin DIP Package)

PIN DESCRIPTIONS

Table 1-1. Pin Descriptions

Pin Names	Pin Type	Pin Description	Circuit Type	Pin No. (32-pin)	Pin No. (40-pin)	Shared Functions
P0.0–P0.7	I/O	I/O port with bit-programmable pins. Configurable to input or push-pull output mode. Pull-up resistors are assignable by software. Pins can be assigned individually as external interrupt inputs with noise filters, interrupt enable/disable, and interrupt pending control.	1	9–16	11–14, 17–20	INT0–INT4
P1.0–P1.7	I/O	I/O port with bit-programmable pins. Configurable to C-MOS input mode or output mode. Pin circuits are either push-pull or n-channel open-drain type. Pull-up resistors are assignable by software.	2	17–24	21–24, 27–30	–
P2.0–P2.3 P2.4–P2.7	I/O	General-purpose I/O port with bit-programmable pins. Configurable to C-MOS input mode, push-pull output mode, or n-channel open-drain output mode. Pull-up resistors are assignable by software. Lower nibble pins, P2.3–P2.0, can be assigned as external interrupt inputs with noise filters, interrupt enable/disable, and interrupt pending control.	3 4	5–8, 25–28	7–10, 31–34	INT5–INT8 –
P3.0 P3.1	I/O	2-bit I/O port with bit-programmable pins. Configurable to C-MOS input mode, push-pull output mode, or n-channel open-drain output mode. Pull-up resistors are assignable by software. The two port 3 pins have high current drive capability.	5	29 30	37 38	T0PWM/ T0CAP/ T1CAP/ REM/T0CK
X_{IN}, X_{OUT}	–	System clock input and output pins	–	2, 3	2, 3	–
RESET/ BACK-UP MODE	I	System reset signal input pin and back-up mode input pin. The pin circuit is a C-MOS input.	6	31	39	–
TEST	I	Test signal input pin (for factory use only; must be connected to V_{SS}).	–	4	4	–
V_{DD}	–	Power supply input pin	–	32	40	–
V_{SS}	–	Ground pin	–	1	1	–