

LS3954 MONOLITHIC DUAL N-CHANNEL JFET



The LS3954 is a Low Noise, Low Drift, Monolithic Dual N-Channel JFET

The LS3954 family are matched JFET pairs for differential amplifiers. The LS3954 family of general purpose JFETs is characterized for low and medium frequency differential amplifiers requiring low offset voltage, drift, noise and capacitance

The LS3954 family exhibits low capacitance - 6pF max and a spot noise figure of - 0.5dB max. The part offers a superior tracking ability.

The 8 Pin P-DIP and 8 Pin SOIC provide ease of manufacturing, and the symmetrical pinout prevents improper orientation.

(See Packaging Information).

LS3954 Applications:

- Wideband Differential Amps
- High Input Impedance Amplifiers

FEATURES								
LOW DRIFT		$ \Delta V_{GS1-2}/\Delta T = 5\mu V/^{\circ}C$ max.						
LOW LEAKAG	GE	$I_G = 20pA TYP.$						
LOW NOISE		$e_n = 10 \text{nV/VHz TYP}.$						
ABSOLUTE MAXIMUM RATINGS								
@ 25°C (unless otherwise noted)								
Maximum Temperatures								
Storage Tem	perature	-65°C to +200°C						
Operating Junction Temperature			+150°C					
Maximum Voltage and Current for Each Transistor – Note 1								
-V _{GSS}	Gate Voltage to Drain or So	60V						
-V _{DSO}	Drain to Source Voltage	60V						
-I _{G(f)}	Gate Forward Current	50mA						
Maximum Power Dissipation								
Device Dissipation @ Free Air – Total 400mW @ 25°C								

MATCHING CHARACTERISTICS @ 25°C UNLESS OTHERWISE NOTED									
	SYMBOL CHARACTERISTICS		VALUE	UNITS	CONDITIONS				
	V _{GS1-2} / T max. DRIFT VS.		10	μV/°C	V _{DG} =20V, I _D =200μA				
		TEMPERATURE			T _A =-55°C to +125°C				
	V _{GS1-2} max.	OFFSET VOLTAGE	5	mV	V _{DG} =20V, I _D =200μA				

ELECTRICAL CHARACTERISTICS @ 25°C (unless otherwise noted)

SYMBOL	CHARACTERISTICS	MIN.	TYP.	MAX.	UNITS	CONDITIONS
BV _{GSS}	Breakdown Voltage	60			V	$V_{DS} = 0$ $I_{D} = 1 \mu A$
BV _{GGO}	Gate-To-Gate Breakdown	60			V	$I_{G}=1$ nA $I_{D}=0$ $I_{S}=0$
	TRANSCONDUCTANCE					
Y_{fSS}	Full Conduction	1000	2000	3000	μmho	V_{DG} = 20V V_{GS} = 0V f = 1kHz
Y _{fS}	Typical Operation	500	700	10 00	μmho	V _{DG} = 20V I _D = 200μA
Y _{FS1-2} / Y _{FS}	M <mark>is</mark> match		0.6	3	%	
I _{DSS}	DRAIN CURRENT Full Conduction	0.5	2	5	mA	V _{DG} = 20V
$ I_{DSS1-2}/I_{DSS} $	Mismatch at Full Conduction		1	5	%	
V _{GS} (off) or V _p	<u>GATE VOLTAGE</u> Pinchoff voltage	1	2	4.5	V	V _{DS} = 20V
V _{GS} (on)	Operating Range	0.5		4	V	V _{DS} =20V
	GATE CURRENT					
-I _G	Operating		20	50	рА	$V_{DG} = 20V$ $I_{D} = 200 \mu A$
-I _G	High Temperature			50	nA	T _A = +125°C
-I _G	Reduced V _{DG}		5		рА	V_{DG} = 10V I_D = 200 μ A
-I _{GSS}	At Full Conduction			100	рА	$V_{DG} = 20V$ $V_{DS} = 0$
	OUTPUT CONDUCTANCE					
Y _{OSS}	Full Conduction			5	μmho	$V_{DG} = 20V$ $V_{GS} = 0V$
Y _{OS}	Operating		0.1	1	μmho	V _{DG} = 20V I _D = 200μA
Y _{OS1-2}	Differential		0.01	0.1	μmho	
	COMMON MODE REJECTION					
CMR	-20 log V _{GS1-2} / V _{DS}		100		dB	$\Delta V_{DS} = 10 \text{ to } 20V \qquad I_{D} = 200 \mu A$
CMR	-20 log V _{GS1-2} / V _{DS}		75		dB	$\Delta V_{DS} = 5 \text{ to } 10V \qquad I_D = 200 \mu A$
	<u>NOISE</u>					V_{DS} = 20V V_{GS} = 0V R_{G} = 10M Ω
NF	Figure			0.5	dB	f= 100Hz NBW= 6Hz
e _n	Voltage			15	nV/√Hz	V _{DS} =20V I _D =200μA f=10Hz NBW=1Hz
	<u>CAPACITANCE</u>					_
C _{ISS}	Input			6	pF	V_{DS} = 20V V_{GS} = 0V f= 1MHz
C _{RSS}	Reverse Transfer			2	pF	
C_{DD}	Drain-to-Drain		0.1		pF	$V_{DG} = 20V$ $I_{D} = 200 \mu A$

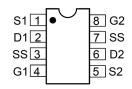
Note 1 – These ratings are limiting values above which the serviceability of any semiconductor may be impaired

Available Packages:

LS3954 in PDIP / SOIC LS3954 available as bare die

Please contact Micross for full package and die dimensions

PDIP / SOIC (Top View)



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