Elektronische Bauelemente

SDN520C

N-Ch: 4.5 A, 20 V, $R_{DS(ON)}$ 58 mΩ
P-Ch: -4.5 A, -20 V, $R_{DS(ON)}$ 112 mΩ
N & P-Channel Enhancement Mode MOSFET

RoHS Compliant Product
A suffix of "-C" specifies halogen and lead-free

DESCRIPTION

These miniature surface mount MOSFETs utilize a high cell Density trench process to provide low $R_{DS(on)}$ and to assures minimal power loss and heat dissipation.

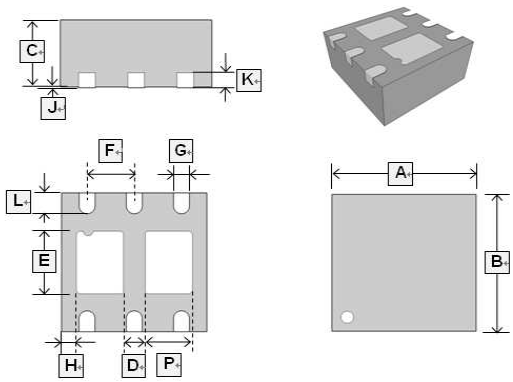
FEATURES

- Low $R_{DS(on)}$ provides higher efficiency and extends battery life.
- Low thermal impedance copper leadframe DFN2X2_6L saves board space.
- Fast switching speed.
- High performance trench technology.

APPLICATION

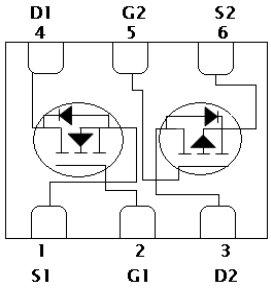
DC-DC converters and power management in portable and battery-powered products such as computers, printers, PCMCIA cards, cellular and cordless telephones.

DFN2x2-6L



REF.	Millimeter			REF.	Millimeter		
	Min.	Typ.	Max.		Min.	Typ.	Max.
A	2.00 BSC.			G	0.23	0.30	0.38
B	2.00 BSC.			H	0.65BSC		
C	0.675	0.75	0.80	J	0	-	0.05
D	0.25	0.30	0.35	K	0.15	0.20	0.25
E	0.81	0.86	0.91	L	0.25	0.30	0.35
F	0.65BSC			P	0.60	0.65	0.70

TOP VIEW



ABSOLUTE MAXIMUM RATINGS(T_A = 25°C unless otherwise specified)

Parameter		Symbol	Ratings		Unit
			N-Channel	P-Channel	
Drain-Source Voltage		V_{DS}	20	-20	V
Gate-Source Voltage		V_{GS}	±8	±8	V
Continuous Drain Current [1]	TA=25℃	I_D	4.5	-4.5	A
	TA=70℃		4.5	-4.5	
Pulsed Drain Current [2]		I_{DM}	8	-8	A
Continuous Source Current (Diode Conduction) [1]		I_S	4.5	-4.5	A
Power Dissipation [1]	TA=25℃	P_D	6.5		W
	TA=70℃		5		
Operating Junction and Storage Temperature Range		T_J, Tstg	-55 ~ +150		℃

Thermal Resistance Rating

Parameter		Symbol	Typ	Max	Unit
Maximum Junction to Ambient [1]	t ≦ 5 sec	$R_{\theta JA}$	52	65	℃ / W
	Steady State		12.5	16	

Notes:
1. Surface Mounted on 1" x 1" FR4 Board.
2. Pulse width limited by maximum junction temperature.

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N & P-Channel Enhancement Mode MOSFET

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise specified)

Parameter		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Gate-Threshold Voltage	N-Ch	$V_{GS(th)}$	1	-	-	V	V_{DS}=V_{GS}, I_D=250uA
	P-Ch		-1	-	-		V_{DS}=V_{GS}, I_D= -250uA
Gate-Body Leakage Current	N-Ch	I_{GSS}	-	-	100	uA	V_{DS}= 0 , V_{GS}= 8 V
	P-Ch		-	-	-100		V_{DS}= 0 , V_{GS}= -8 V
Zero Gate Voltage Drain Current	N-Ch	I_{DSS}	-	-	1	uA	V_{DS}=16 V, V_{GS}=0
	P-Ch		-	-	-1		V_{DS}=-16V, V_{GS}=0
	N-Ch		-	-	10		V_{DS}=16V, V_{GS}=0 , T_J=55℃
	P-Ch		-	-	-10		V_{DS}= -16V, V_{GS}=0 , T_J=55℃
On-State Drain Current [1]	N-Ch	$I_{D(on)}$	5	-	-	A	V_{DS} = 5V, V_{GS}=4.5 V
	P-Ch		-5	-	-		V_{DS} = -5V, V_{GS}= -4.5 V
Drain-Source On-Resistance [1]	N-Ch	$R_{DS(ON)}$	-	-	58	mΩ	V_{GS}=4.5V, I_D= 1A
	P-Ch		-	-	112		V_{GS}=-4.5V, I_D= 1A
	N-Ch		-	-	82		V_{GS}=2.5V, I_D= A
	P-Ch		-	-	172		V_{GS}=-2.5V, I_D= -1A
Forward Transconductance [1]	N-Ch	g_{fs}	-	10	-	S	V_{DS}= 5V, I_D= 1A
	P-Ch		-	5	-		V_{DS}= -5V, I_D= 11A
Diode Forward Voltage [1]	N-Ch	V_{SD}	-	0.80	-	S	I_S= 1.05A, V_{GS}= 0
	P-Ch		-	-0.83	-		I_S= -1.05A, V_{GS}= 0
Dynamic [2]							
Total Gate Charge	N-Ch	Q_g	-	7.5	-	nC	N-Channel V_{DS}=15V, V_{GS}= 4.5V, I_D= 2.7A P-Channel V_{DS}= -15V, V_{GS}= -4.5V, I_D= -3.1A
	P-Ch		-	3.8	-		
Gate-Source Charge	N-Ch	Q_{gs}	-	0.6	-		
	P-Ch		-	0.6	-		
Gate-Drain Charge	N-Ch	Q_{gd}	-	1.0	-		
	P-Ch		-	1.5	-		
Turn-on Delay Time	N-Ch	$T_{d(on)}$	-	5	-	nS	N-Channel V_{DD}= 15V, R_{GEN}= 15Ω, V_{GS}= 4.5V, I_D= 1A P-Channel V_{DD}= -15V, R_{GEN}= 15Ω V_{GS}= -4.5V, I_D= -1A
	P-Ch		-	5	-		
Rise Time	N-Ch	T_r	-	12	-		
	P-Ch		-	15	-		
Turn-off Delay Time	N-Ch	$T_{d(off)}$	-	13	-		
	P-Ch		-	20	-		
Fall Time	N-Ch	T_f	-	7	-		
	P-Ch		-	20	-		

Notes:
1. Pulse test: PW <= 300us duty cycle <= 2%.
2. Guaranteed by design, not subject to production testing.