

M5M44400BJ,L,TP,RT-5,-6,-7,-8,-5S,-6S,-7S,-8S

FAST PAGE MODE 4194304-BIT(1048576-WORD BY 4-BIT)DYNAMIC RAM

DESCRIPTION

This is a family of 1048576-word by 4-bit dynamic RAMS, fabricated with the high performance CMOS process, and is ideal for large-capacity memory systems where high speed, low power dissipation, and low costs are essential.

The use of quadruple-layer polysilicon process combined with silicide technology and a single-transistor dynamic storage stacked capacitor cell provide high circuit density at reduced costs.

Multiplexed address inputs permit both a reduction in pins and an increase in system densities.

Self or extended refresh current is small enough for battery back-up application.

FEATURES

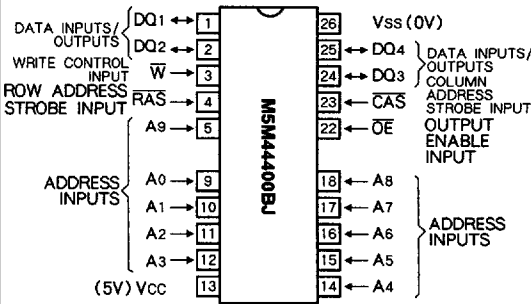
Type name	RAS access time (max. ns)	CAS access time (max. ns)	Address access (max. ns)
M5M44400BXX-5,-5S	50	13	25
M5M44400BXX-6,-6S	60	15	30
M5M44400BXX-7,-7S	70	20	35
M5M44400BXX-8,-8S	80	20	40

Type name	OE access time (max. ns)	Cycle time (min. ns)	Power dissipation (typ. mW)
M5M44400BXX-5,-5S	13	90	500
M5M44400BXX-6,-6S	15	110	400
M5M44400BXX-7,-7S	20	130	350
M5M44400BXX-8,-8S	20	150	300

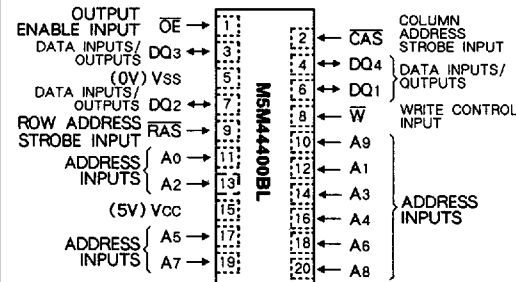
XX = J, L, TP, RT

- Standard 26pin SOJ, 20pin ZIP, 26pin TSOP (II)
 - Single 5V ± 10% supply
 - Low stand-by power dissipation
 - CMOS Input level.....5.5mW (max)
 - CMOS Input level.....0.55mW (max)*
 - Low operating power dissipation
 - M5M44400BXX-5,-5S 687.5mW (max)
 - M5M44400BXX-6,-6S 550.0mW (max)
 - M5M44400BXX-7,-7S 467.5mW (max)
 - M5M44400BXX-8,-8S 412.5mW (max)
 - Self refresh capability*
 - Self refresh current 150 μA (max)
 - Extended refresh capability
 - Extended refresh current 150 μA (max)
 - Fast-page mode(1024-bit random access), Read-modify-write, RAS-only refresh, CAS before RAS refresh, Hidden refresh, CBR Self Refresh (-5S, -6S, -7S, -8S) capabilities.
 - Early write mode and OE to control output buffer impedance
 - All inputs, output TTL compatible and low capacitance
 - 1024 refresh cycles every 16.4ms(A₀~A₉)
 - 1024 refresh cycles every 128ms(A₀~A₉)*
 - 4-bit parallel test mode capability
- * : Applicable to self refresh version (M5M44400BJ, L, TP, RT-5S,-6S, -7S, -8S : option) only.

PIN CONFIGURATION (TIO WIVEW)



Outline 26P0J (300mil SOJ)



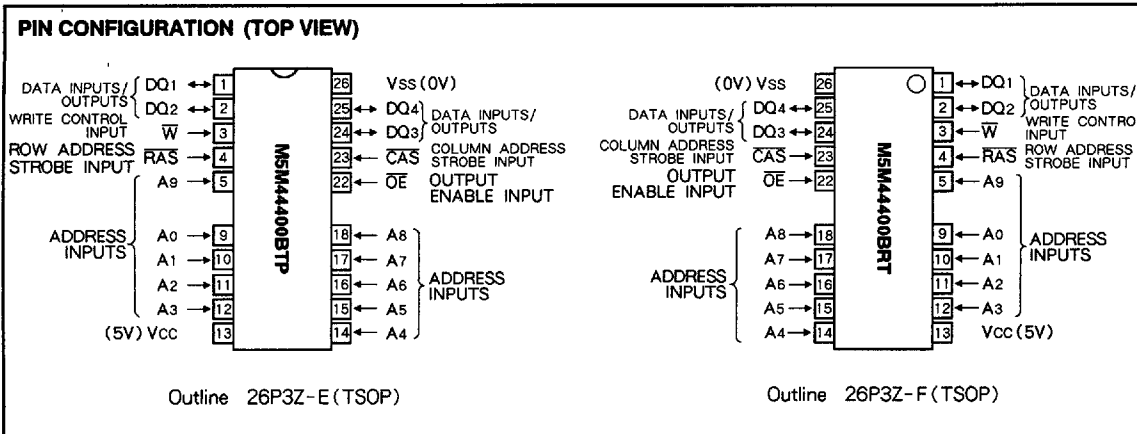
Outline 20P5L-B (ZIP)

APPLICATION

Main memory unit for computers, Microcomputer memory, Refresh memory for CRT

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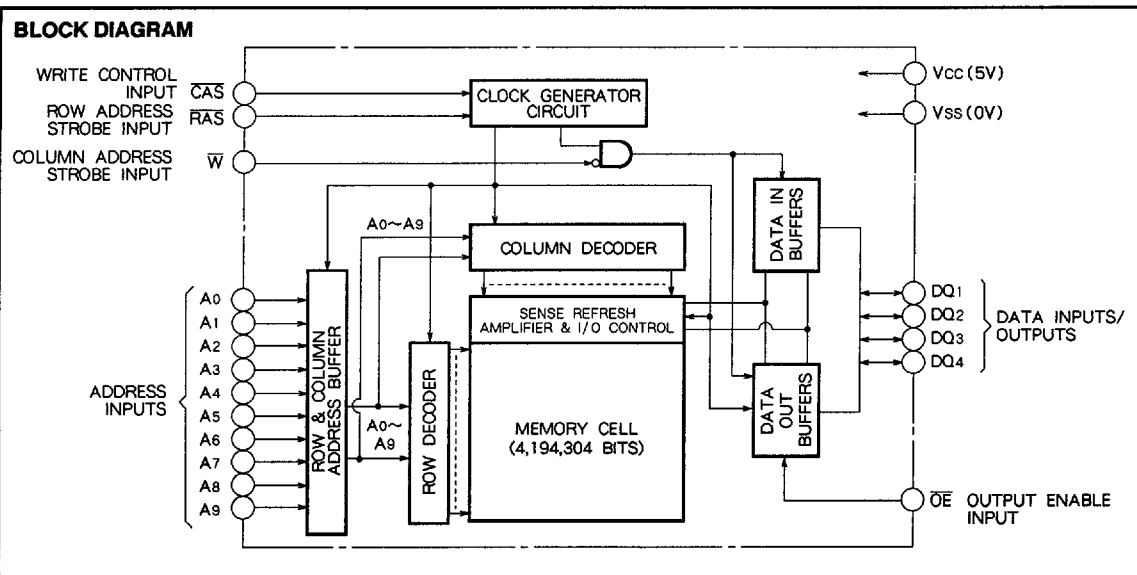
FUNCTION

The M5M44400BJ,L,TP,RT provide, in addition to normal read, write, and read-modify-write operations, a number of other functions, e.g., fast page mode, $\overline{\text{RAS}}$ -only refresh, and delayed-write. The input conditions for each are shown in Table 1.

Table 1. Input condition for each mode

Operation	Inputs						Input/Output		Refresh	Remark
	$\overline{\text{RAS}}$	$\overline{\text{CAS}}$	W	$\overline{\text{OE}}$	Row address	Column address	Input D	Output Q		
Read	ACT	ACT	NAC	ACT	APD	APD	OPN	VLD	YES	Fast page mode identical
Write (Early write)	ACT	ACT	ACT	DNC	APD	APD	VLD	OPN	YES	
Write (Delayed write)	ACT	ACT	ACT	DNC	APD	APD	VLD	IVD	YES	
Read-modify-write	ACT	ACT	ACT	ACT	APD	APD	VLD	VLD	YES	
$\overline{\text{RAS}}$ -only refresh	ACT	NAC	DNC	DNC	APD	DNC	DNC	OPN	YES	
Hidden refresh	ACT	ACT	DNC	ACT	APD	DNC	OPN	VLD	YES	
$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh (Extended*)	ACT	ACT	NAC	DNC	DNC	DNC	DNC	OPN	YES	
Self Refresh*	ACT	ACT	NAC	DNC	DNC	DNC	DNC	OPN	YES	
Stand-by	NAC	DNC	DNC	DNC	DNC	DNC	DNC	OPN	NO	

Notes. ACT : active, NAC : nonactive, DNC : don't care, VLD : valid, IVD : invalid, APD : applied, OPN : open



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ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V _{CC}	Supply voltage	With respect to V _{SS}	- 1~7	V
V _I	Input voltage		- 1~7	V
V _O	Output voltage		- 1~7	V
I _O	Output current	T _a = 25°C	50	mA
P _d	Power dissipation		1000	mW
T _{opr}	Operating temperature		0~70	°C
T _{stg}	Storage temperature		- 65~150	°C

RECOMMENDED OPERATING CONDITIONS (T_a = 0~70°C, unless otherwise noted) (Note 1)

Symbol	Parameter	Limits			Unit
		Min	Nom	Max	
V _{CC}	Supply voltage	4.5	5	5.5	V
V _{SS}	Supply voltage	0	0	0	V
V _{IH}	High-level input voltage, all inputs	2.4		6.5	V
V _{IL}	Low-level input voltage	DQ ₁ ~DQ ₄	- 1.0	0.8	V
		Others	- 2.0	0.8	

Note 1. All voltage values are with respect to V_{SS}.

ELECTRICAL CHARACTERISTICS (T_a = 0~70°C, V_{CC} = 5V ± 10%, V_{SS} = 0V, unless otherwise noted) (Note 2)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
V _{OH}	High-level output voltage	I _{OH} = - 5mA	2.4		V _{CC}	V
V _{OL}	Low-level output voltage	I _{OL} = 4.2mA	0		0.4	V
I _{OZ}	Off-state output current	Q floating, 0V ≤ V _{OUT} ≤ 5.5V	- 10		10	μA
I _I	Input current	0V ≤ V _{IN} ≤ 6.5V, Other inputs pins=0V	- 10		10	μA
I _{CC1} (AV)	Average supply current from V _{CC} , operating (Note 3, 4, 5)	R _{AS} , C _{AS} cycling trc = twc = min. output open			125	mA
					100	
					85	
					75	
I _{CC2} (AV)	Supply current from V _{CC} , stand-by (Note 6)	R _{AS} = C _{AS} = V _{IH} , output open			2	mA
		R _{AS} = C _{AS} ≥ V _{CC} - 0.5 output open			1 0.1	
I _{CC3} (AV)	Average supply current from V _{CC} , refreshing (Note 3, 5)	R _{AS} cycling C _{AS} = V _{IH} , trc = min. output open			125	mA
					100	
					85	
					75	
I _{CC4} (AV)	Average supply current from V _{CC} , Fast-Page-Mode (Note 3, 4, 5)	R _{AS} = V _{IL} C _{AS} cycling trc = min, output open			125	mA
					100	
					85	
					75	
I _{CC6} (AV)	Average supply current from V _{CC} , C _{AS} before R _{AS} refresh mode (Note 3)	C _{AS} before R _{AS} refresh cycling, trc = min. output open			105	mA
					85	
					75	
					65	
I _{CC8} (AV)	Average supply current from V _{CC} Extended-Refresh cycle (Note 6)	Stand-by : R _{AS} ≥ V _{CC} - 0.2V C _{AS} ≥ V _{CC} - 0.2V or C _{AS} ≤ 0.2V C _{AS} before R _{AS} refresh : R _{AS} cycling C _{AS} ≤ 0.2V or C _{AS} before R _{AS} refresh cycling W ≤ 0.2V or ≥ V _{CC} - 0.2V OE ≤ 0.2V or ≥ V _{CC} - 0.2V A ₀ ~A ₉ ≤ 0.2V or ≥ V _{CC} - 0.2V DQ = open, trc = 125 μs t _{RAS} = t _{TRAS} min~1 μs			150	μA
I _{CC9} (AV)	Average supply current from V _{CC} Self-Refresh cycle (Note 6)	R _{AS} = C _{AS} ≤ 0.2V			150	μA

Note 2. Current flowing into an IC is positive, out is negative.

3. I_{CC1}(AV), I_{CC3}(AV) and I_{CC4}(AV) are dependent on cycle rate. Maximum current is measured at the fastest cycle rate.

4. I_{CC1}(AV) and I_{CC4}(AV) are dependent on output loading. Specified values are obtained with the output open.

5. Column Address can be changed once or less while R_{AS} = V_{IL} and C_{AS} = V_{IH}.

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CAPACITANCE (Ta = 0~70 °C, Vcc = 5V ± 10 %, Vss = 0V, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
Ci(A)	Input capacitance, address inputs	Vi = Vss			5	pF
					6	
Ci(CLK)	Input capacitance, clock inputs	f = 1MHz			7	pF
					7	
Ci/O	Input/Output capacitance, data ports	Vi = 25mVrms			7	pF
					7	

SWITCHING CHARACTERISTICS (Ta = 0~70 °C, Vcc = 5V ± 10 %, Vss = 0V, unless otherwise noted) (Notes 6, 13, 14)

Symbol	Parameter	Limits								Unit
		M5M44400B-5, -5S		M5M44400B-6, -6S		M5M44400B-7, -7S		M5M44400B-8, -8S		
		Min	Max	Min	Max	Min	Max	Min	Max	
tCAC	Access time from $\overline{\text{CAS}}$ (Note 7, 8)		13		15		20		20	ns
tRAC	Access time from $\overline{\text{RAS}}$ (Note 7, 9)		50		60		70		80	ns
tAA	Column Address access time (Note 7, 10)		25		30		35		40	ns
tCPA	Access time from $\overline{\text{CAS}}$ precharge (Note 7, 11)		30		35		40		45	ns
tOEA	Access time from $\overline{\text{OE}}$ (Note 7)		13		15		20		20	ns
tCLZ	Output low impedance from $\overline{\text{CAS}}$ low (Note 7)	5		5		5		5		ns
tOFF	Output disable time after $\overline{\text{CAS}}$ high (Note 12)	0	13	0	15	0	20	0	20	ns
tOEZ	Output disable time after $\overline{\text{OE}}$ high (Note 12)	0	13	0	15	0	20	0	20	ns

- Note 6. An initial pause of 500 μ s is required after power-up followed by a minimum of eight initialization cycles (any combination of cycles containing a $\overline{\text{RAS}}$ clock such as $\overline{\text{RAS}}$ -only refresh).
 Note the $\overline{\text{RAS}}$ may be cycled during the initial pause. And any 8 $\overline{\text{RAS}}$ or $\overline{\text{RAS}}/\overline{\text{CAS}}$ cycles are required after prolonged periods (greater than 16.4 ms) of $\overline{\text{RAS}}$ inactivity before proper device operation is achieved.
7. Measured with a load circuit equivalent to 2TTL loads and 100pF.
 8. Assumes that $t_{\text{RCD}} \geq t_{\text{RCD}}(\text{max})$ and $t_{\text{ASC}} \geq t_{\text{ASC}}(\text{max})$.
 9. Assumes that $t_{\text{RCD}} \leq t_{\text{RCD}}(\text{max})$ and $t_{\text{RAD}} \leq t_{\text{RAD}}(\text{max})$. If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} will increase by amount that t_{RCD} or t_{RAD} exceeds the value shown.
 10. Assumes that $t_{\text{RAD}} \geq t_{\text{RAD}}(\text{max})$ and $t_{\text{ASC}} \leq t_{\text{ASC}}(\text{max})$.
 11. Assumes that $t_{\text{CP}} \leq t_{\text{CP}}(\text{max})$ and $t_{\text{ASC}} \geq t_{\text{ASC}}(\text{max})$.
 12. $t_{\text{OFF}}(\text{max})$ and $t_{\text{OEZ}}(\text{max})$ defines the time at which the output achieves the high impedance state ($|I_{\text{OUT}}| \leq \pm 10 \mu\text{A}$) and is not reference to $V_{\text{OH}}(\text{min})$ or $V_{\text{OL}}(\text{max})$.

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TIMING REQUIREMENTS (For Read, Write, Read-Modify-Write, Refresh, and Fast Page Cycles)

(Ta = 0~70°C, Vcc = 5V ± 10%, Vss = 0V, unless otherwise noted) (Notes 13, 14)

Symbol	Parameter		Limits								Unit
			M5M44400B-5, -5S		M5M44400B-6, -6S		M5M44400B-7, -7S		M5M44400B-8, -8S		
			Min	Max	Min	Max	Min	Max	Min	Max	
tREF	Refresh cycle time	M5M44400B		16.4		16.4		16.4		16.4	ms
		M5M44400B(S)		128		128		128		128	
tRP	RAS high pulse width		30		40		50		60	ns	
tRCD	Delay time, RAS low to CAS low (Note 15)		18	37	20	45	20	50	20	60	ns
tCRP	Delay time, CAS high to RAS low		5		5		5		5	ns	
tRPC	Delay time, RAS high to CAS low		0		0		0		0	ns	
tCPN	CAS high pulse width		10		10		10		10	ns	
tRAD	Column address delay time from RAS low (Note 16)		13	25	15	30	15	35	15	40	ns
tASR	Row address setup time before RAS low		0		0		0		0	ns	
tASC	Column address setup time before CAS low (Note 17)		0	10	0	10	0	10	0	15	ns
tRAH	Row address hold time after RAS low		8		10		10		10	ns	
tCAH	Column address hold time after CAS low		13		15		15		15	ns	
tdZC	Delay time, data to CAS low (Note 18)		0		0		0		0	ns	
tdZO	Delay time, data to OE low (Note 18)		0		0		0		0	ns	
tcDD	Delay time, CAS high to data (Note 19)		13		15		20		20	ns	
tODD	Delay time, OE high to data (Note 19)		13		15		20		20	ns	
tT	Transition time (Note 20)		1	50	1	50	1	50	1	50	ns

Note 13. The timing requirements are assumed $t_T = 5ns$.

14. $V_{IH}(min)$ and $V_{IL}(max)$ are reference levels for measuring timing of input signals.

15. $t_{RCD}(max)$ is specified as a reference point only. If t_{RCD} is less than $t_{RCD}(max)$, access time is t_{RAC} .

If t_{RCD} is greater than $t_{RCD}(max)$, access time is controlled exclusively by t_{CAC} or t_{AA} .

$t_{RCD}(min)$ is specified as $t_{RCD}(min) = t_{RAH}(min) + 2t_T + t_{ASC}(min)$.

16. $t_{RAD}(max)$ is specified as a reference point only. If $t_{RAD} \geq t_{RAD}(max)$ and $t_{ASC} \leq t_{ASC}(max)$, access time is controlled exclusively by t_{AA} .

17. $t_{ASC}(max)$ is specified as a reference point only. If $t_{RCD} \geq t_{RCD}(max)$ and $t_{ASC} \geq t_{ASC}(max)$, access time is controlled exclusively by t_{CAC} .

18. Either t_{DZC} or t_{DZO} must be satisfied.

19. Either t_{cDD} or t_{ODD} must be satisfied.

20. t_T is measured between $V_{IH}(min)$ and $V_{IL}(max)$.

Read and Refresh Cycles

Symbol	Parameter		Limits								Unit
			M5M44400B-5, -5S		M5M44400B-6, -6S		M5M44400B-7-7S		M5M44400B-8, -8S		
			Min	Max	Min	Max	Min	Max	Min	Max	
tRC	Read cycle time		90		110		130		150	ns	
tRAS	RAS low pulse width		50	10000	60	10000	70	10000	80	10000	ns
tCAS	CAS low pulse width		13	10000	15	10000	20	10000	20	10000	ns
tCSH	CAS hold time after RAS low		50		60		70		80	ns	
tRSH	RAS hold time after CAS low		13		15		20		20	ns	
tRCS	Read setup time before CAS low		0		0		0		0	ns	
tRCH	Read hold time after CAS high (Note 21)		0		0		0		0	ns	
tRRH	Read hold time after RAS high (Note 21)		10		10		10		10	ns	
tRAL	Column address to RAS hold time		25		30		35		40	ns	
tOCH	CAS hold time after OE low		13		15		20		20	ns	
tORH	RAS hold time after OE low		13		15		20		20	ns	

Note 21. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.

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Write Cycle (Early Write and Delayed Write Cycles)

Symbol	Parameter	Limits								Unit
		M5M44400B-5, -5S		M5M44400B-6, -6S		M5M44400B-7, -7S		M5M44400B-8, -8S		
		Min	Max	Min	Max	Min	Max	Min	Max	
tWC	Write cycle time	90		110		130		150		ns
tRAS	RAS low pulse width	50	10000	60	10000	70	10000	80	10000	ns
tCAS	CAS low pulse width	13	10000	15	10000	20	10000	20	10000	ns
tCSH	CAS hold time after RAS low	50		60		70		80		ns
tRSH	RAS hold time after CAS low	13		15		20		20		ns
twCS	Write setup time before CAS low (Note 23)	0		0		0		0		ns
twCH	Write hold time after CAS low	8		10		15		15		ns
tcWL	CAS hold time after W low	13		15		20		20		ns
trWL	RAS hold time after W low	13		15		20		20		ns
tWP	Write pulse width	8		10		15		15		ns
tDS	Data setup time before CAS low or W low	0		0		0		0		ns
tDH	Data hold time after CAS low or W low	8		10		15		15		ns
toEH	OE hold time after W low	13		15		20		20		ns

Read-Write and Read-Modify-Write Cycles

Symbol	Parameter	Limits								Unit
		M5M44400B-5, -5S		M5M44400B-6, -6S		M5M44400B-7, -7S		M5M44400B-8, -8S		
		Min	Max	Min	Max	Min	Max	Min	Max	
trWC	Read Write/read modify write cycle time (Note 22)	126		150		175		195		ns
tRAS	RAS low pulse width	86	10000	95	10000	115	10000	125	10000	ns
tCAS	CAS low pulse width	49	10000	50	10000	65	10000	65	10000	ns
tCSH	CAS hold time after RAS low	86		95		115		125		ns
tRSH	RAS hold time after CAS low	49		50		65		65		ns
trCS	Read setup time before CAS low	0		0		0		0		ns
tcWD	Delay time, CAS low to W low (Note 23)	35		35		40		40		ns
trWD	Delay time, RAS low to W low (Note 23)	73		80		90		100		ns
tAWD	Delay time, address to W low (Note 23)	48		50		55		60		ns
tcWL	CAS hold time after W low	13		15		20		20		ns
trWL	RAS hold time after W low	13		15		20		20		ns
tWP	Write pulse width	8		10		15		15		ns
tDS	Data setup time before W low	0		0		0		0		ns
tDH	Data hold time after W low	8		10		15		15		ns
toEH	OE hold time after W low	13		15		15		20		ns

Note 22. trWC is specified as $trWC(\min) = tRAC(\max) + tODD(\min) + trWL(\min) + trP(\min) + 4t$.

23. twCS, tcWD, trWD and tAWD and tcpWD are specified as reference points only. If $twCS \geq twCS(\min)$ the cycle is an early write cycle and the DQ pins will remain high impedance throughout the entire cycle. If $tcWD \geq tcWD(\min)$, $trWD \geq trWD(\min)$, $tAWD \geq tAWD(\min)$, and $tcpWD \geq tcpWD(\min)$ (for fast page mode cycle only), the cycle is a read-modify-write cycle and the DQ will contain the data read from the selected address. If neither of the above condition (delayed-write) of the DQ (at access time and until CAS or OE goes back to VIH) is indeterminate.

Fast-Page Mode Cycle (Read, Write, Read-Write, and Read-Modify-Write Cycles) (Note 24)

Symbol	Parameter	Limits								Unit
		M5M44400B-5, -5S		M5M44400B-6, -6S		M5M44400B-7, -7S		M5M44400B-8, -8S		
		Min	Max	Min	Max	Min	Max	Min	Max	
tPC	Fast page mode read/write cycle time	35		40		45		50		ns
tPRWC	Fast Page mode read write/read modify write cycle time	71		75		95		100		ns
tRAS	RAS low pulse width for read write cycle (Note 25)	85	100000	100	100000	115	100000	135	100000	ns
tCP	CAS high pulse width (Note 26)	8	12	10	15	10	15	10	20	ns
tcPRH	RAS hold time after CAS precharge	30		35		40		45		ns
tcpWD	Delay time, CAS precharge to W low (Note 23)	30		35		40		45		ns

Note 24. All previously specified timing requirements and switching characteristics are applicable to their respective fast page mode cycle.

25. tRAS(min) is specified as two cycles of CAS input are performed.

26. tCP(max) is specified as a reference point only.

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CAS before RAS Refresh, Extended Refresh*Cycle (Note 27)

Symbol	Parameter	Limits								Unit
		M5M44400B-5, -5S		M5M44400B-6, -6S		M5M44400B-7, -7S		M5M44400B-8, -8S		
		Min	Max	Min	Max	Min	Max	Min	Max	
tCSR	CAS setup time before RAS low	5		5		5		5		ns
tCHR	CAS hold time after RAS low	10		10		15		15		ns
tRSR	Read setup time before RAS low	10		10		10		10		ns
tRHR	Read hold time after RAS low	10		10		15		15		ns
tCAS	CAS low pulse width	25		25		30		30		ns

Note 27. Eight or more CAS before RAS cycles instead of eight RAS cycles are necessary for proper operation of CAS before RAS refresh mode.

Self Refresh Cycle*

Symbol	Parameter	Limits								Unit
		M5M44400B-5S		M5M44400B-6S		M5M44400B-7S		M5M44400B-8S		
		Min	Max	Min	Max	Min	Max	Min	Max	
trASS	CBR self refresh RAS low pulse width	100		100		100		100		μs
trPS	CBR self refresh RAS high precharge time	90		110		130		150		ns
tCHS	CBR self refresh CAS hold time	-50		-50		-50		-50		ns
tRSR	Read setup time before RAS low	10		10		10		10		ns
tRHR	Read hold time after RAS low	10		10		15		15		ns

Test Mode Specification (Note 28)

ELECTRICAL CHARACTERISTICS (Ta = 0~70°C, Vcc = 5V ± 10%, Vss = 0V, unless otherwise noted) (Note 2)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
Icc1(AV)	Average supply current from Vcc operating (Note 3, 4, 5)	RAS, CAS cycling trc = twc = min. output open			145	mA
					115	
					100	
					85	
Icc3(AV)	Average supply current from Vcc refreshing (Note 3, 5)	RAS cycling CAS = VIH, trc = min. output open			145	mA
					115	
					100	
					85	
Icc4(AV)	Average supply current from Vcc Fast-Page-Mode (Note 3, 4, 5)	RAS = VIL CAS cycling trc = min., output open			145	mA
					115	
					100	
					85	
Icc6(AV)	Average supply current from Vcc CAS before RAS refresh mode (Note 3)	CAS before RAS refresh cycling, trc = min. output open			120	mA
					100	
					85	
					75	

Note 28. All previously specified electrical characteristics, switching characteristics and timing requirements are applicable to that of test mode.

M5M44400BJ,L,TP,RT-5,-6,-7,-8,-5S,-6S,-7S,-8S

FAST PAGE MODE 4194304-BIT(1048576-WORD BY 4-BIT)DYNAMIC RAM

SWITCHING CHARACTERISTICS (Ta = 0~70°C, Vcc = 5V ± 10%, Vss = 0V, unless otherwise noted) (Notes 6, 13, 14)

Symbol	Parameter	Limits								Unit
		M5M44400B-5, -5S		M5M44400B-6, -6S		M5M44400B-7, -7S		M5M44400B-8, -8S		
		Min	Max	Min	Max	Min	Max	Min	Max	
tCAC	Access time from $\overline{\text{CAS}}$ (Note 7, 8)		18		20		25		25	ns
tRAC	Access time from $\overline{\text{RAS}}$ (Note 7, 9)		55		65		75		85	ns
tAA	Column Address access time (Note 7, 10)		30		35		40		45	ns
tCPA	Access time from $\overline{\text{CAS}}$ precharge (Note 7, 11)		35		40		45		50	ns
tOEA	Access time from $\overline{\text{OE}}$ (Note 7)		18		20		25		25	ns

TIMING REQUIREMENTS (Ta = 0~70°C, Vcc = 5V ± 10%, Vss = 0V, unless otherwise noted) (Notes 13, 14)

Read and Refresh Cycles

Symbol	Parameter	Limits								Unit
		M5M44400B-5, -5S		M5M44400B-6, -6S		M5M44400B-7, -7S		M5M44400B-8, -8S		
		Min	Max	Min	Max	Min	Max	Min	Max	
trc	Read cycle time	95		115		135		155		ns
trAS	$\overline{\text{RAS}}$ low pulse width	55	10000	65	10000	75	10000	85	10000	ns
tCAS	$\overline{\text{CAS}}$ low pulse width	18	10000	20	10000	25	10000	25	10000	ns
tCSH	$\overline{\text{CAS}}$ hold time after $\overline{\text{RAS}}$ low	55		65		75		85		ns
trSH	$\overline{\text{RAS}}$ hold time after $\overline{\text{CAS}}$ low	18		20		25		25		ns
trAL	Column address to $\overline{\text{RAS}}$ hold time	30		35		40		45		ns
toCH	$\overline{\text{CAS}}$ hold time after $\overline{\text{OE}}$ low	18		20		25		25		ns
toRH	$\overline{\text{RAS}}$ hold time after $\overline{\text{OE}}$ low	18		20		25		25		ns

Read - Write and Read - Modify - Write Cycles

Symbol	Parameter	Limits								Unit
		M5M44400B-5, -5S		M5M44400B-6, -6S		M5M44400B-7, -7S		M5M44400B-8, -8S		
		Min	Max	Min	Max	Min	Max	Min	Max	
trWC	Read Write/read modify write cycle time (Note 22)	131		155		180		200		ns
trAS	$\overline{\text{RAS}}$ low pulse width	91	10000	100	10000	120	10000	130	10000	ns
tCAS	$\overline{\text{CAS}}$ low pulse width	54	10000	55	10000	70	10000	70	10000	ns
tCSH	$\overline{\text{CAS}}$ hold time after $\overline{\text{RAS}}$ low	91		100		120		130		ns
trSH	$\overline{\text{RAS}}$ hold time $\overline{\text{CAS}}$ low	54		55		70		70		ns
tcWD	Delay time, $\overline{\text{CAS}}$ low to $\overline{\text{W}}$ low (Note 23)	40		40		45		45		ns
trWD	Delay time, $\overline{\text{RAS}}$ low to $\overline{\text{W}}$ low (Note 23)	78		85		95		105		ns
tAWD	Delay time, address to $\overline{\text{W}}$ low (Note 23)	53		55		60		65		ns

Fast-Page Mode Cycle (Read, Write, Read - Write, and Read - Modify - Write Cycles) (Note 24)

Symbol	Parameter	Limits								Unit
		M5M44400B-5, -5S		M5M44400B-6, -6S		M5M44400B-7, -7S		M5M44400B-8, -8S		
		Min	Max	Min	Max	Min	Max	Min	Max	
tpc	Fast page mode read/write cycle time	40		45		50		55		ns
tpRWC	Fast page mode read write/read modify write cycle time	76		80		100		105		ns
trAS	$\overline{\text{RAS}}$ low pulse width for read write cycle	90	100000	110	100000	125	100000	145	100000	ns
tcPRH	$\overline{\text{RAS}}$ hold time after $\overline{\text{CAS}}$ precharge	35		40		45		50		ns
tcPWD	Delay time, $\overline{\text{CAS}}$ precharge to $\overline{\text{W}}$ low (Note 23)	35		40		45		50		ns

Test Mode Set Cycle

Symbol	Parameter	Limits								Unit
		M5M44400B-5, -5S		M5M44400B-6, -6S		M5M44400B-7, -7S		M5M44400B-8, -8S		
		Min	Max	Min	Max	Min	Max	Min	Max	
tWSR	Write setup time before $\overline{\text{RAS}}$ low	10		10		10		10		ns
tWHR	Write hold time after $\overline{\text{RAS}}$ low	10		10		15		15		ns

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Note 29. Self refresh sequence

Two refreshing ways should be used properly depending on the low pulse width(t_{RASS}) of \overline{RAS} signal during self refresh period.

1. In case of $t_{RASS} < 300ms$

1.1 Distributed refresh during Read/Write operation

(A) Timing Diagrams

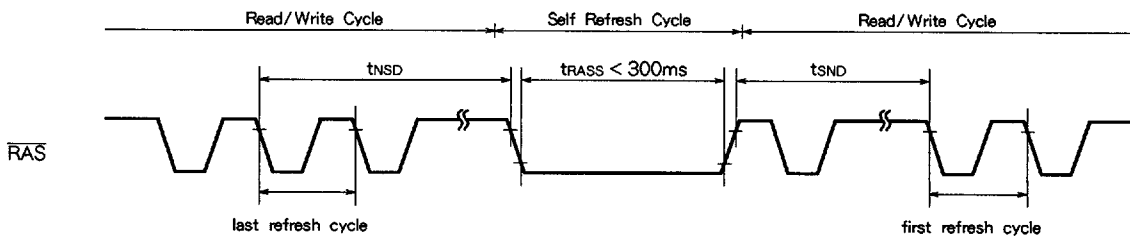


Table 2

Read/Write Cycle	Read/Write → Self Refresh	Self Refresh → Read/Write
CBR distributed refresh	$t_{NSD} + t_{NSD} \leq 16.4ms$	
\overline{RAS} only distributed refresh	$t_{NSD} \leq 16 \mu s$	$t_{NSD} \leq 16 \mu s$

(B) Definition of refresh

Definition of CBR distributed refresh

The CBR distributed refresh performs more than 1024 discrete CBR cycles within 16.4 ms.

Definition of \overline{RAS} only distributed refresh

All combination of nine row address signals ($A_0 \sim A_8$) are selected during 1024 discrete \overline{RAS} only refresh cycles within 16.4 ms.

1.1.1 CBR distributed Refresh

- Switching from read/write operation to self refresh operation. The time interval from the falling edge of \overline{RAS} signal in the last CBR refresh cycle during read/write operation period to the falling edge of \overline{RAS} signal at the start of self refresh operation should be set within t_{NSD} (shown in table 2).
- Switching from self refresh operation to read/write operation. The time interval from the rising edge of \overline{RAS} signal at the end of self refresh operation to the falling edge of \overline{RAS} signal in the first CBR refresh cycle during read/write operation period should be set within t_{NSD} (shown in table 2).

1.1.2 \overline{RAS} only distributed refresh

- Switching from read/write operation to self refresh operation. The time interval t_{NSD} from the falling edge of \overline{RAS} signal in the last \overline{RAS} only refresh cycle during read/write operation period to the falling edge of \overline{RAS} signal at the start of self refresh operation should be set within $16 \mu s$.
- Switching from self refresh operation to read/write operation. The time interval t_{NSD} from the rising edge of \overline{RAS} signal at the end of self refresh operation to the falling edge of \overline{RAS} signal in the first CBR refresh cycle during read/write operation period should be set within $16 \mu s$.

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1.2 Burst refresh during Read/Write operation

(A) Timing diagram

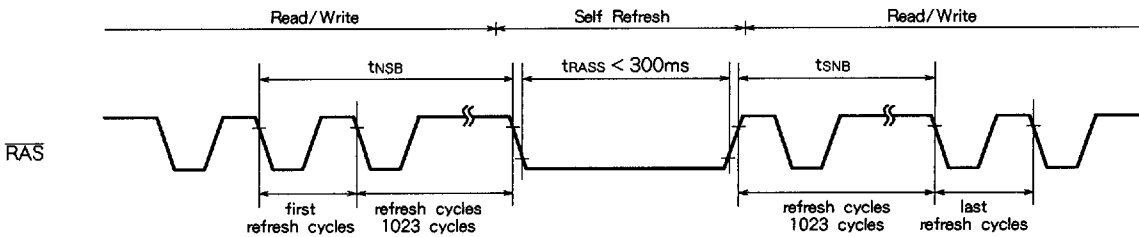


Table 3

Read/Write Cycle	Read/Write → Self Refresh	Self Refresh → Read/Write
CBR burst refresh	$t_{NSB} \leq 16.4ms$	$t_{SNB} \leq 16.4ms$
\overline{RAS} only burst refresh	$t_{NSB} + t_{SNB} \leq 16.4ms$	

(B) Definition of burst refresh

Definition of CBR burst refresh

The CBR burst refresh performs more than 1024 continuous CBR cycles within 16.4ms.

Definition of \overline{RAS} only burst refresh

All combination of ten row address signals ($A_0 \sim A_9$) are selected during 1024 continuous \overline{RAS} only refresh cycles within 16.4 ms.

1.2.1 CBR distributed Refresh

- Switching from read/write operation to self refresh operation. The time interval t_{NSB} from the falling edge of \overline{RAS} signal in the first CBR refresh cycle during read/write operation period to the falling edge of \overline{RAS} signal at the start of self refresh operation should be set within 16.4 ms.
- Switching from self refresh operation to read/write operation. The time interval t_{SNB} from the rising edge of \overline{RAS} signal at the end of self refresh operation to the falling edge of \overline{RAS} signal in the last CBR refresh cycle during read/write operation period should be set within 16.4 ms.

1.2.2 \overline{RAS} only distributed refresh

- Switching from read/write operation to self refresh operation. The time interval from the falling edge of \overline{RAS} signal in the first \overline{RAS} only refresh cycle during read/write operation period to the falling edge of \overline{RAS} signal at the start of self refresh operation should be set within t_{NSB} (shown in table 3).
- Switching from self refresh operation to read/write operation. The time interval from the rising edge of \overline{RAS} signal at the end of self refresh operation to the falling edge of \overline{RAS} signal in the last \overline{RAS} only refresh cycle during read/write operation period should be set within t_{SNB} (shown in table 3).

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2. In case of $t_{RAS} \geq 300ms$

(A) Timing diagram

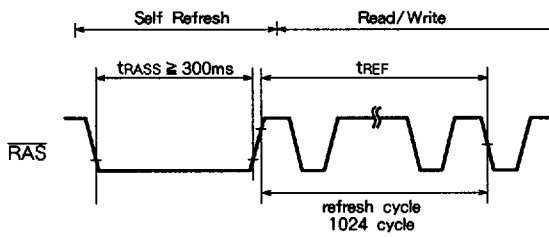


Table 4

Read/Write	Self Refresh→Read/Write
CBR distributed refresh	$t_{REF} \leq 16.4ms$
\overline{RAS} only distributed refresh	
CBR burst refresh	
\overline{RAS} only burst refresh	

(B) Definition of refresh

The same as 1.1-(B) and 1.2-(B)

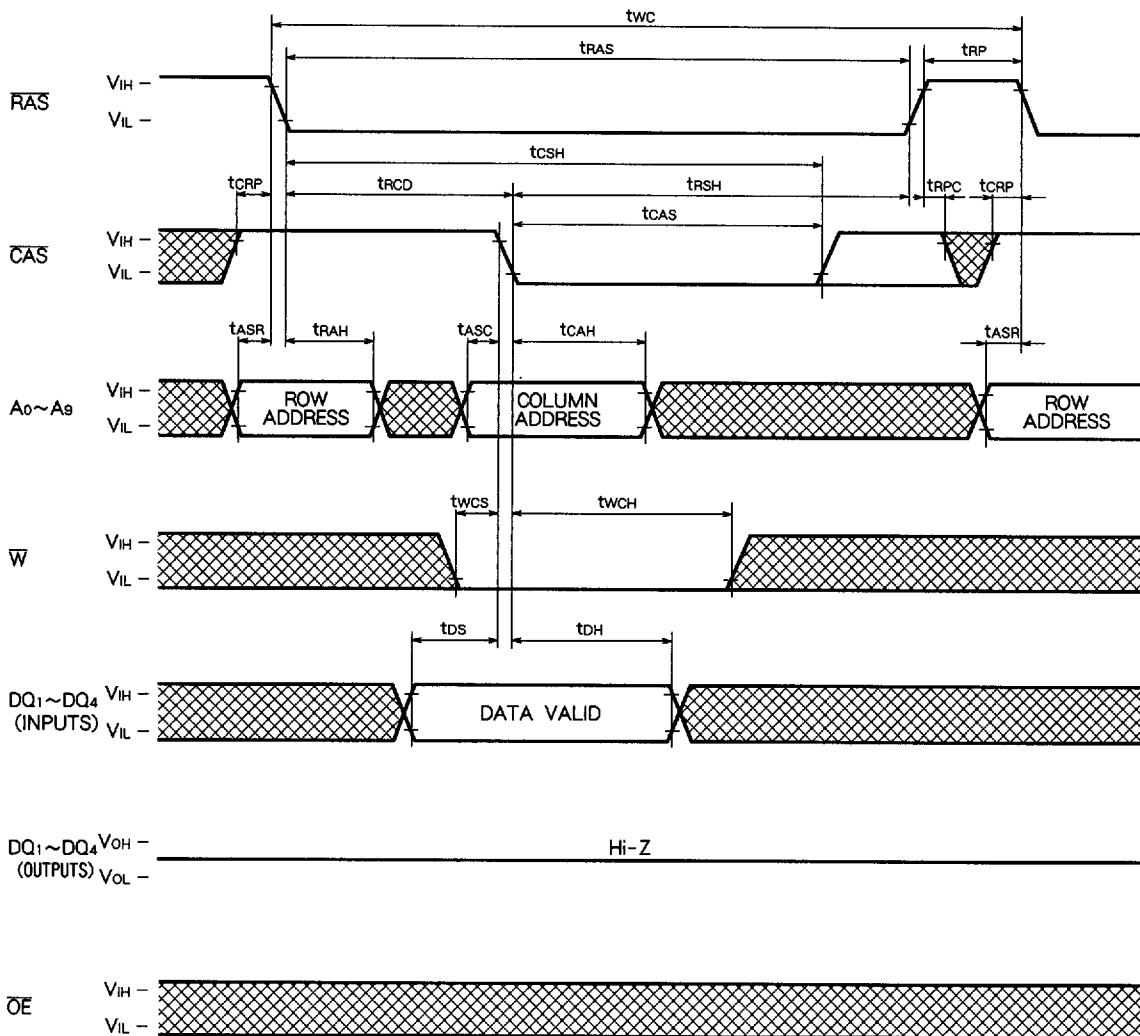
2.1

Regardless of the refresh (CBR distributed refresh, \overline{RAS} only distributed refresh, CBR burst refresh, \overline{RAS} only burst refresh) during Read/Write operation the minimum of 1024 cycles refresh should be performed within 16.4 ms from the rising edge of \overline{RAS} signal at the end of self refresh operation.

M5M44400BJ,L,TP,RT-5,-6,-7,-8,-5S,-6S,-7S,-8S

FAST PAGE MODE 4194304-BIT(1048576-WORD BY 4-BIT)DYNAMIC RAM

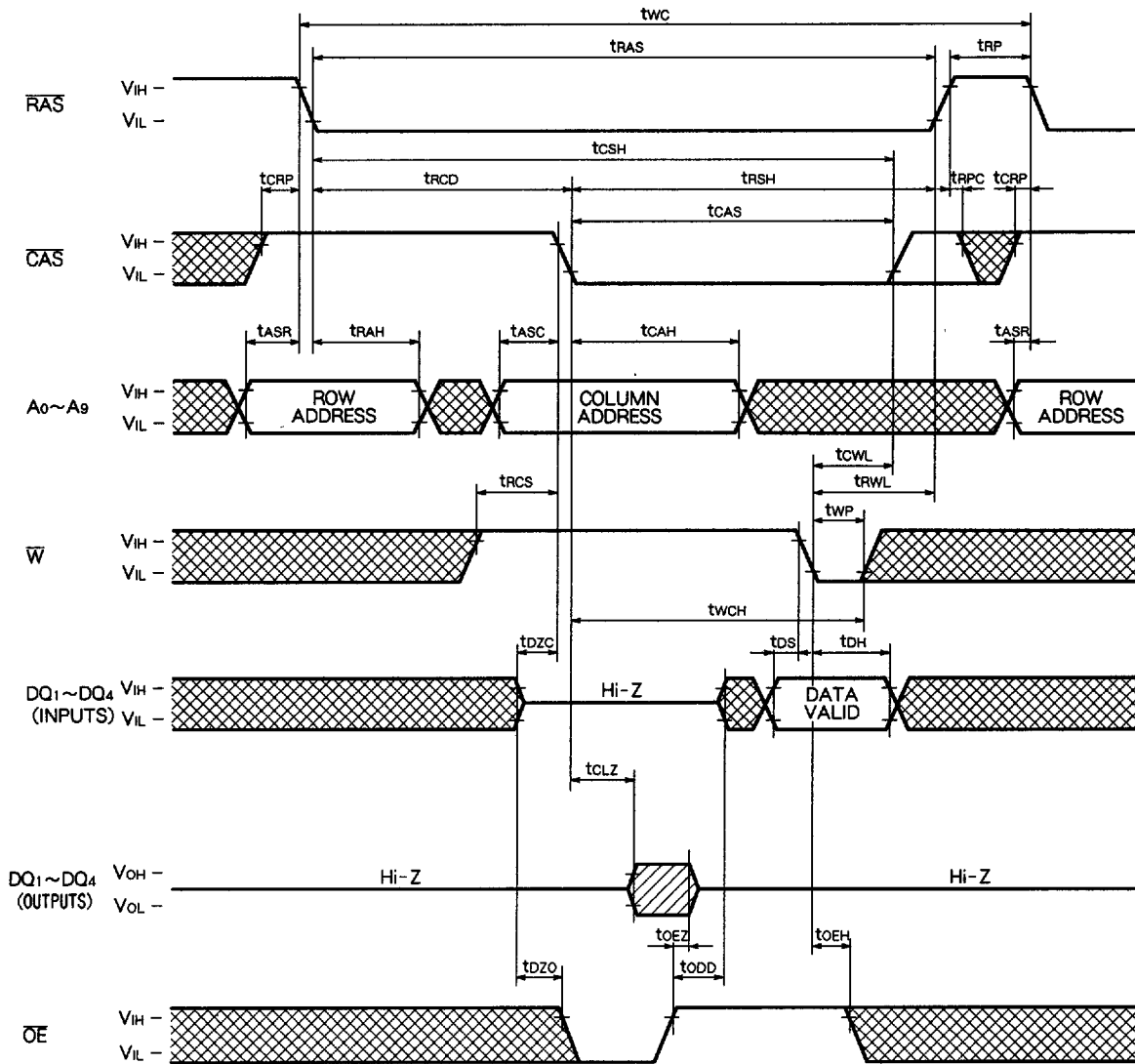
Write Cycle (Early write)



M5M44400BJ,L,TP,RT-5,-6,-7,-8,-5S,-6S,-7S,-8S

FAST PAGE MODE 4194304-BIT(1048576-WORD BY 4-BIT)DYNAMIC RAM

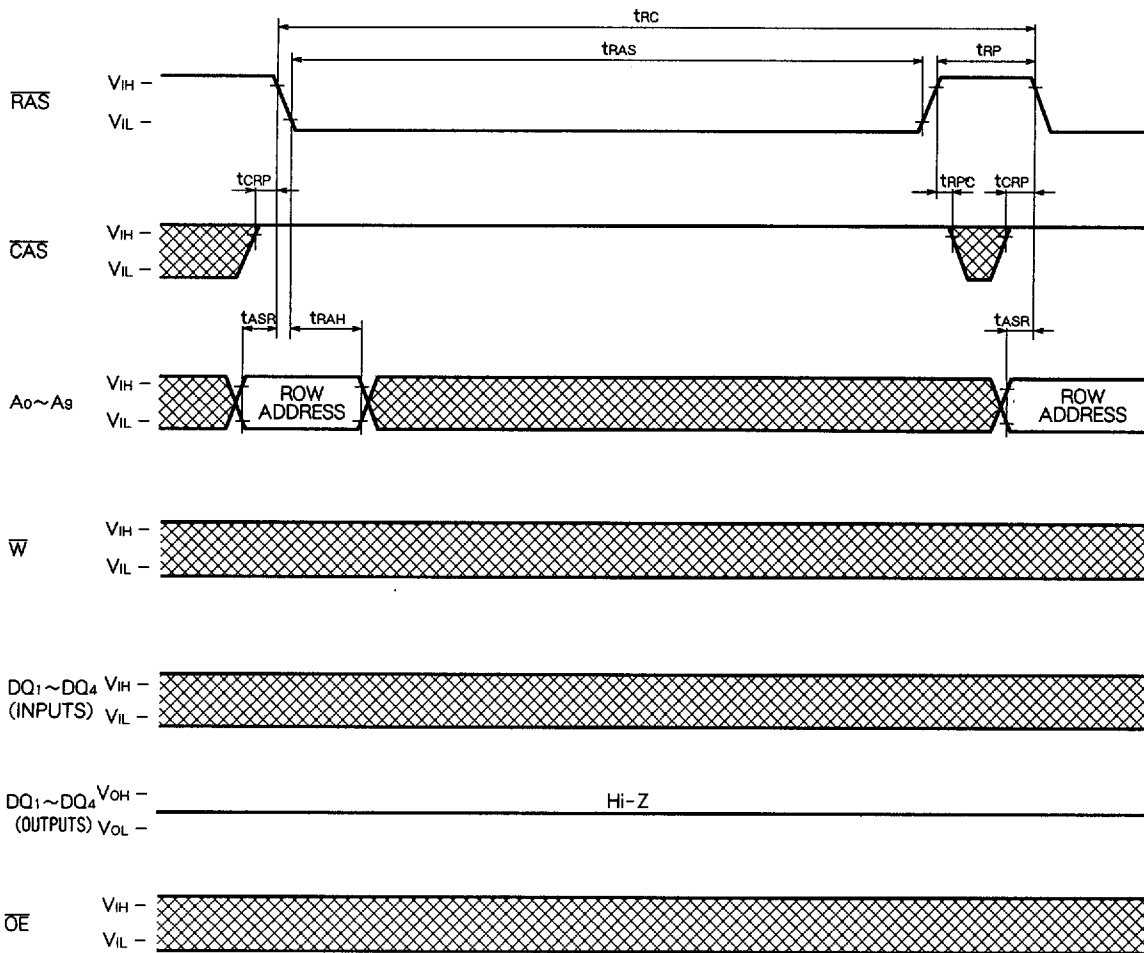
Write Cycle (Delayed Write)



M5M44400BJ,L,TP,RT-5,-6,-7,-8,-5S,-6S,-7S,-8S

FAST PAGE MODE 4194304-BIT(1048576-WORD BY 4-BIT)DYNAMIC RAM

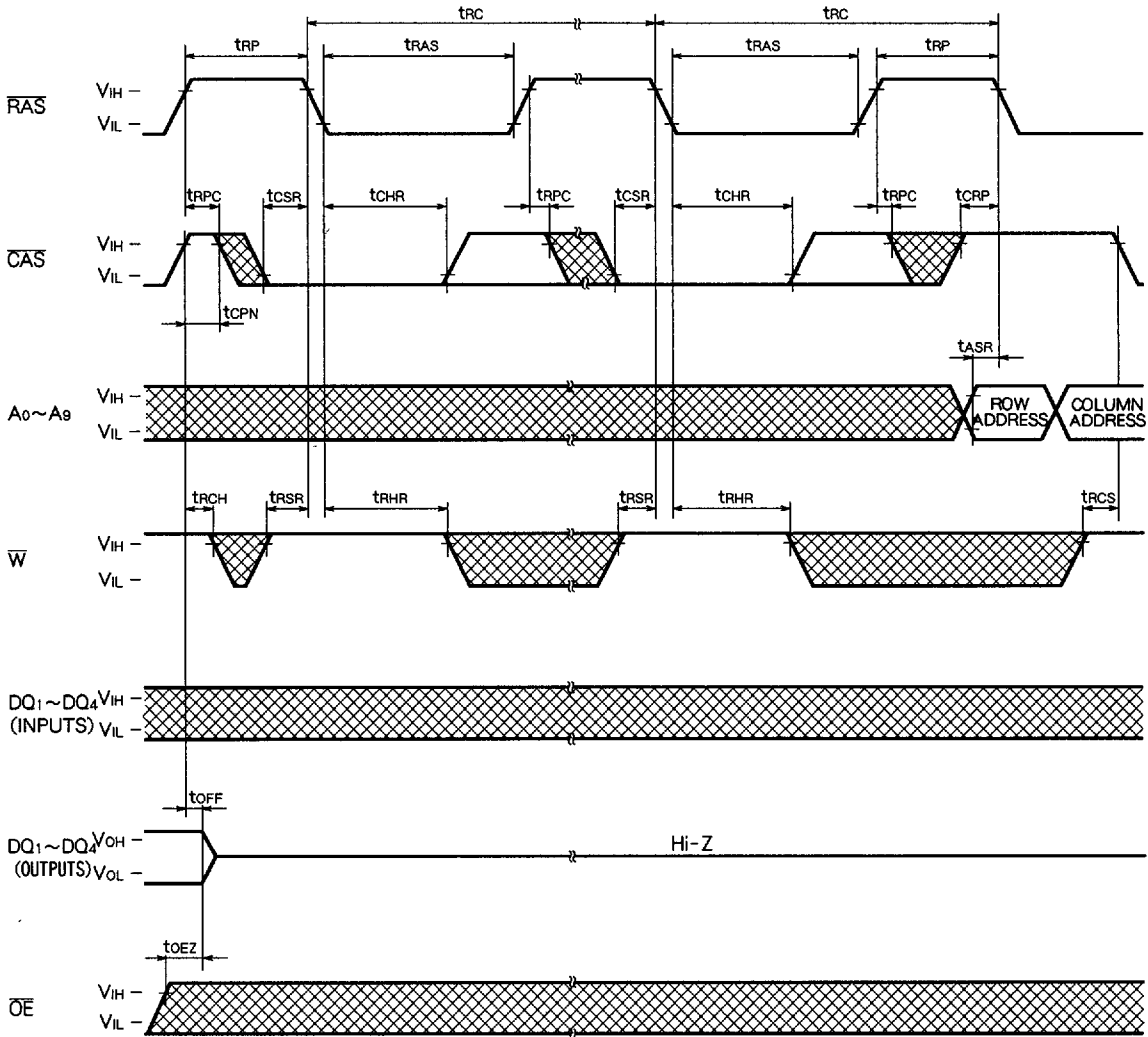
RAS-only Refresh Cycle



M5M44400BJ,L,TP,RT-5,-6,-7,-8,-5S,-6S,-7S,-8S

FAST PAGE MODE 4194304-BIT(1048576-WORD BY 4-BIT)DYNAMIC RAM

CAS before RAS Refresh Cycle, Extended Refresh Cycle *

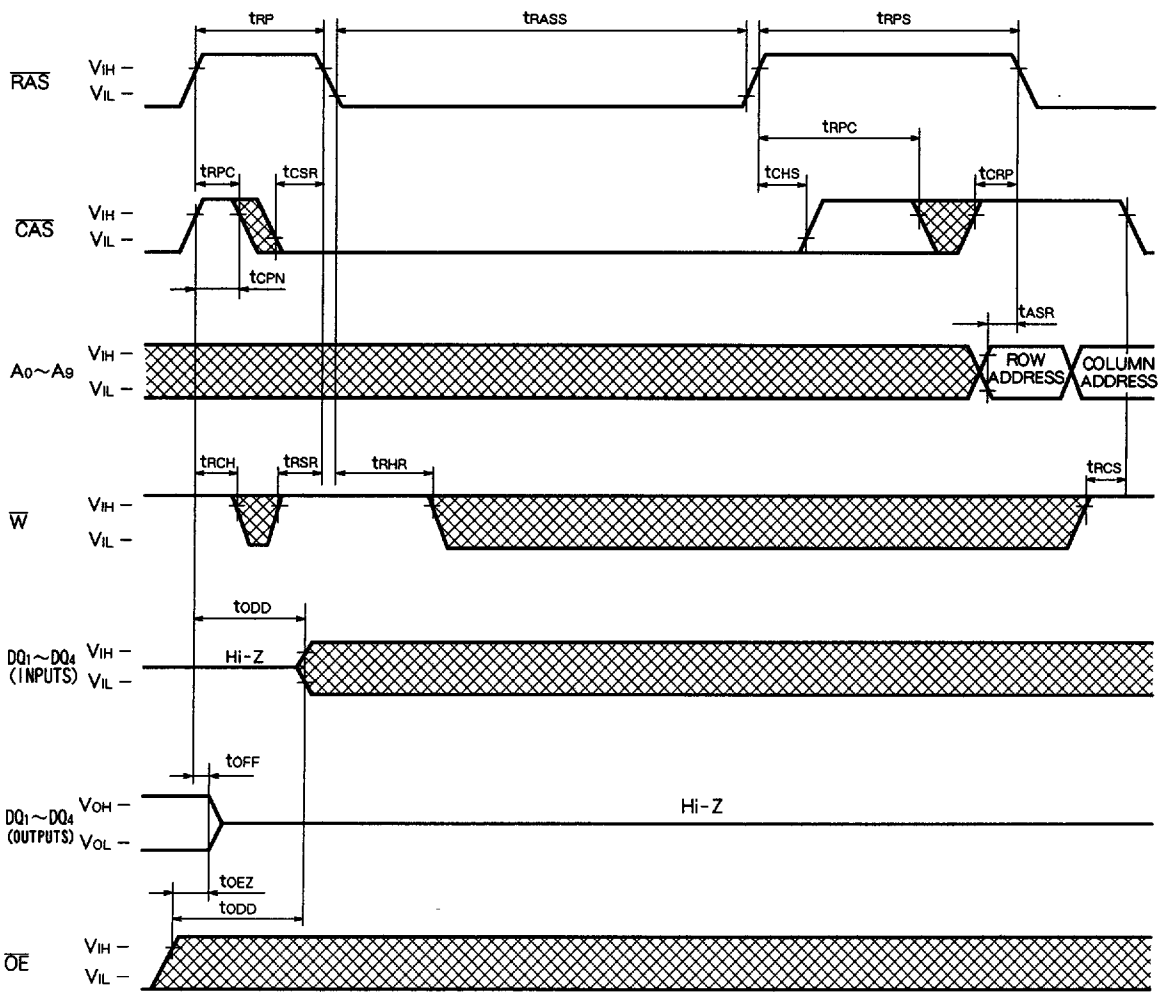


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M5M44400BJ,L,TP,RT-5,-6,-7,-8,-5S,-6S,-7S,-8S

FAST PAGE MODE 4194304-BIT(1048576-WORD BY 4-BIT)DYNAMIC RAM

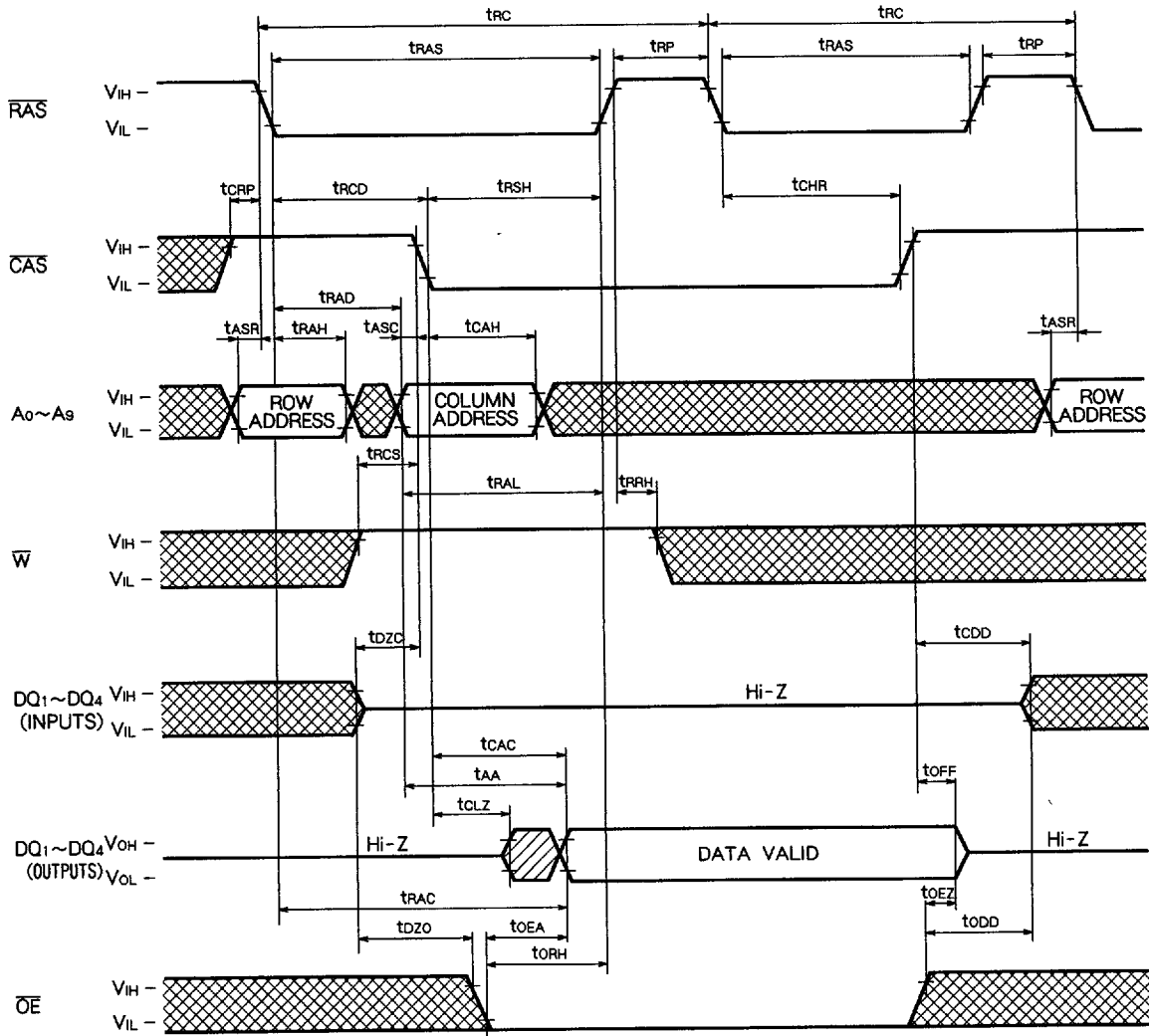
Self Refresh Cycle* (Note 29)



M5M44400BJ,L,TP,RT-5,-6,-7,-8,-5S,-6S,-7S,-8S

FAST PAGE MODE 4194304-BIT(1048576-WORD BY 4-BIT)DYNAMIC RAM

Hidden Refresh Cycle (Read) (Note 31)

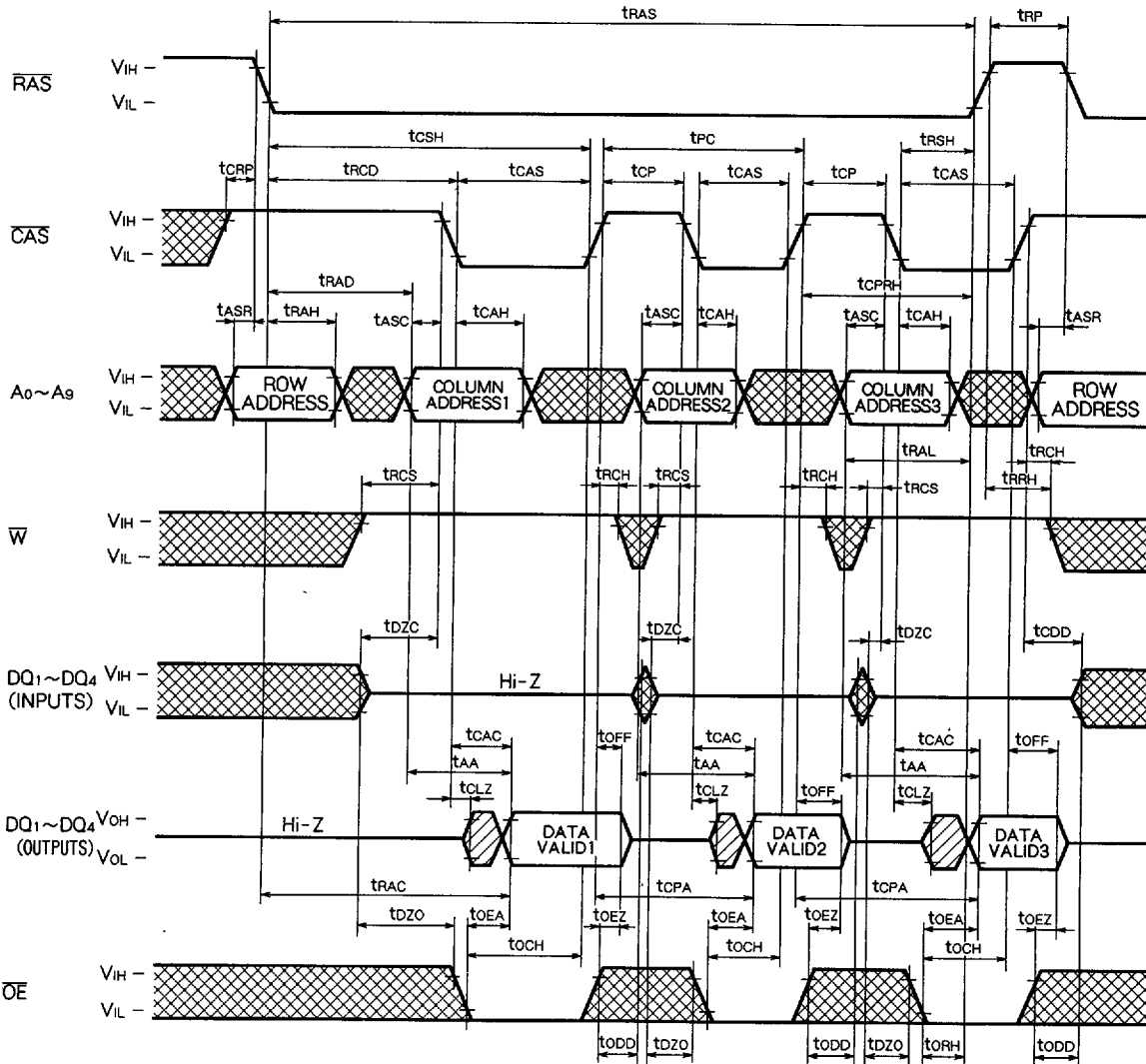


Note 31. Early write, delayed write, read write or read modify write cycle is applicable instead of read cycle.
 Timing requirements and output state are the same as that of each cycle shown above.

M5M44400BJ,L,TP,RT-5,-6,-7,-8,-5S,-6S,-7S,-8S

FAST PAGE MODE 4194304-BIT(1048576-WORD BY 4-BIT)DYNAMIC RAM

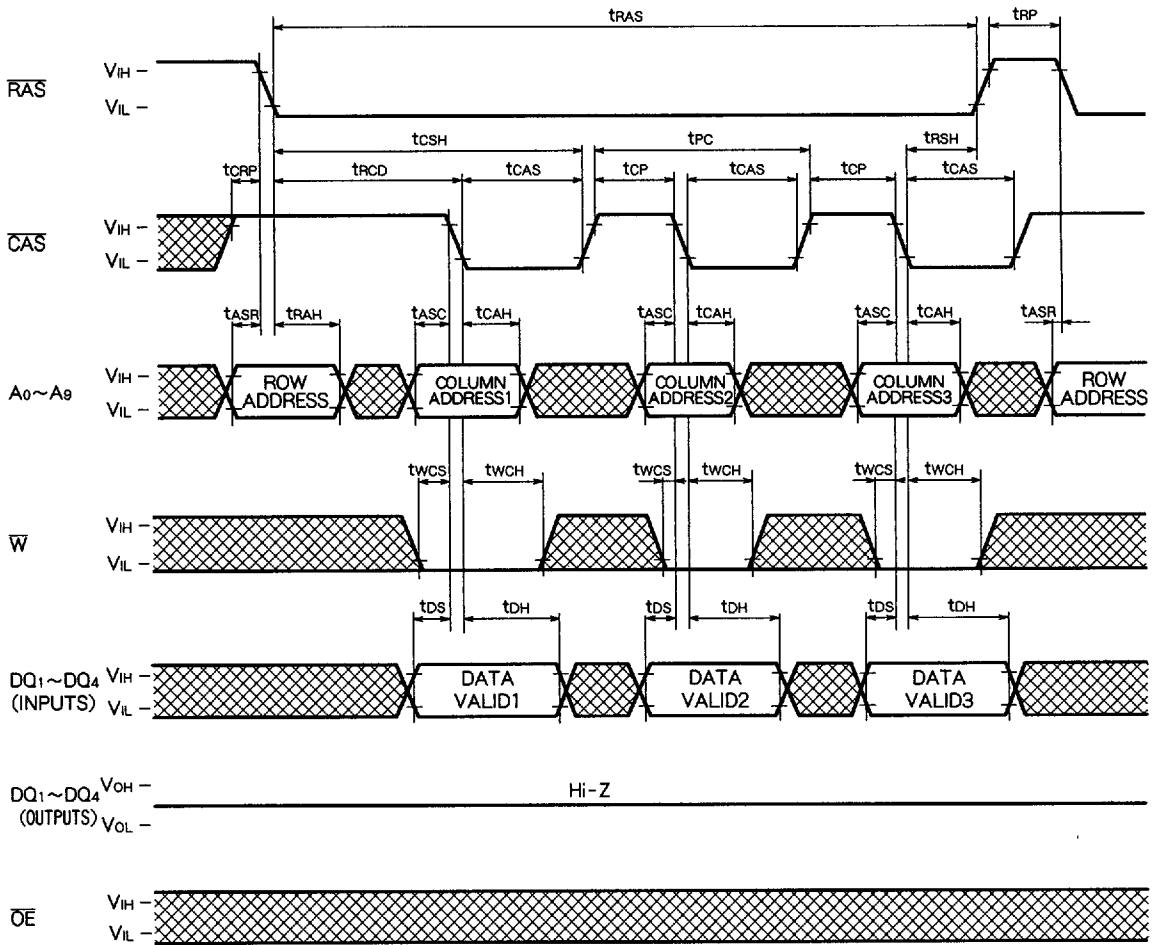
Fast Page Mode Read Cycle



M5M44400BJ,L,TP,RT-5,-6,-7,-8,-5S,-6S,-7S,-8S

FAST PAGE MODE 4194304-BIT(1048576-WORD BY 4-BIT)DYNAMIC RAM

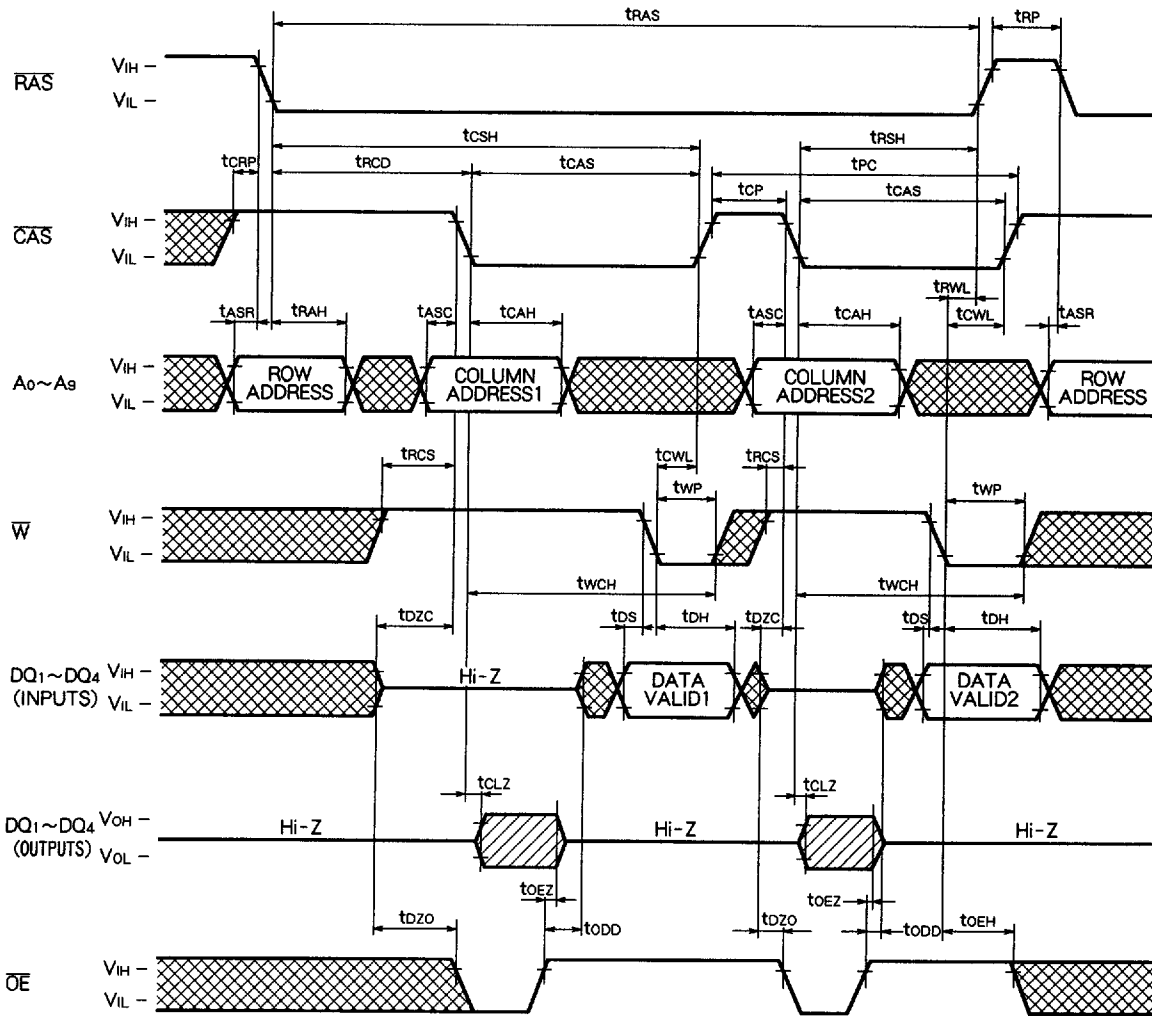
Fast Page Mode Write Cycle (Early Write)



M5M44400BJ,L,TP,RT-5,-6,-7,-8,-5S,-6S,-7S,-8S

FAST PAGE MODE 4194304-BIT(1048576-WORD BY 4-BIT)DYNAMIC RAM

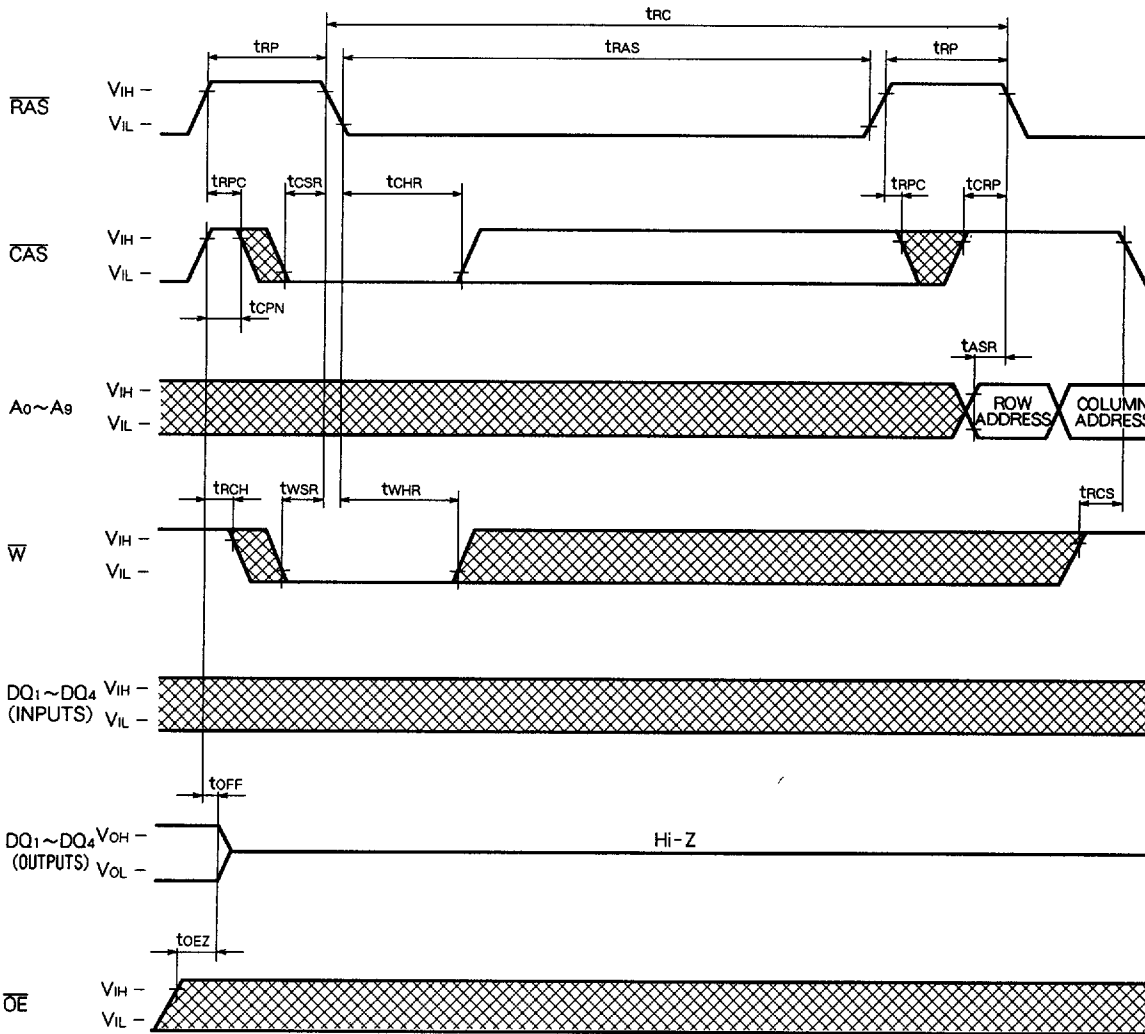
Fast Page Mode Write Cycle (Delayed Write)



M5M44400BJ,L,TP,RT-5,-6,-7,-8,-5S,-6S,-7S,-8S

FAST PAGE MODE 4194304-BIT(1048576-WORD BY 4-BIT)DYNAMIC RAM

Test Mode Set Cycle (Note 32)



Note 32. The cycle is also available for the initialization cycle, but in this case device enters test mode. The test mode function is initiated with a \bar{W} and \bar{CAS} before \bar{RAS} cycle (WCBR cycle) as specified above timing diagram. The test mode function is terminated by either a \bar{CAS} before \bar{RAS} (CBR) refresh or a \bar{RAS} only refresh cycle. During the test mode, the device is internally organized as 4 bits wide (256 kilobytes deep) for each DQ (input/output) port. No addressing of A0, A1 (column only) is required. During a write cycle, data on the each DQ (input) pin is written in parallel into all 4 bits for each DQ port and can be written independently for each DQ port. During a read cycle, the each DQ (output) pin indicates independently a HIGH state if all 4 bits are equal, and a LOW state if any bits differ. During the test mode operation, a WCBR cycle is used to perform refresh.