



SANYO Semiconductors

DATA SHEET

LE25FU406B — CMOS IC 4M-bit (512K×8) Serial Flash Memory

Overview

The LE25FU406B is a serial interface-compatible flash memory device with a 512K × 8-bit configuration. It uses a single 2.5V power supply for both reading and writing (program and erase functions) and does not require a special power supply. As such, it can support on-board programming. It has three erase functions, each of which corresponds to the size of the memory area in which the data is to be erased at one time: the small sector (4K bytes) erase function, the sector (64K bytes) erase function, and the chip erase function (for erasing all the data together). The memory space can be efficiently utilized by selecting one of these functions depending on the application. A page program method is supported for data writing. The page program method of the LE25FU406B can program any amount of data from 1 to 256 bytes. The program time of 2.0ms (typ.) when programming 256 bytes (1 page) at one time makes for fast data writing. While making the most of the features inherent to a serial flash memory device, the LE25FU406B is housed in an 8-pin ultra-miniature package. Serial flash memory devices tend to be at a disadvantage in terms of their read speed, but the LE25FU406B has maximally eliminated this speed-related disadvantage by supporting clocks with frequencies up to 30MHz under SPI bus specifications. All these features make this device ideally suited to storing program codes in applications such as portable information devices and small disk systems, which are required to have increasingly more compact dimensions.

Features

- Read/write operations enabled by single 2.5V power supply: 2.30 to 3.60V supply voltage range
- Operating frequency : 30MHz
50MHz (at the planning stage)
- Temperature range : 0 to 70°C
-40 to +85°C (at the planning stage)

Continued on next page.

* This product is licensed from Silicon Storage Technology, Inc. (USA), and manufactured and sold by SANYO Semiconductor Co., Ltd.

■ Any and all SANYO Semiconductor Co.,Ltd. products described or contained herein are, with regard to "standard application", intended for the use as general electronics equipment (home appliances, AV equipment, communication device, office equipment, industrial equipment etc.). The products mentioned herein shall not be intended for use for any "special application" (medical equipment whose purpose is to sustain life, aerospace instrument, nuclear control device, burning appliances, transportation machine, traffic signal system, safety equipment etc.) that shall require extremely high level of reliability and can directly threaten human lives in case of failure or malfunction of the product or may cause harm to human bodies, nor shall they grant any guarantee thereof. If you should intend to use our products for applications outside the standard applications of our customer who is considering such use and/or outside the scope of our intended standard applications, please consult with us prior to the intended use. If there is no consultation or inquiry before the intended use, our customer shall be solely responsible for the use.

■ Specifications of any and all SANYO Semiconductor Co.,Ltd. products described or contained herein stipulate the performance, characteristics, and functions of the described products in the independent state, and are not guarantees of the performance, characteristics, and functions of the described products as mounted in the customer's products or equipment. To verify symptoms and states that cannot be evaluated in an independent device, the customer should always evaluate and test devices mounted in the customer's products or equipment.

SANYO Semiconductor Co., Ltd.

TOKYO OFFICE Tokyo Bldg., 1-10, 1 Chome, Ueno, Taito-ku, TOKYO, 110-8534 JAPAN

LE25FU406B

Continued from preceding page.

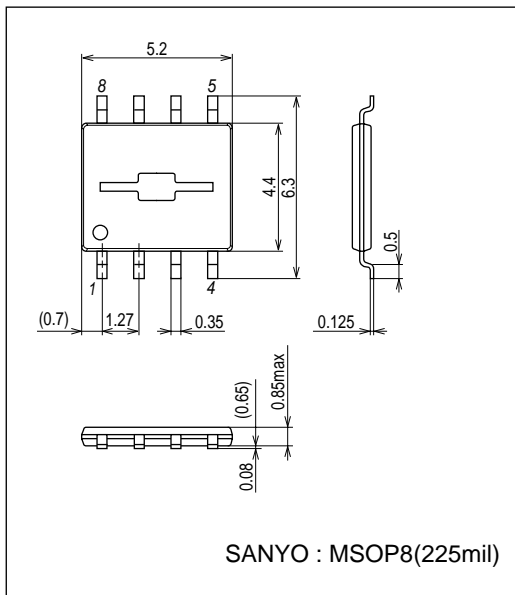
- Serial interface : SPI mode 0, mode 3 supported
- Sector size : 4K bytes/small sector, 64K bytes/sector
- Small sector erase, sector erase, chip erase functions
- Page program function (256 bytes/page)
- Block protect function
- Highly reliable read/write
 - Number of rewrite times : 100,000 times
 - Small sector erase time : 40ms (typ.), 150ms (max.)
 - Sector erase time : 80ms (typ.), 250ms (max.)
 - Chip erase time : 200ms (typ.), 2.0s (max.)
 - Page program time : 2.0ms/256 bytes (typ.), 2.5ms/256 bytes (max.)
- Status functions
 - Ready/busy information, protect information
- Data retention period : 20 years
- Package : LE25FU406BTT MSOP8 (225mil)
 : LE25FU406BMA MFP8 (225mil)
 : LE25FU406BFN VSON8

Package Dimensions

unit:mm (typ)

3276

[LE25FU406BTT]

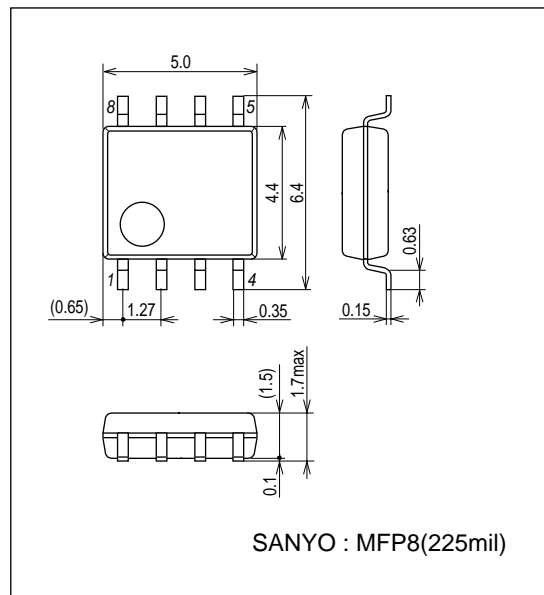


Package Dimensions

unit:mm (typ)

3032D

[LE25FU406BMA]



LE25FU406B

Package Dimensions

unit:mm (typ)

3327

[LE25FU406BFN]

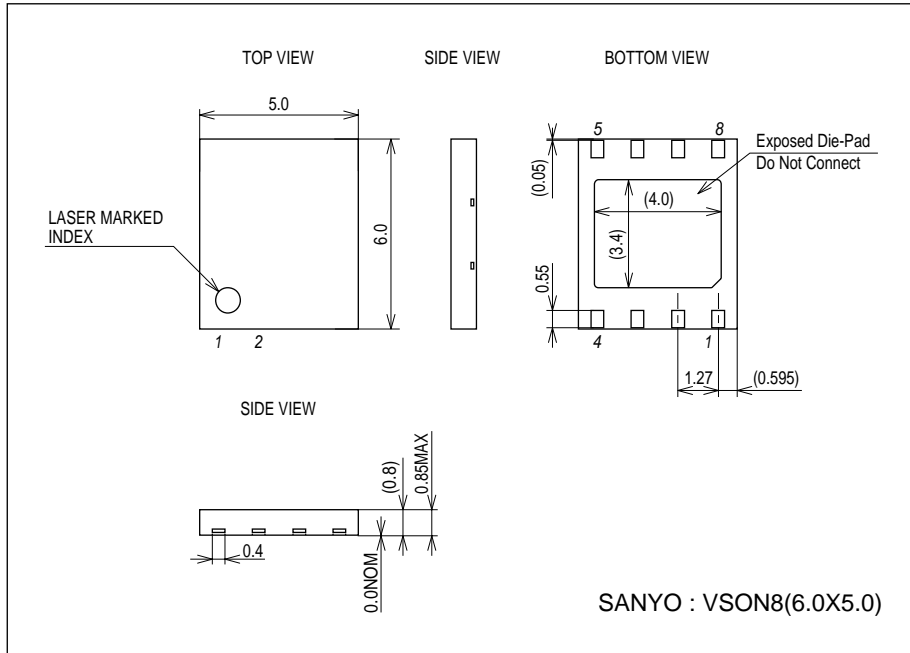
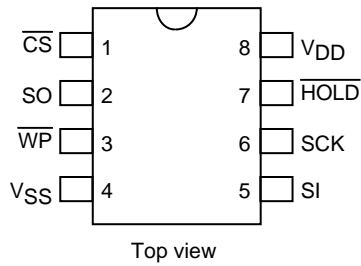
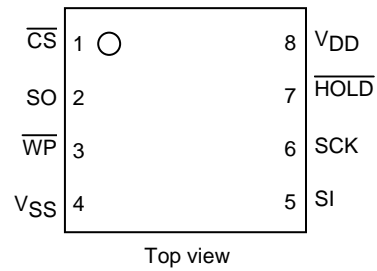


Figure 1 Pin Assignments



MSOP8 (LE25FU406BTT)
MFP8 (LE25FU406BMA)



VSON8 (LE25FU406BFN)

Figure 2 Block Diagram

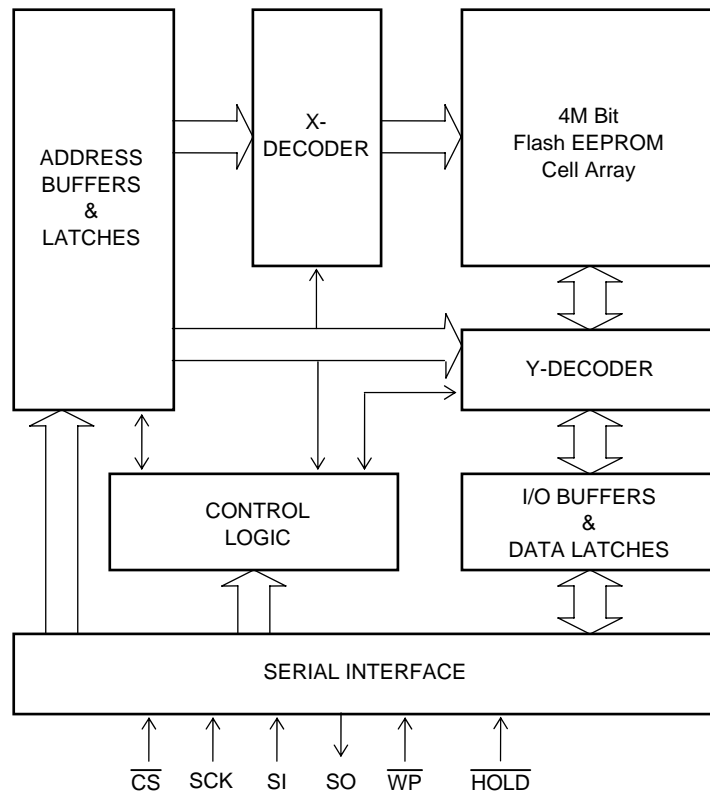


Table 1 Pin Description

| Symbol | Pin Name | Description |
|--------------------------|--------------------|---|
| SCK | Serial clock | This pin controls the data input/output timing. The input data and addresses are latched synchronized to the rising edge of the serial clock, and the data is output synchronized to the falling edge of the serial clock. |
| SI | Serial data input | The data and addresses are input from this pin, and latched internally synchronized to the rising edge of the serial clock. |
| SO | Serial data output | The data stored inside the device is output from this pin synchronized to the falling edge of the serial clock. |
| $\overline{\text{CS}}$ | Chip select | The device becomes active when the logic level of this pin is low; it is deselected and placed in standby status when the logic level of the pin is high. |
| WP | Write protect | The status register write protect (SRWP) takes effect when the logic level of this pin is low. |
| $\overline{\text{HOLD}}$ | Hold | Serial communication is suspended when the logic level of this pin is low. |
| V _{DD} | Power supply | This pin supplies the 2.30 to 3.60V supply voltage. |
| V _{SS} | Ground | This pin supplies the 0V supply voltage. |

LE25FU406B

Table 2 Command Settings

| Command | 1st bus cycle | 2nd bus cycle | 3rd bus cycle | 4th bus cycle | 5th bus cycle | 6th bus cycle | Nth bus cycle |
|-----------------------|---------------|---------------|---------------|---------------|---------------|---------------|---------------|
| Read | 03h | A23-A16 | A15-A8 | A7-A0 | | | |
| | 0Bh | A23-A16 | A15-A8 | A7-A0 | X | | |
| Small sector erase | D7h | A23-A16 | A15-A8 | A7-A0 | | | |
| Sector erase | D8h | A23-A16 | A15-A8 | A7-A0 | | | |
| Chip erase | C7h | | | | | | |
| Page program | 02h | A23-A16 | A15-A8 | A7-A0 | PD *1 | PD *1 | PD *1 |
| Write enable | 06h | | | | | | |
| Write disable | 04h | | | | | | |
| Power down | B9h | | | | | | |
| Status register read | 05h | | | | | | |
| Status register write | 01h | DATA | | | | | |
| Read silicon ID 1 *2 | 9Fh | | | | | | |
| Read silicon ID 2 *3 | ABh | X | X | A7-A0 | | | |
| Exit power down mode | ABh | | | | | | |

Explanatory notes for Table 2

"X" signifies "don't care" (that is to say, any value may be input).

The "h" following each code indicates that the number given is in hexadecimal notation.

Addresses A23 to A19 for all commands are "Don't care".

In order for commands other than the read command to be recognized, \overline{CS} must rise after all the bus cycle input.

*1: "PD" stands for page program data. Any amount of data from 1 to 256 bytes in 1-byte unit is input.

*2: Of the two silicon ID commands, it is for the command with the 9Fh setting that the manufacturer code 62h is first output. For as long as the clock input is continued, 1Eh of the device code is output continuously, followed by the repeated output of 62h and 1Eh.

*3: Of the two silicon ID commands, it is for the command with the ABh setting that manufacturer code 62h is first output when address A0 is "0", and the device code 1Eh is first output when address A0 is "1".

Addresses A7 to A1 are "don't care". For as long as the clock input is continued, 62h and 1Eh are repeatedly output.

Device Operation

The LE25FU406B features electrical on-chip erase functions using a single 2.5V power supply, that have been added to the EPROM functions of the industry standard that support serial interfaces. Interfacing and control are facilitated by incorporating the command registers inside the chip. The read, erase, program and other required functions of the device are executed through the command registers. The command addresses and data input in accordance with "Table 2 Command Settings" are latched inside the device in order to execute the required operations. "Figure 3 Serial Input Timing" shows the timing waveforms of the serial data input. First, at the falling \overline{CS} edge the device is selected, and serial input is enabled for the commands, addresses, etc. These inputs are introduced internally in sequence starting with bit 7 in synchronization with the rising SCK edge. At this time, output pin SO is in the high-impedance state. The output pin is placed in the low-impedance state when the data is output in sequence starting with bit 7 synchronized to the falling clock edge during read, status register read and silicon ID. Refer to "Figure 4 Serial Output Timing" for the serial output timing.

The LE25FU406B supports both serial interface SPI mode 0 and SPI mode 3. At the falling \overline{CS} edge, SPI mode 0 is automatically selected if the logic level of SCK is low, and SPI mode 3 is automatically selected if the logic level of SCK is high.

Figure 3 Serial Input Timing

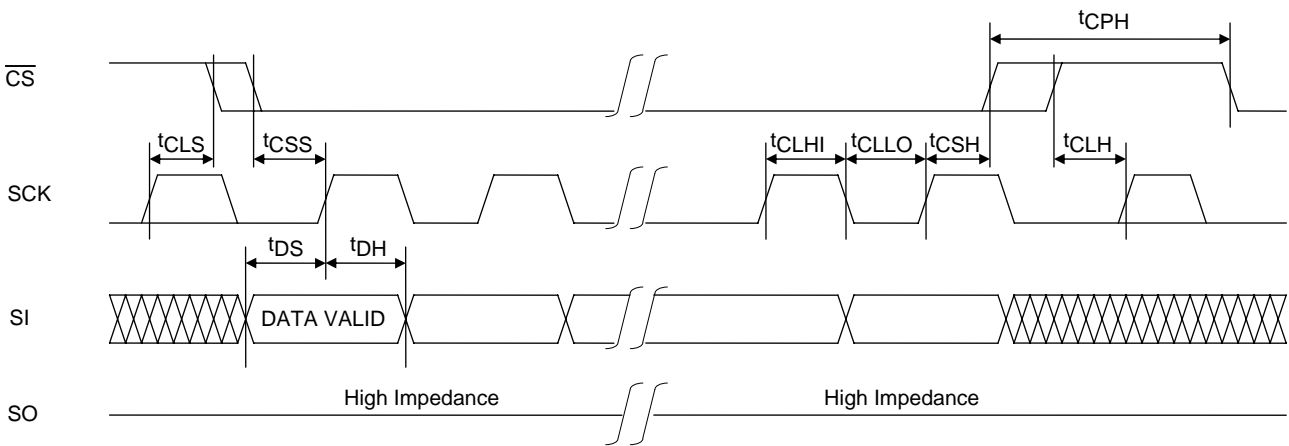
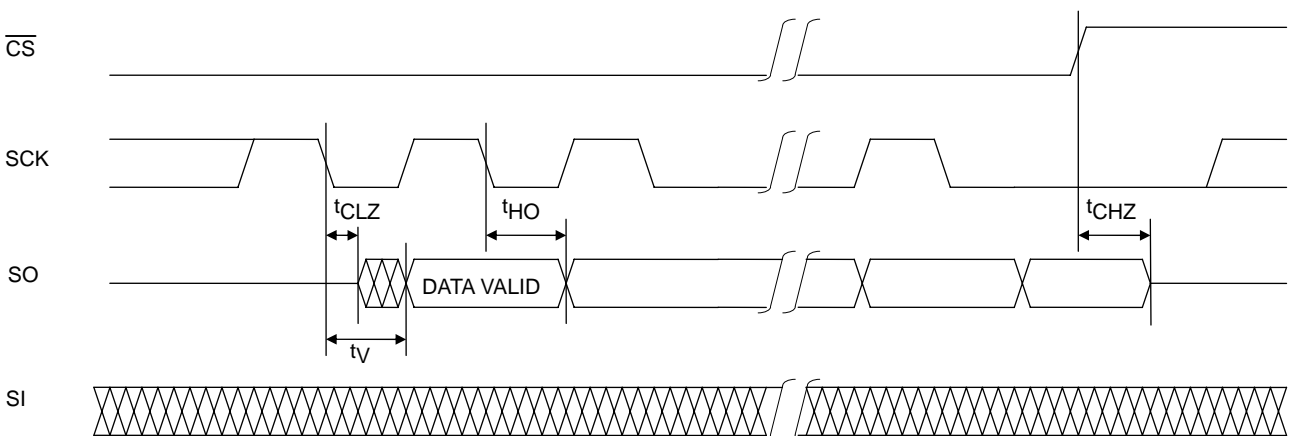


Figure 4 Serial Output Timing



Description of Commands and Their Operations

"Table 2 Command Settings" provides a list and overview of the commands. A detailed description of the functions and operations corresponding to each command is presented below.

1. Read

There are two read commands, the 4 bus cycle read command and 5 bus cycle read command. Consisting of the first through fourth bus cycles, the 4 bus cycle read command inputs the 24-bit addresses following (03h), and the data in the designated addresses is output synchronized to SCK. The data is output from SO on the falling clock edge of fourth bus cycle bit 0 as a reference. "Figure 5-a 4 Bus Read" shows the timing waveforms.

Consisting of the first through fifth bus cycles, the 5 bus cycle read command inputs the 24-bit addresses and 8 dummy bits following (0Bh). The data is output from SO using the falling clock edge of fifth bus cycle bit 0 as a reference. "Figure 5-b 5 Bus Read" shows the timing waveforms. The only difference between these two commands is whether the dummy bits in the fifth bus cycle are input.

When SCK is input continuously after the read command has been input and the data in the designated addresses has been output, the address is automatically incremented inside the device while SCK is being input, and the corresponding data is output in sequence. If the SCK input is continued after the internal address arrives at the highest address (7FFFh), the internal address returns to the lowest address (0000h), and data output is continued. By setting the logic level of CS to high, the device is deselected, and the read cycle ends. While the device is deselected, the output pin SO is in a high-impedance state.

Figure 5-a 4 Bus Read

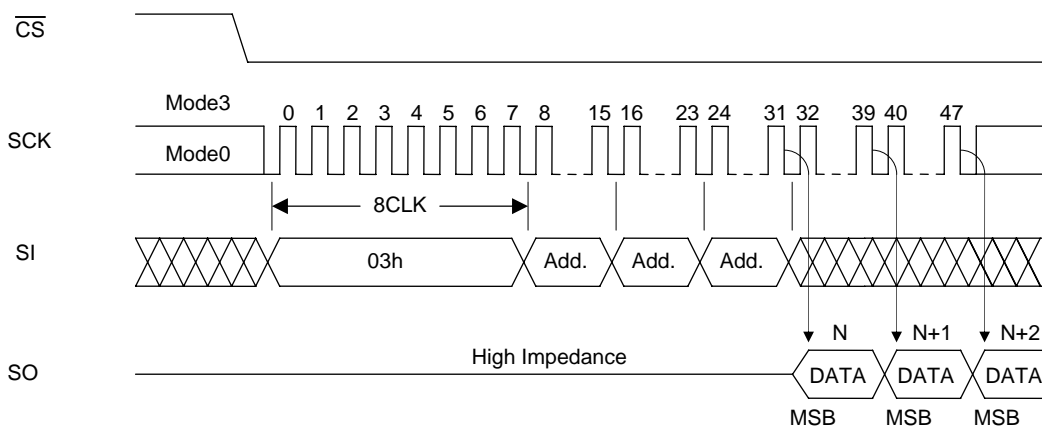
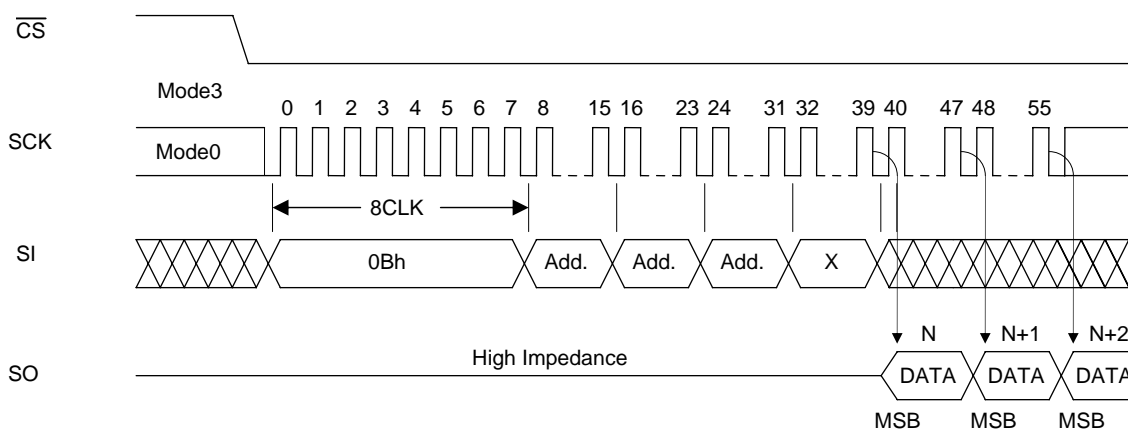


Figure 5-b 5 Bus Read



2. Status Registers

The status registers hold the operating and setting statuses inside the device, and this information can be read (status register read) and the protect information can be rewritten (status register write). There are 8 bits in total, and "Table 3 Status registers" gives the significance of each bit.

Table 3 Status Registers

| Bit | Name | Logic | Function | Power-on Time Information | | | | |
|------|-------------------------|-------|---|---------------------------|---|-------------------------|---|-------------------------|
| Bit0 | $\overline{\text{RDY}}$ | 0 | Ready | 0 | | | | |
| | | 1 | Erase/Program | | | | | |
| Bit1 | WEN | 0 | Write disabled | 0 | | | | |
| | | 1 | Write enabled | | | | | |
| Bit2 | BP0 | 0 | Block protect information See status register descriptions on BP0, BP1, and BP2. | Nonvolatile information | | | | |
| | | 1 | | | | | | |
| Bit3 | BP1 | 0 | | | Block protect information See status register descriptions on BP0, BP1, and BP2. | Nonvolatile information | | |
| | | 1 | | | | | | |
| Bit4 | BP2 | 0 | | | | | Block protect information See status register descriptions on BP0, BP1, and BP2. | Nonvolatile information |
| | | 1 | | | | | | |
| Bit5 | | | Reserved bits | 0 | | | | |
| Bit6 | | | | 0 | | | | |
| Bit7 | SRWP | 0 | Status register write enabled | Nonvolatile information | | | | |
| | | 1 | Status register write disabled | | | | | |

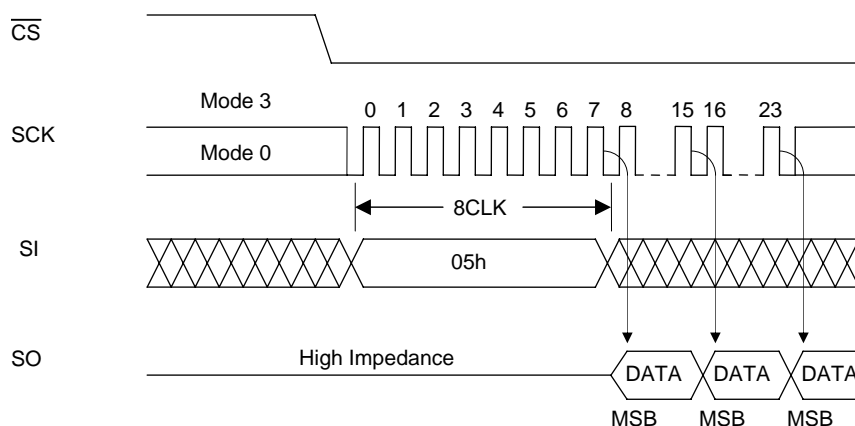
2-1. Status register read

The contents of the status registers can be read using the status register read command. This command can be executed even during the following operations.

- Small sector erase, sector erase, chip erase
- Page program
- Status register write

"Figure 6 Status Register Read" shows the timing waveforms of status register read. Consisting only of the first bus cycle, the status register command outputs the contents of the status registers synchronized to the falling edge of the clock (SCK) with which the eighth bit of (05h) has been input. In terms of the output sequence, SRWP (bit 7) is the first to be output, and each time one clock is input, all the other bits up to RDY (bit 0) are output in sequence, synchronized to the falling clock edge. If the clock input is continued after RDY (bit 0) has been output, the data is output by returning to the bit (SRWP) that was first output, after which the output is repeated for as long as the clock input is continued. The data can be read by the status register read command at any time (even during a program or erase cycle).

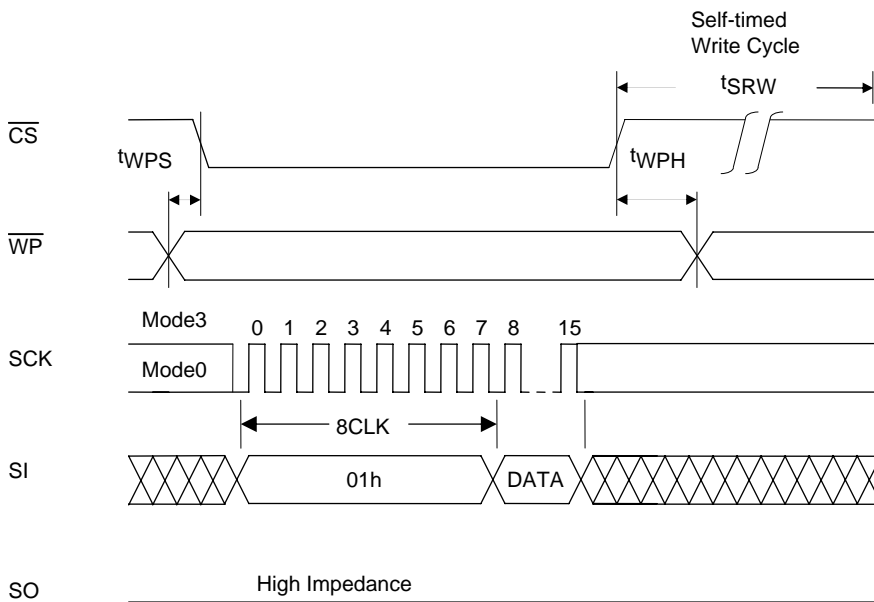
Figure 6 Status Register Read



2-2. Status register write

The information in status registers BP0, BP1, BP2 and SRWP can be rewritten using the status register write command. RDY, WEN, bit 5, and bit 6 are read-only bits and cannot be rewritten. The information in bits BP0, BP1, BP2, and SRWP is stored in the non-volatile memory, and when it is written in these bits, the contents are retained even at power-down. "Figure 7 Status Register Write" shows the timing waveforms of status register write, and Figure 20 shows a status register write flowchart. Consisting of the first and second bus cycles, the status register write command initiates the internal write operation at the rising CS edge after the data has been input following (01h). Erase and program are performed automatically inside the device by status register write so that erasing or other processing is unnecessary before executing the command. By the operation of this command, the information in bits BP0, BP1, BP2, and SRWP can be rewritten. Since bits RDY (bit 0), WEN (bit 1), 4, 5, and 6 of the status register cannot be written, no problem will arise if an attempt is made to set them to any value when rewriting the status register. Status register write ends can be detected by RDY of status register read. Information in the status registers can be rewritten 1,000 times (min.). To initiate status register write, the logic level of the WP pin must be set high and status register WEN must be set to "1".

Figure 7 Status Register Write



2-3. Contents of each status register

RDY (bit 0)

The RDY register is for detecting the write (program, erase and status register write) end. When it is "1", the device is in a busy state, and when it is "0", it means that write is completed.

LE25FU406B

WEN (bit 1)

The WEN register is for detecting whether the device can perform write operations. If it is set to "0", the device will not perform the write operation even if the write command is input. If it is set to "1", the device can perform write operations in any area that is not block-protected.

WEN can be controlled using the write enable and write disable commands. By inputting the write enable command (06h), WEN can be set to "1"; by inputting the write disable command (04h), it can be set to "0." In the following states, WEN is automatically set to "0" in order to protect against unintentional writing.

- At power-on
- Upon completion of small sector erase, sector erase or chip erase
- Upon completion of page program
- Upon completion of status register write

* If a write operation has not been performed inside the LE25FU406B because, for instance, the command input for any of the write operations (small sector erase, sector erase, chip erase, page program, or status register write) has failed or a write operation has been performed for a protected address, WEN will retain the status established prior to the issue of the command concerned. Furthermore, its state will not be changed by a read operation.

BP0, BP1, BP2 (bits 2, 3, 4)

Block protect BP0, BP1, and BP2 are status register bits that can be rewritten, and the memory space to be protected can be set depending on these bits. For the setting conditions, refer to "Table 4 Protect level setting conditions".

Table 4 Protect Level Setting Conditions

| Protect Level | Status Register Bits | | | Protected Area |
|----------------------------|----------------------|-----|-----|------------------|
| | BP2 | BP1 | BP0 | |
| 0 (Whole area unprotected) | 0 | 0 | 0 | None |
| 1 (1/8 protected) | 0 | 0 | 1 | 70000h to 7FFFFh |
| 2 (1/4 protected) | 0 | 1 | 0 | 60000h to 7FFFFh |
| 3 (1/2 protected) | 0 | 1 | 1 | 40000h to 7FFFFh |
| 4 (Whole area protected) | 1 | 0 | 0 | 00000h to 7FFFFh |
| 4 (Whole area protected) | 1 | 0 | 1 | 00000h to 7FFFFh |
| 4 (Whole area protected) | 1 | 1 | 0 | 00000h to 7FFFFh |
| 4 (Whole area protected) | 1 | 1 | 1 | 00000h to 7FFFFh |

* Chip erase is enabled only when the protect level is 0.

SRWP (bit 7)

Status register write protect SRWP is the bit for protecting the status registers, and its information can be rewritten. When SRWP is "1" and the logic level of the \overline{WP} pin is low, the status register write command is ignored, and status registers BP0, BP1, BP2, and SRWP are protected. When the logic level of the \overline{WP} pin is high, the status registers are not protected regardless of the SRWP state. The SRWP setting conditions are shown in "Table 5 SRWP setting conditions".

Table 5 SRWP Setting Conditions

| \overline{WP} Pin | SRWP | Status Register Protect State |
|---------------------|------|-------------------------------|
| 0 | 0 | Unprotected |
| | 1 | Protected |
| 1 | 0 | Unprotected |
| | 1 | Unprotected |

Bits 5 and 6 are reserved bits, and have no significance.

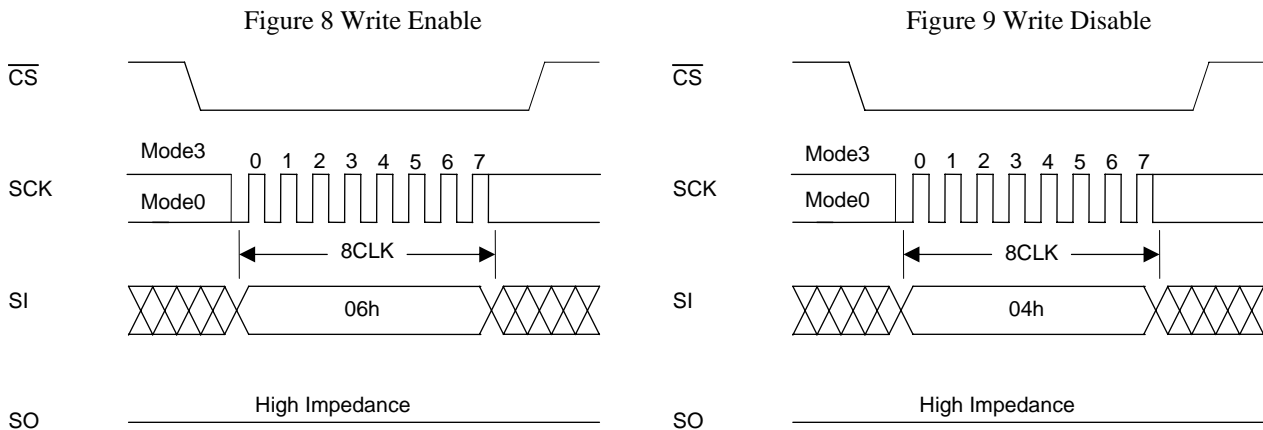
3. Write Enable

Before performing any of the operations listed below, the device must be placed in the write enable state. Operation is the same as for setting status register WEN to "1", and the state is enabled by inputting the write enable command. "Figure 8 Write Enable" shows the timing waveforms when the write enable operation is performed. The write enable command consists only of the first bus cycle, and it is initiated by inputting (06h).

- Small sector erase, sector erase, chip erase
- Page program
- Status register write

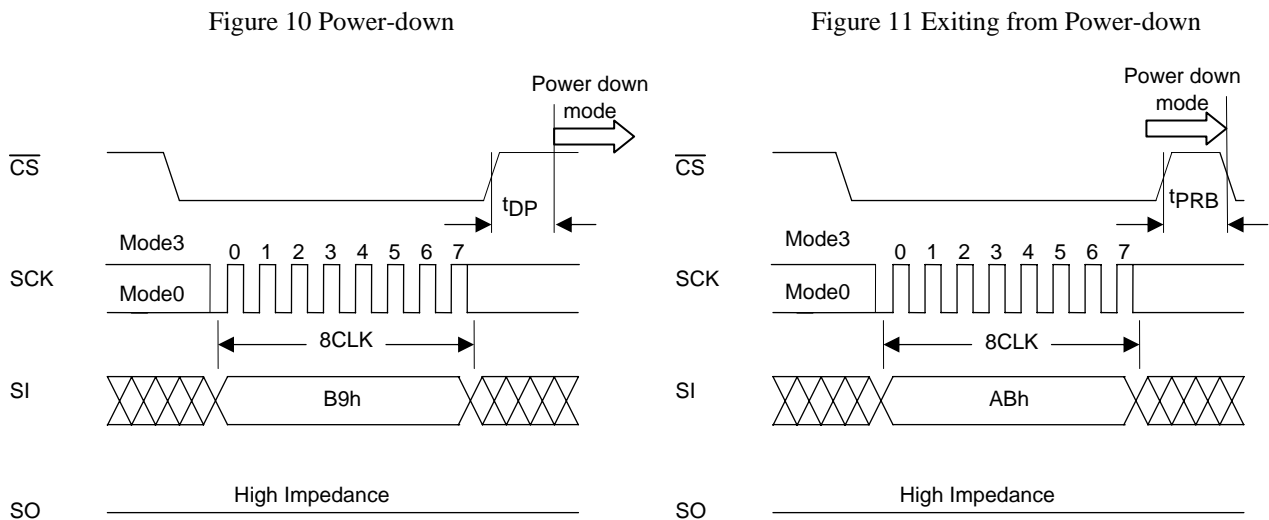
4. Write Disable

The write disable command sets status register WEN to "0" to prohibit unintentional writing. "Figure 9 Write Disable" shows the timing waveforms. The write disable command consists only of the first bus cycle, and it is initiated by inputting (04h). The write disable state (WEN "0") is exited by setting WEN to "1" using the write enable command (06h).



5. Power-down

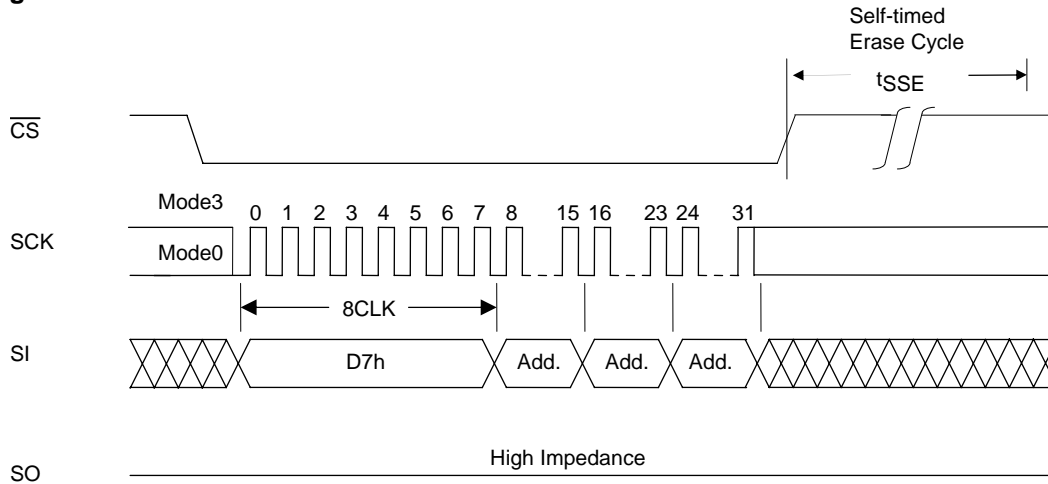
The power-down command sets all the commands, with the exception of the silicon ID read command and the command to exit from power-down, to the acceptance prohibited state (power-down). "Figure 10 Power-down" shows the timing waveforms. The power-down command consists only of the first bus cycle, and it is initiated by inputting (B9h). However, a power-down command issued during an internal write operation will be ignored. The power-down state is exited using the power-down exit command (power-down is exited also when one bus cycle or more of the silicon ID read command (ABh) has been input). "Figure 11 Exiting from Power-down" shows the timing waveforms of the power-down exit command.



6. Small Sector Erase

Small sector erase is an operation that sets the memory cell data in any small sector to "1". A small sector consists of 4Kbytes. "Figure 12 Small Sector Erase" shows the timing waveforms, and Figure 21 shows a small sector erase flowchart. The small sector erase command consists of the first through fourth bus cycles, and it is initiated by inputting the 24-bit addresses following (D7h). Addresses A18 to A12 are valid, and Addresses A23 to A19 are "don't care". After the command has been input, the internal erase operation starts from the rising \overline{CS} edge, and it ends automatically by the control exercised by the internal timer. Erase end can also be detected using status register \overline{RDY} .

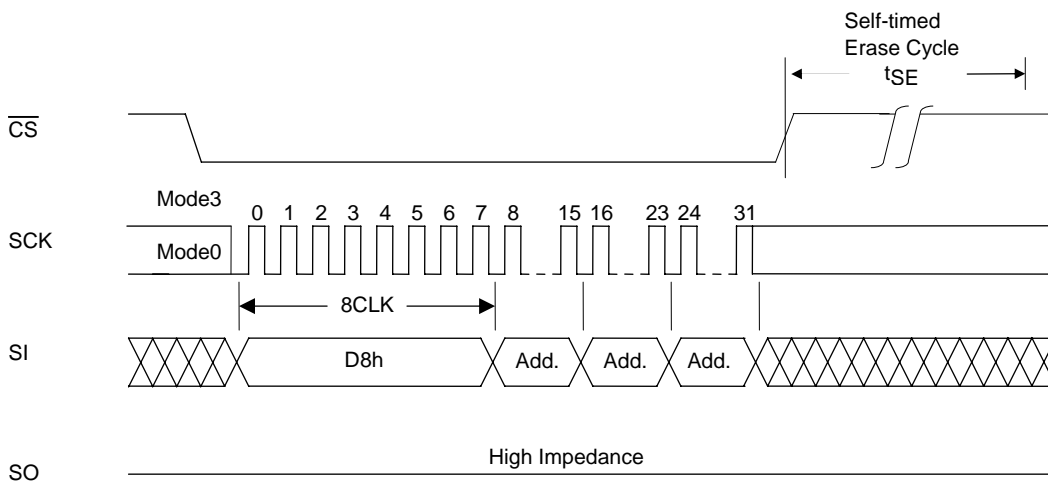
Figure 12 Small Sector Erase



7. Sector Erase

Sector erase is an operation that sets the memory cell data in any sector to "1". A sector consists of 64Kbytes. "Figure 13 Sector Erase" shows the timing waveforms, and Figure 21 shows a sector erase flowchart. The sector erase command consists of the first through fourth bus cycles, and it is initiated by inputting the 24-bit addresses following (D8h). Addresses A18 to A16 are valid, and Addresses A23 to A19 are "don't care". After the command has been input, the internal erase operation starts from the rising \overline{CS} edge, and it ends automatically by the control exercised by the internal timer. Erase end can also be detected using status register \overline{RDY} .

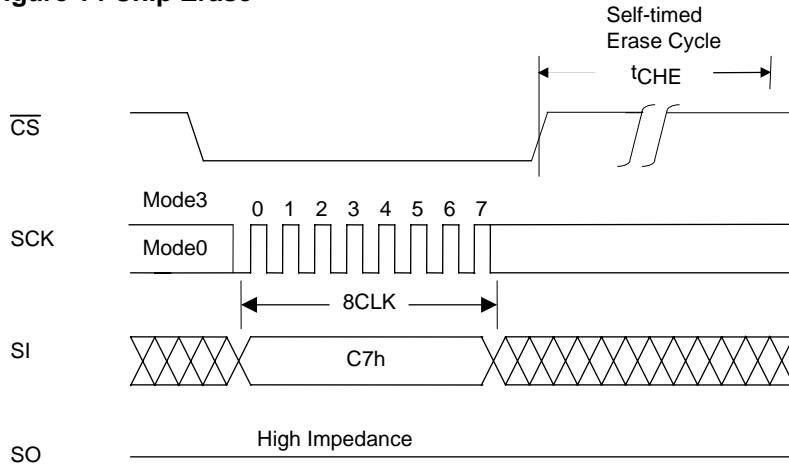
Figure 13 Sector Erase



8. Chip Erase

Chip erase is an operation that sets the memory cell data in all the sectors to "1". "Figure 14 Chip Erase" shows the timing waveforms, and Figure 21 shows a chip erase flowchart. The chip erase command consists only of the first bus cycle, and it is initiated by inputting (C7h). After the command has been input, the internal erase operation starts from the rising \overline{CS} edge, and it ends automatically by the control exercised by the internal timer. Erase end can also be detected using status register \overline{RDY} .

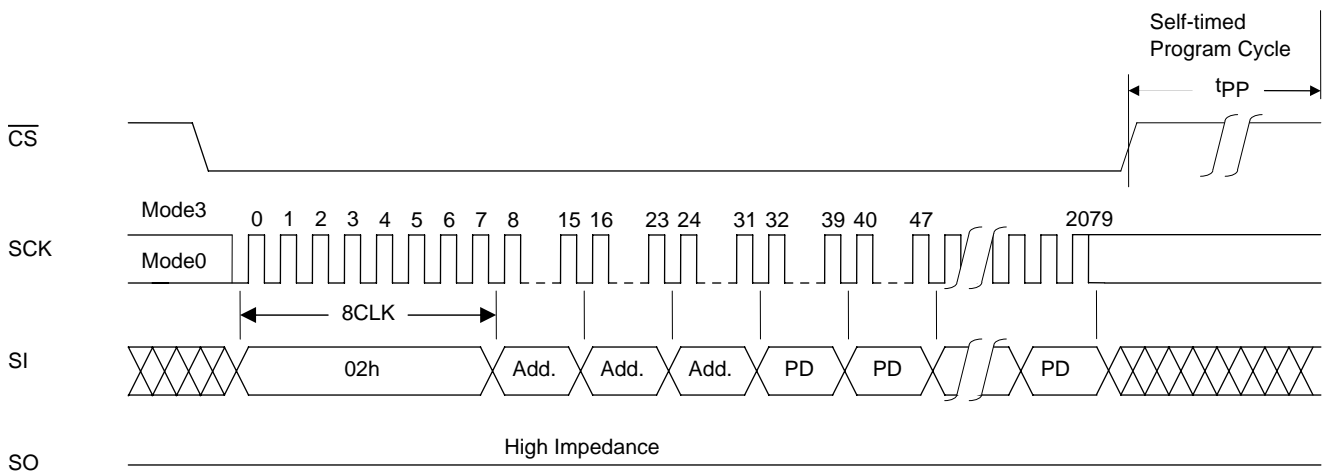
Figure 14 Chip Erase



9. Page Program

Page program is an operation that programs any number of bytes from 1 to 256 bytes within the same sector page (page addresses: A18 to A8). Before initiating page program, the data on the page concerned must be erased using small sector erase, sector erase, or chip erase. "Figure 15 Page Program" shows the page program timing waveforms, and Figure 22 shows a page program flowchart. After the falling \overline{CS} edge, the command (02H) is input followed by the 24-bit addresses. Addresses A18 to A0 are valid. The program data is then loaded at each rising clock edge until the rising \overline{CS} edge, and data loading is continued until the rising \overline{CS} edge. If the data loaded has exceeded 256 bytes, the 256 bytes loaded last are programmed. The program data must be loaded in 1-byte increments, and the program operation is not performed at the rising \overline{CS} edge occurring at any other timing. The page program time is 2.0ms (typ.) when 256 bytes (1 page) are programmed at one time.

Figure 15 Page Program



10. Silicon ID Read

Silicon ID read is an operation that reads the manufacturer code and device code information. "Table 6 Silicon ID codes table" lists the silicon ID codes. The silicon ID read command is not accepted during writing.

Two methods are used for silicon ID reading. The first method involves inputting the 9Fh command: the setting is completed with only the first bus cycle input, and in subsequent bus cycles the manufacturer code 62h and device code 1Eh are repeatedly output in succession so long as the clock input is continued. Refer to "Figure 16-a Silicon ID read 1" for the waveforms.

The second method involves inputting the ABh command. This command consists of the first through fourth bus cycles, and the silicon ID can be read when 16 dummy bits and an 8-bit address are input after (ABh). When address A0 is "0", the manufacturer code 62h is read in the fifth bus cycle, and the device code 1Eh is read in the sixth bus cycle. "Figure 16-b Silicon ID read 2" shows the timing waveforms. If, after the manufacturer code or device code has been read, the SCK input is continued, the manufacturer code and device code are output alternately with each bus cycle. When address A0 is "1", reading starts with device code 1Eh in the fifth bus cycle.

Table 6 Silicon ID Codes

| | Address A0 | Output Code |
|-------------------|------------|-------------|
| Manufacturer code | 0 | 62h |
| Device code | 1 | 1Eh |

The data is output starting with the falling clock edge of the fourth bus cycle bit 0, and silicon ID reading ends at the rising CS edge.

Figure 16-a Silicon ID Read 1

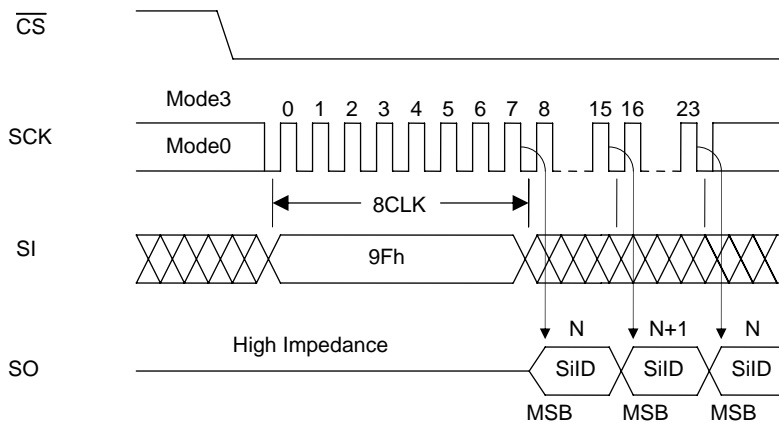
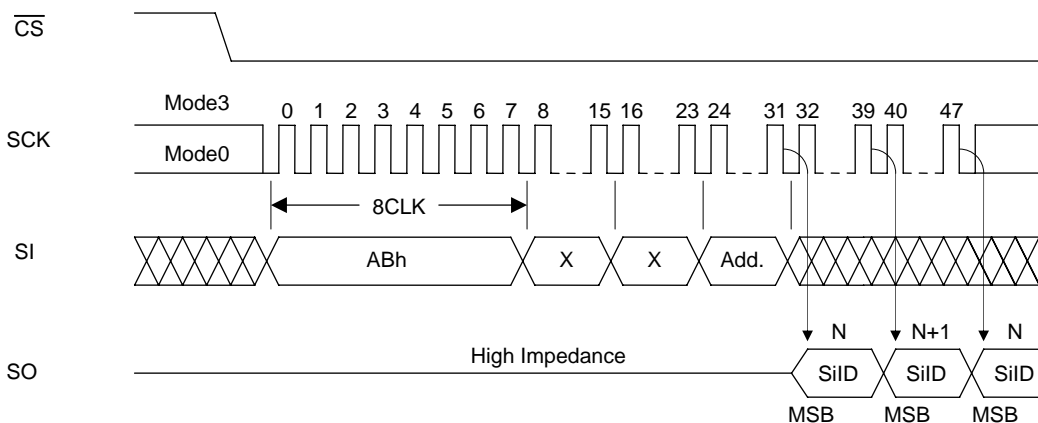


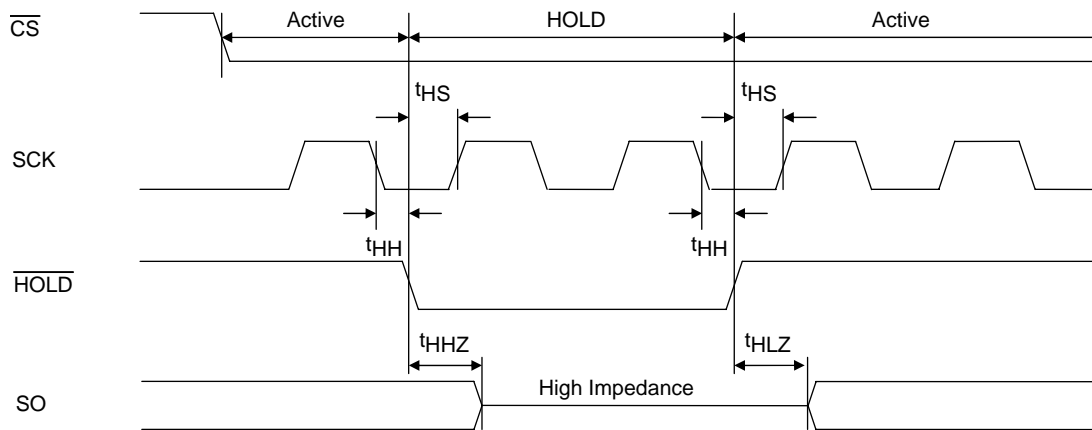
Figure 16-b Silicon ID Read 2



11. Hold Function

Using the $\overline{\text{HOLD}}$ pin, the hold function suspends serial communication (it places it in the hold status). "Figure 17 $\overline{\text{HOLD}}$ " shows the timing waveforms. The device is placed in the hold status at the falling $\overline{\text{HOLD}}$ edge while the logic level of SCK is low, and it exits from the hold status at the rising $\overline{\text{HOLD}}$ edge. When the logic level of SCK is high, $\overline{\text{HOLD}}$ must not rise or fall. The hold function takes effect when the logic level of $\overline{\text{CS}}$ is low, the hold status is exited and serial communication is reset at the rising $\overline{\text{CS}}$ edge. In the hold status, the SO output is in the high-impedance state, and SI and SCK are "don't care".

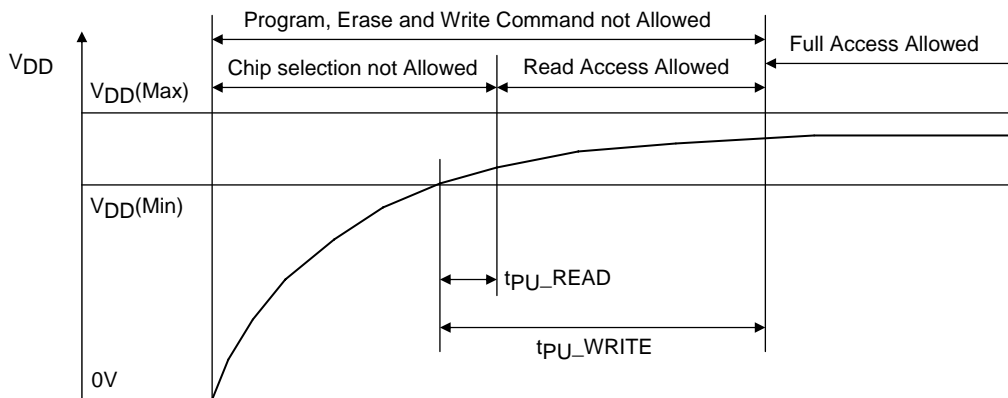
Figure 17 $\overline{\text{HOLD}}$



12. Power-on

In order to protect against unintentional writing, $\overline{\text{CS}}$ must be kept at V_{CC} At power-on. After power-on, the supply voltage has stabilized at 2.30V or higher, wait for 100 μs ($t_{\text{pU_READ}}$) before inputting the command to start a read operation. Similarly, wait for 10ms ($t_{\text{pU_WRITE}}$) after the voltage has stabilized before inputting the command to start a write operation.

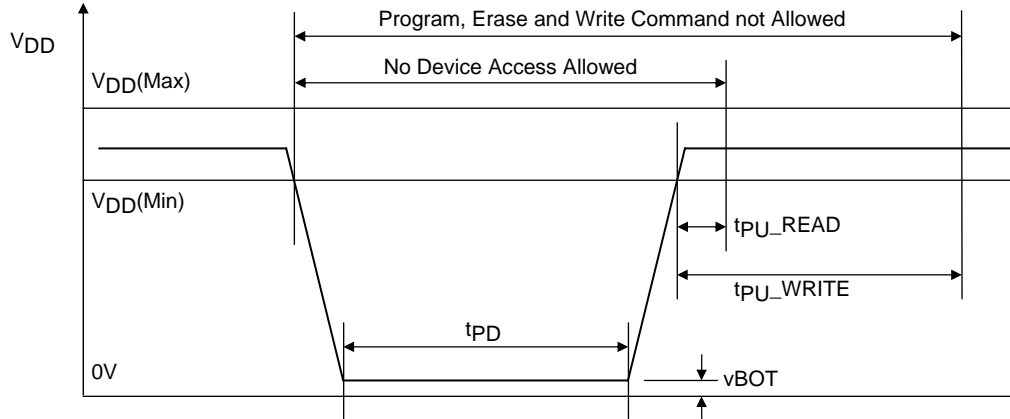
Figure 18 Power-on Timing



13. Hardware Data Protection

In order to protect against unintentional writing at power-on, the LE25FU406B incorporates a power-on reset function. The following conditions must be met in order to ensure that the power reset circuit will operate stably. No guarantees are given for data in the event of an instantaneous power failure occurring during the writing period.

Figure 19 Power-down Timing



14. Software Data Protection

The LE25FU406B eliminates the possibility of unintentional operations by not recognizing commands under the following conditions.

- When a write command is input and the rising \overline{CS} edge timing is not in a bus cycle (8 CLK units of SCK)
- When the page program data is not in 1-byte increments
- When the status register write command is input for 2 bus cycles or more

15. Decoupling Capacitor

A 0.1 μ F ceramic capacitor must be provided to each device and connected between V_{DD} and V_{SS} in order to ensure that the device will operate stably.

LE25FU406B

Specifications

Absolute Maximum Ratings

| Parameter | Symbol | Conditions | Ratings | unit |
|------------------------|--------|--------------------------|----------------------|------|
| Maximum supply voltage | | With respect to V_{SS} | -0.5 to +4.6 | V |
| DC voltage (all pins) | | With respect to V_{SS} | -0.5 to $V_{DD}+0.5$ | V |
| Storage temperature | Tstg | | -55 to +150 | °C |

Operating Conditions

| Parameter | Symbol | Conditions | Ratings | unit |
|-------------------------------|--------|------------|------------------------------------|------|
| Operating supply voltage | | | 2.30 to 3.60 | V |
| Operating ambient temperature | | | 0 to 70 | °C |
| | | | -40 to +85 (at the planning stage) | |

Allowable DC Operating Conditions

| Parameter | Symbol | Conditions | Ratings | | | unit |
|--|-----------|---|--------------|-----|--------------|------|
| | | | min | typ | max | |
| Read mode operating current | I_{CCR} | $\overline{CS}=0.1V_{DD}$, $\overline{HOLD}=\overline{WP}=0.9V_{DD}$ $SI=0.1V_{DD}/0.9V_{DD}$, $SO=open$ operating frequency=30MHz, $V_{DD}=V_{DD\ max}$ | | | 6 | mA |
| Write mode operating current (erase+page program) | I_{CCW} | $V_{DD}=V_{DD\ max}$, $t_{SSE}=40ms$, $t_{SE}=80ms$, $t_{CHE}=200ms$, $t_{pp}=2.5ms$ | | | 15 | mA |
| CMOS standby current | I_{SB} | $\overline{CS}=V_{DD}$, $\overline{HOLD}=\overline{WP}=V_{DD}$, $SI=V_{SS}/V_{DD}$, $SO=open$, $V_{DD}=V_{DD\ max}$ | | | 50 | μA |
| Power-down standby current | I_{DSB} | $\overline{CS}=V_{DD}$, $\overline{HOLD}=\overline{WP}=V_{DD}$, $SI=V_{SS}/V_{DD}$, $SO=open$, $V_{DD}=V_{DD\ max}$ | | | 10 | μA |
| Input leakage current | I_{LI} | $V_{IN}=V_{SS}$ to V_{DD} , $V_{DD}=V_{DD\ max}$ | | | 2 | μA |
| Output leakage current | I_{LO} | $V_{IN}=V_{SS}$ to V_{DD} , $V_{DD}=V_{DD\ max}$ | | | 2 | μA |
| Input low voltage | V_{IL} | $V_{DD}=V_{DD\ max}$ | -0.3 | | $0.3V_{DD}$ | V |
| Input high voltage | V_{IH} | $V_{DD}=V_{DD\ min}$ | $0.7V_{DD}$ | | $V_{DD}+0.3$ | V |
| Output low voltage | V_{OL} | $I_{OL}=100\mu A$, $V_{DD}=V_{DD\ min}$ $I_{OL}=1.6mA$, $V_{DD}=V_{DD\ min}$ | | | 0.2 0.4 | V |
| Output high voltage | V_{OH} | $I_{OH}=-100\mu A$, $V_{DD}=V_{DD\ min}$ | $V_{CC}-0.2$ | | | V |

Power-on Timing

| Parameter | Symbol | Ratings | | unit |
|---------------------------------------|-----------------|---------|-----|------|
| | | min | max | |
| Time from power-on to read operation | t_{PU_READ} | 100 | | μs |
| Time from power-on to write operation | t_{PU_WRITE} | 10 | | ms |
| Power-down time | t_{PD} | 10 | | ms |
| Power-down voltage | V_{BOT} | | 0.2 | V |

Pin Capacitance at $T_a=25^\circ C$, $f=1MHz$

| Parameter | Symbol | Conditions | Ratings | unit |
|------------------------|----------|-------------|---------|------|
| | | | max | |
| Output pin capacitance | C_{DQ} | $V_{DQ}=0V$ | 12 | pF |
| Input pin Capacitance | C_{IN} | $V_{IN}=0V$ | 6 | pF |

Note: These parameter values do not represent the results of measurements undertaken for all devices but rather values for some of the sampled devices.

LE25FU406B

AC Characteristics

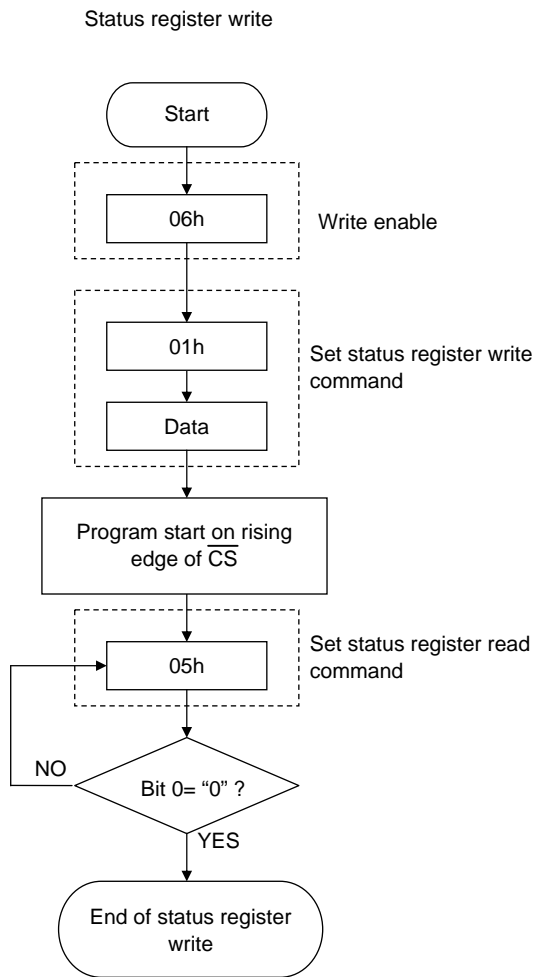
| Parameter | Symbol | Ratings | | | unit |
|--|-------------------|---------|------|------|------|
| | | min | typ | max | |
| Clock frequency | f _{CLK} | | | 30 | MHz |
| SCK logic high level pulse width | t _{CLHI} | 16 | | | ns |
| SCK logic low level pulse width | t _{CLLO} | 16 | | | ns |
| Input signal rising/falling time | t _{RF} | | | 20 | ns |
| $\overline{\text{CS}}$ setup time | t _{CSS} | 10 | | | ns |
| SCK setup time | t _{CLS} | 10 | | | ns |
| Data setup time | t _{DS} | 5 | | | ns |
| Data hold time | t _{DH} | 5 | | | ns |
| $\overline{\text{CS}}$ hold time | t _{CSH} | 10 | | | ns |
| SCK hold time | t _{CLH} | 10 | | | ns |
| $\overline{\text{CS}}$ wait pulse width | t _{CPH} | 25 | | | ns |
| Output high impedance time from $\overline{\text{CS}}$ | t _{CHZ} | | | 15 | ns |
| Output data time from SCK | t _v | | 10 | 15 | ns |
| Output data hold time | t _{HO} | 1 | | | ns |
| $\overline{\text{HOLD}}$ setup time | t _{HS} | 7 | | | ns |
| $\overline{\text{HOLD}}$ hold time | t _{HH} | 3 | | | ns |
| Output low impedance time from $\overline{\text{HOLD}}$ | t _{HLZ} | | | 9 | ns |
| Output high impedance time from $\overline{\text{HOLD}}$ | t _{HHZ} | | | 9 | ns |
| $\overline{\text{WP}}$ setup time | t _{WPS} | 20 | | | ns |
| $\overline{\text{WP}}$ hold time | t _{WPH} | 20 | | | ns |
| Write status register time | t _{SRW} | | 5 | 15 | ms |
| Page programming cycle time | t _{PP} | | 2.0 | 2.5 | ms |
| Small sector erase cycle time | t _{SSE} | | 0.04 | 0.15 | s |
| Sector erase cycle time | t _{SE} | | 0.08 | 0.25 | s |
| Chip erase cycle time | t _{CHE} | | 0.2 | 2.0 | s |
| Power-down time | t _{DP} | | | 3 | μs |
| Power-down recovery time | t _{PRB} | | | 3 | μs |
| Output low impedance time from SCK | t _{CLZ} | 0 | | | ns |

AC Test Conditions

Input pulse level..... 0V, 2.5V
 Input rising/falling time.... 5ns
 Input timing level..... 0.3V_{DD}, 0.7V_{DD}
 Output timing level 1/2×V_{DD}
 Output load 30pF

Note: As the test conditions for "typ", the measurements are conducted using 2.5V for V_{DD} at room temperature.

Figure 20 Status Register Write Flowchart



* Automatically placed in write disabled state at the end of the status register write

Figure 21 Erase Flowcharts

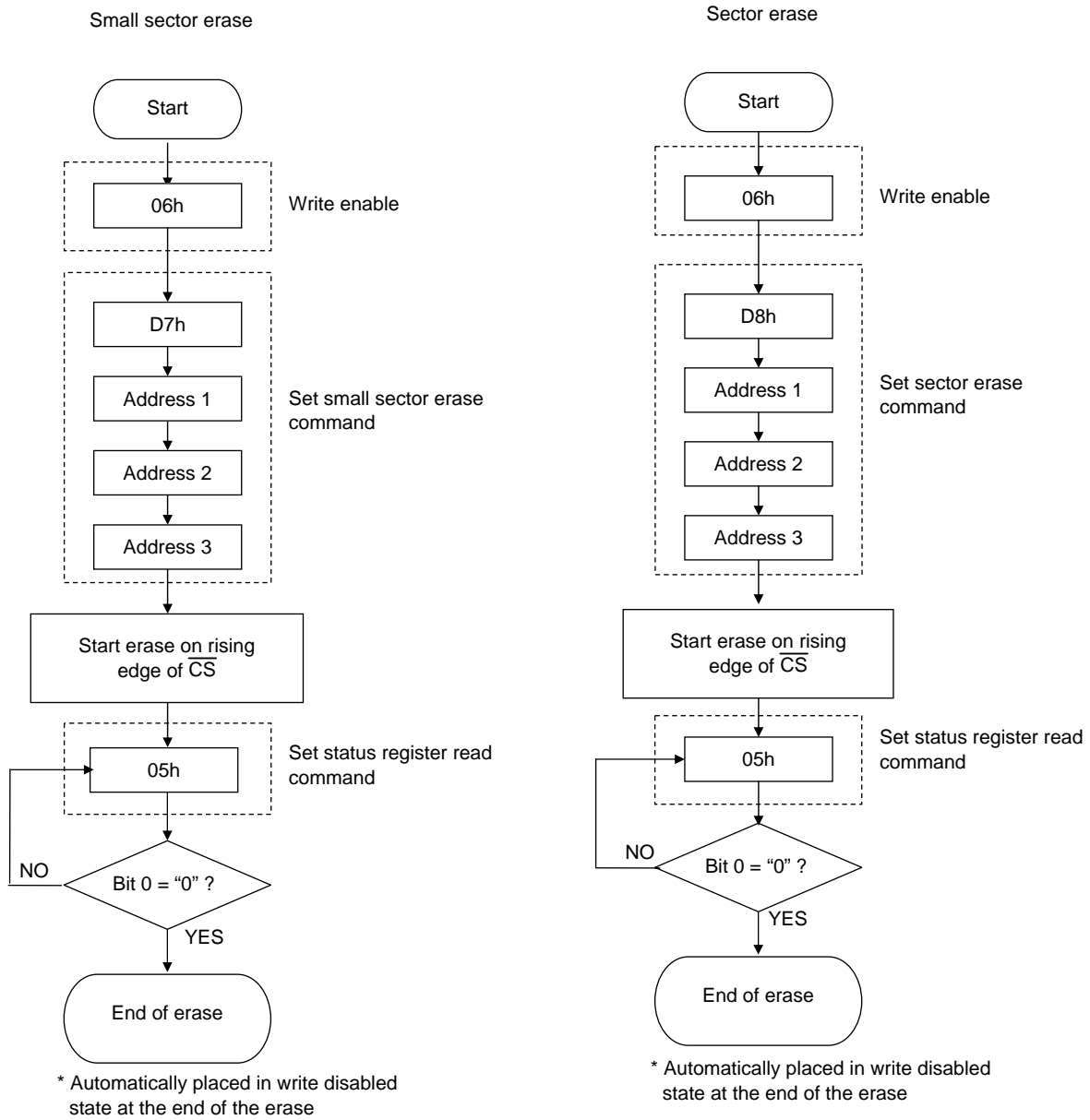
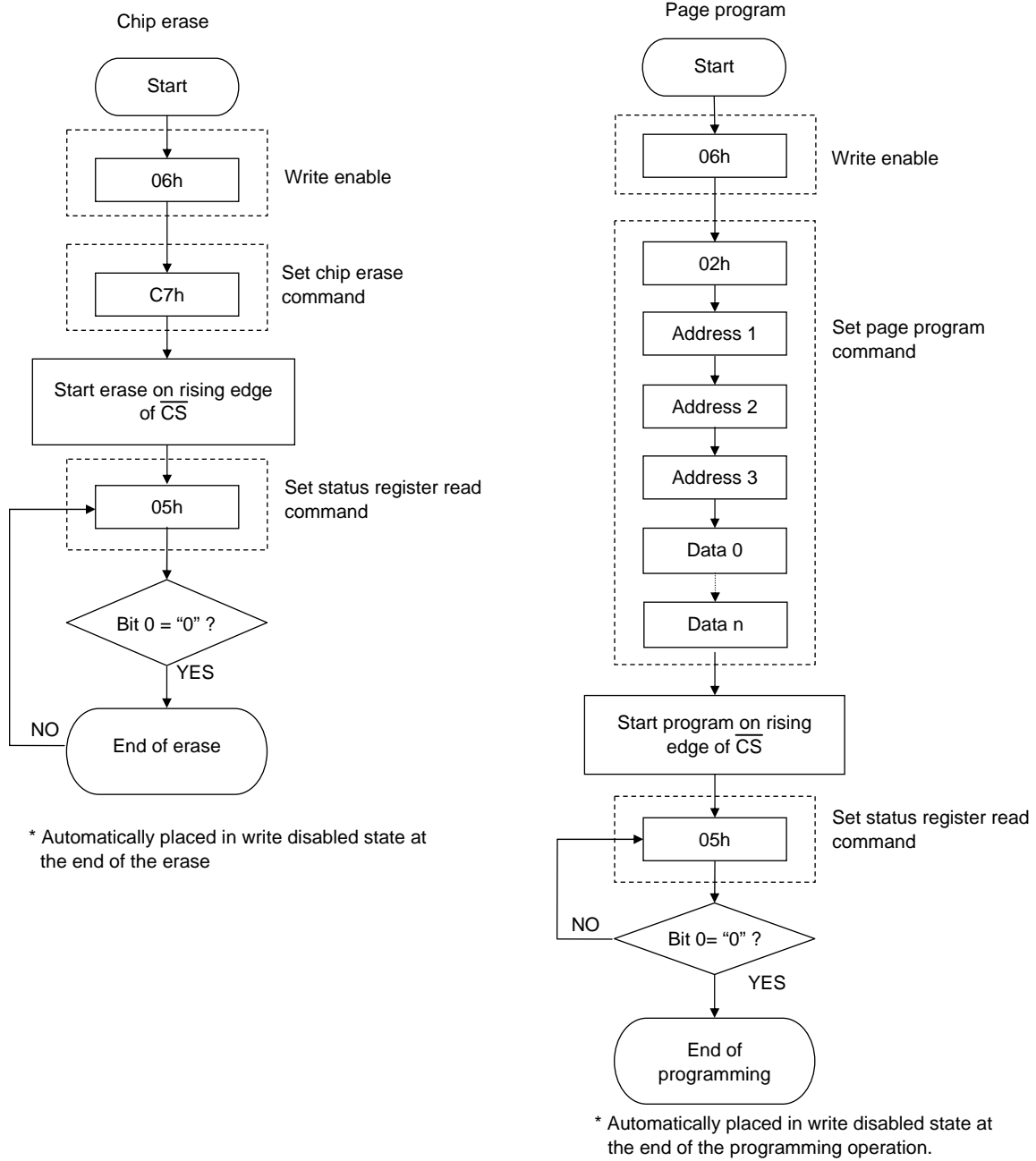


Figure 22 Page Program Flowchart



- SANYO Semiconductor Co.,Ltd. assumes no responsibility for equipment failures that result from using products at values that exceed, even momentarily, rated values (such as maximum ratings, operating condition ranges, or other parameters) listed in products specifications of any and all SANYO Semiconductor Co.,Ltd. products described or contained herein.
- SANYO Semiconductor Co.,Ltd. strives to supply high-quality high-reliability products, however, any and all semiconductor products fail or malfunction with some probability. It is possible that these probabilistic failures or malfunction could give rise to accidents or events that could endanger human lives, trouble that could give rise to smoke or fire, or accidents that could cause damage to other property. When designing equipment, adopt safety measures so that these kinds of accidents or events cannot occur. Such measures include but are not limited to protective circuits and error prevention circuits for safe design, redundant design, and structural design.
- In the event that any or all SANYO Semiconductor Co.,Ltd. products described or contained herein are controlled under any of applicable local export control laws and regulations, such products may require the export license from the authorities concerned in accordance with the above law.
- No part of this publication may be reproduced or transmitted in any form or by any means, electronic or mechanical, including photocopying and recording, or any information storage or retrieval system, or otherwise, without the prior written consent of SANYO Semiconductor Co.,Ltd.
- Any and all information described or contained herein are subject to change without notice due to product/technology improvement, etc. When designing equipment, refer to the "Delivery Specification" for the SANYO Semiconductor Co.,Ltd. product that you intend to use.
- Information (including circuit diagrams and circuit parameters) herein is for example only; it is not guaranteed for volume production.
- Upon using the technical information or products described herein, neither warranty nor license shall be granted with regard to intellectual property rights or any other rights of SANYO Semiconductor Co.,Ltd. or any third party. SANYO Semiconductor Co.,Ltd. shall not be liable for any claim or suits with regard to a third party's intellectual property rights which has resulted from the use of the technical information and products mentioned above.

This catalog provides information as of July, 2008. Specifications and information herein are subject to change without notice.