NBSG53A

2.5V/3.3V SiGe Selectable Differential Clock and Data D Flip-Flop/Clock Divider with Reset and OLS*

The NBSG53A is a multi–function differential D flip–flop (DFF) or fixed divide by 2 (DIV/2) clock generator. This is part of the GigaComm™ family of high performance Silicon Germanium products. A strappable control pin is provided to select between the two functions. The device is housed in a low profile 4x4 mm 16–pin Flip–Chip BGA (FCBGA) package.

The NBSG53A is a device with data, clock, OLS, reset, and select inputs. Differential inputs incorporate internal 50 Ω termination resistors and accept NECL (Negative ECL), PECL (Positive ECL), CMOS, CML, or LVDS. The OLS input is used to program the peak–to–peak output amplitude between 0 and 800 mV in five discrete steps. The RESET and SELECT inputs are single–ended and can be driven with either LVECL or LVCMOS input levels.

Data is transferred to the outputs on the positive edge of the clock. The differential clock inputs of the NBSG53A allow the device to also be used as a negative edge triggered device.

- Maximum Input Clock Frequency (DFF) > 8 GHz Typical (See Figures 3, 5, 7, 9, and 10)
- Maximum Input Clock Frequency (DIV/2) > 10 GHz Typical (See Figures 4, 6, 8, 9, and 10)
- 210 ps Typical Propagation Delay (OLS = FLOAT)
- 45 ps Typical Rise and Fall Times (OLS = FLOAT)
- DIV/2 Mode (Active with Select Low)
- DFF Mode (Active with Select High)
- Selectable Swing PECL Output with Operating Range: V_{CC} = 2.375 V to 3.465 V with V_{EE} = 0 V
- Selectable Swing NECL Output with NECL Inputs with Operating Range: V_{CC} = 0 V with V_{EE} = –2.375 V to –3.465 V
- Output Level Select (0 V, 200 mV, 400 mV, 600 mV, or 800 mV Peak–to–Peak Output)
- 50 Ω Internal Input Termination Resistors on all Differential Inputs

*Output Level Select

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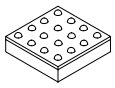


FCBGA–16
BA SUFFIX
CASE 489

MARKING DIAGRAM**

L = Wafer Lot
Y = Year
W = Work Week

**For further details, refer to Application Note AND8002/D

ORDERING INFORMATION

Device	Package	Shipping
NBSG53ABA	4x4 mm FCBGA–16	100 Units/Tray
NBSG53ABAR2	4x4 mm FCBGA–16	500/Tape & Reel

Board	Description
SG53ABAEVB	NBSG53ABA Evaluation Board

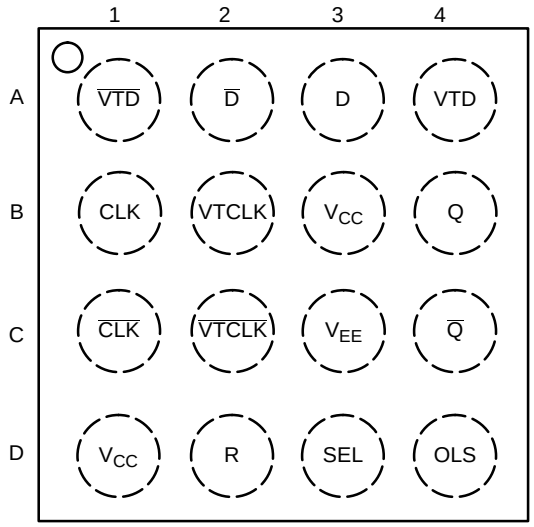


Figure 1. Pinout (Top View)

PIN DESCRIPTION

PIN	FUNCTION
D, $\overline{D}$	Data Inputs
Q, $\overline{Q}$	Data Outputs
VTD, $\overline{VTD}$, VTCLK, $\overline{VTCLK}$	50 Ω Internal Input Termination Resistor
CLK, $\overline{CLK}$	Clock Inputs
R*, SEL*	LVECL, LVCMOS Control Inputs (RESET, SELECT)
V_{CC}	Positive Supply
V_{EE}	Negative Supply
OLS	(Output Level Select) Input

* Pin will default low when left open.

OUTPUT LEVEL SELECT (OLS)

OLS	Q/$\overline{Q}$ VPP	OLS Sensitivity
V_{CC}	800 mV	OLS – 75 mV
V_{CC} – 0.4 V	200 mV	OLS ± 150 mV
V_{CC} – 0.8 V	600 mV	OLS ± 100 mV
V_{CC} – 1.2 V	0	OLS ± 75 mV
V_{EE}*	400 mV	OLS + 100 mV
Float	600 mV	N/A

* When an output level of 400 mV is desired and $V_{CC} - V_{EE} > 3.0$ V, 2.0 kΩ resistor should be connected from OLS to V_{EE}.

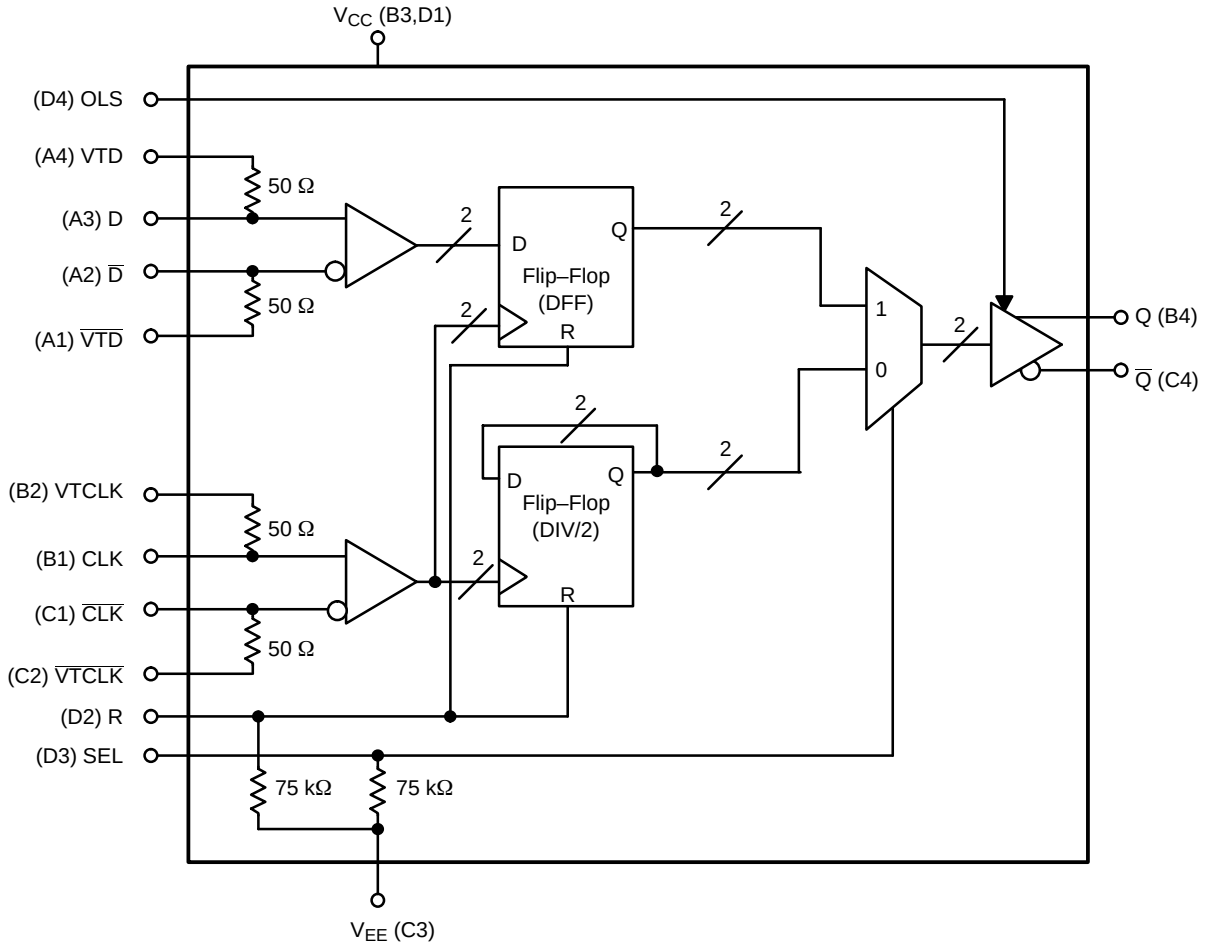


Figure 2. Simplified Logic Diagram

TRUTH TABLE

R	SEL	D	CLK	Q	Function
H	x	x	x	L	Reset
L	H	L	Z	L	DFF
L	H	H	Z	H	DFF
L	L	x	Z	$\overline{Q}$	DIV/2

Z = LOW to HIGH Transition

INTERFACING OPTIONS

INTERFACING OPTIONS	CONNECTIONS
CML	Connect VTCLK, VTD and $\overline{VTCLK}$, $\overline{VTD}$ to V_{CC}
LVDS	Connect VTCLK, VTD and $\overline{VTCLK}$, $\overline{VTD}$ Together
AC–COUPLED	Bias VTCLK, VTD and $\overline{VTCLK}$, $\overline{VTD}$ Inputs within Common Mode Range (V_{IHCMR})
RSECL, PECL, NECL	Standard ECL Termination Techniques
LVTTL, LVCMOS	An External Voltage (V_{THR}) should be Applied to the Unused Differential Input. Nominal V_{THR} is 1.5 V for LVTTL and $V_{CC}/2$ for LVCMOS Inputs. This Voltage must be within the V_{THR} Specification.

ATTRIBUTES

Characteristics	Value
Positive Operating Voltage Range for V_{CC} (V_{EE} = 0 V)	2.375 V to 3.465 V
Negative Operating Voltage Range for V_{EE} (V_{CC} = 0 V)	–2.375 V to –3.465 V
Internal Input Pulldown Resistor (R, SEL)	75 kΩ
ESD Protection Human Body Model Machine Model Charged Device Model	> 1.5 kV > 50 V > 4 kV
Moisture Sensitivity (Note 1)	Level 3
Flammability Rating	UL 94 V–0 @ 0.125 in
Oxygen Index	28 to 34
Transistor Count	482
Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test	

1. For additional information, refer to Application Note AND8003/D.

MAXIMUM RATINGS (Note 2)

Symbol	Parameter	Condition 1	Condition 2	Rating	Units
V_{CC}	Positive Power Supply	V_{EE} = 0 V		3.6	V
V_{EE}	Negative Power Supply	V_{CC} = 0 V		–3.6	V
V_I	Positive Input Negative Input	V_{EE} = 0 V V_{CC} = 0 V	$V_I \le V_{CC}$ $V_I \ge V_{EE}$	3.6 –3.6	V V
V_{INPP} (IN–IN)	Differential Input Voltage	$V_{CC} - V_{EE} \ge$ 2.8 V $V_{CC} - V_{EE} <$ 2.8 V		2.8 $\lvert V_{CC} - V_{EE} \rvert$	V V
I_{IN}	Input Current Through R_T (50 Ω Resistor)	Static Surge		45 80	mA mA
I_{OUT}	Output Current	Continuous Surge		25 50	mA mA
T_A	Operating Temperature Range			–40 to +70	°C
T_{stg}	Storage Temperature Range			–65 to +150	°C
θ_{JA}	Thermal Resistance (Junction–to–Ambient) (Note 3)	0 LFPM 500 LFPM	16 FCBGA 16 FCBGA	108 86	°C/W °C/W
θ_{JC}	Thermal Resistance (Junction–to–Case)	2S2P (Note 3)	16 FCBGA	5	°C/W
T_{sol}	Wave Solder	< 15 Seconds		225	°C

2. Maximum Ratings are those values beyond which device damage may occur.
3. JEDEC standard 51–6, multilayer board – 2S2P (2 signal, 2 power).

DC CHARACTERISTICS, INPUT WITH PECL OUTPUT V_{CC} = 2.5 V; V_{EE} = 0 V (Note 4)

Symbol	Characteristic	–40°C			25°C			70°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Power Supply Current	33	45	57	33	45	57	33	45	57	mA
V_{OH}	Output HIGH Voltage (Note 5)	1460	1510	1560	1490	1540	1590	1515	1565	1615	mV
V_{OL}	Output LOW Voltage (Note 5) ($OLS = V_{CC}$) ($OLS = V_{CC} – 0.4$ V) ($OLS = V_{CC} – 0.8$ V, OLS = FLOAT) ($OLS = V_{CC} – 1.2$ V) ($OLS = V_{EE}$)	 555 1235 775 1455 1005	 705 1295 895 1505 1095	 855 1355 1015 1555 1185	 595 1270 810 1490 1040	 745 1330 930 1540 1130	 895 1390 1050 1590 1220	 625 1295 840 1510 1065	 775 1355 960 1560 1155	 925 1415 1080 1610 1245	mV
V_{outpp}	Output p–p Voltage ($OLS = V_{CC}$) ($OLS = V_{CC} – 0.4$ V) ($OLS = V_{CC} – 0.8$ V, OLS = FLOAT) ($OLS = V_{CC} – 1.2$ V) ($OLS = V_{EE}$)	 715 125 525 0 325	 805 215 615 5 415		 705 120 520 0 320	 795 210 610 0 410		 700 120 515 0 320	 790 210 605 5 410		mV
V_{IH}	Input HIGH Voltage (Single–Ended) (Notes 7 and 9) CLK, $\overline{CLK}$, D, $\overline{D}$	V_{EE} + 1275	V_{CC} – 1000*	V_{CC}	V_{EE} + 1275	V_{CC} – 1000*	V_{CC}	V_{EE} + 1275	V_{CC}– 1000*	V_{CC}	mV
V_{IL}	Input LOW Voltage (Single–Ended) (Notes 8 and 9) CLK, $\overline{CLK}$, D, $\overline{D}$	V_{EE}	V_{CC}– 1400*	V_{IH}– 150	V_{EE}	V_{CC}– 1400*	V_{IH}– 150	V_{EE}	V_{CC}– 1400*	V_{IH}– 150	mV
V_{IH}	Input High Voltage (Single–Ended) R, SEL	1290		1615	1355		1680	1415		1740	mV
V_{IL}	Input Low Voltage (Single–Ended) R, SEL	565		890	630		955	690		1015	mV
V_{THR}	Input Threshold Voltage (Single–Ended) (Note 9)	V_{EE}+ 1125		V_{CC}– 75	V_{EE}+ 1125		V_{CC}– 75	V_{EE}+ 1125		V_{CC}– 75	mV
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential) (Note 6)	1.2		2.5	1.2		2.5	1.2		2.5	V
R_T	Internal Termination Resistor	45	50	55	45	50	55	45	50	55	Ω
I_{IH}	Input HIGH Current (@V_{IH}) R, SEL CLK, $\overline{CLK}$, D, $\overline{D}$		35 5	100 50		35 5	100 50		35 5	100 50	μA
I_{IL}	Input LOW Current (@V_{IL}) R, SEL CLK, $\overline{CLK}$, D, $\overline{D}$		20 5	100 50		20 5	100 50		20 5	100 50	μA

NOTE: GigaComm circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse airflow greater than 500 lfpm is maintained.

4. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.125 V to –0.965 V.
5. All outputs loaded with 50 Ω to V_{CC} – 2.0 volts.
6. V_{IHCMR} min varies 1:1 with V_{EE}, V_{IHCMR} max varies 1:1 with V_{CC}. The V_{IHCMR} range is referenced to the most positive side of the differential input signal.
7. V_{IH} cannot exceed V_{CC}. $|V_{IH} – V_{THR}| < 2600$ mV.
8. V_{IL} always $\geq V_{EE}$. $|V_{IL} – V_{THR}| < 2600$ mV.
9. V_{THR} is the voltage applied to one input when running in single–ended mode.

*Typicals used for testing purposes.

DC CHARACTERISTICS, INPUT WITH PECL OUTPUT V_{CC} = 3.3 V; V_{EE} = 0 V (Note 10)

Symbol	Characteristic	–40°C			25°C			70°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Power Supply Current	35	47	59	35	47	59	35	47	59	mA
V_{OH}	Output HIGH Voltage (Note 11)	2260	2310	2360	2290	2340	2390	2315	2365	2415	mV
V_{OL}	Output LOW Voltage (Note 11) (OLS = V_{CC}) (OLS = V_{CC} – 0.4 V) (OLS = V_{CC} – 0.8 V, OLS = FLOAT) (OLS = V_{CC} – 1.2 V) **(OLS = V_{EE})	 1320 2030 1550 2260 1785	 1470 2090 1670 2310 1875	 1620 2150 1790 2360 1965	 1360 2065 1585 2290 1820	 1510 2125 1705 2340 1910	 1660 2185 1825 2390 2000	 1390 2090 1615 2315 1850	 1540 2150 1735 2365 1940	 1690 2210 1855 2415 2030	mV
V_{outpp}	Output p–p Voltage (OLS = V_{CC}) (OLS = V_{CC} – 0.4 V) (OLS = V_{CC} – 0.8 V, OLS = FLOAT) (OLS = V_{CC} – 1.2 V) **(OLS = V_{EE})	 750 130 550 0 345	 840 220 640 0 435		 740 125 545 0 340	 830 215 635 0 430		 735 125 540 0 335	 825 215 630 0 425		mV
V_{IH}	Input HIGH Voltage (Single–Ended) (Notes 13 and 15) CLK, $\overline{CLK}$, D, $\overline{D}$	V_{EE} + 1275	V_{CC} – 1000*	V_{CC}	V_{EE} + 1275	V_{CC} – 1000*	V_{CC}	V_{EE} + 1275	V_{CC} – 1000*	V_{CC}	mV
V_{IL}	Input LOW Voltage (Single–Ended) (Notes 14 and 15) CLK, $\overline{CLK}$, D, $\overline{D}$	V_{IH}– 2600	V_{CC}– 1400*	V_{IH}– 150	V_{IH}– 2600	V_{CC}– 1400*	V_{IH}– 150	V_{IH}– 2600	V_{CC}– 1400*	V_{IH}– 150	mV
V_{IH}	Input High Voltage (Single–Ended) R, SEL	2090		2415	2155		2480	2215		2540	mV
V_{IL}	Input Low Voltage (Single–Ended) R, SEL	1365		1690	1430		1755	1490		1815	mV
V_{THR}	Input Threshold Voltage (Single–Ended) (Note 15)	V_{EE}+ 1125		V_{CC}– 75	V_{EE}+ 1125		V_{CC}– 75	V_{EE}+ 1125		V_{CC}– 75	mV
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential) (Note 12)	1.2		3.3	1.2		3.3	1.2		3.3	V
R_T	Internal Termination Resistor	45	50	55	45	50	55	45	50	55	Ω
I_{IH}	Input HIGH Current (@V_{IH}) R, SEL CLK, $\overline{CLK}$, D, $\overline{D}$		35 5	100 50		35 5	100 50		35 5	100 50	μA
I_{IL}	Input LOW Current (@V_{IL}) R, SEL CLK, $\overline{CLK}$, D, $\overline{D}$		20 5	100 50		20 5	100 50		20 5	100 50	μA

NOTE: GigaComm Circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse airflow greater than 500 lfpm is maintained.

10. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.925 V to –0.165 V.
11. All outputs loaded with 50 Ω to V_{CC} – 2.0 volts.
12. V_{IHCMR} min varies 1:1 with V_{EE}, V_{IHCMR} max varies 1:1 with V_{CC}. The V_{IHCMR} range is referenced to the most positive side of the differential input signal.
13. V_{IH} cannot exceed V_{CC}. $|V_{IH} – V_{THR}| < 2600$ mV.
14. V_{IL} always $\geq V_{EE}$. $|V_{IL} – V_{THR}| < 2600$ mV.
15. V_{THR} is the voltage applied to one input when running in single–ended mode.

*Typicals used for testing purposes.

**When an output level of 400 mV is desired an $V_{CC} – V_{EE} > 3.0$ V, a 2 kΩ resistor should be connected from OLS to V_{EE}.

DC CHARACTERISTICS, NECL INPUT WITH NECL OUTPUT V_{CC} = 0 V; V_{EE} = –3.465 V to –2.375 V (Note 16)

Symbol	Characteristic	–40°C			25°C			70°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Power Supply Current	35	47	59	35	47	59	35	47	59	mA
V_{OH}	Output HIGH Voltage (Note 17)	–1040	–990	–940	–1010	–960	–910	–985	–935	–885	mV
V_{OL}	Output LOW Voltage (Note 17)										mV
	–3.465 V ≤ V_{EE} ≤ –3.0 V										
	(V_{OLS} = V_{CC})	–1980	–1830	–1680	–1940	–1790	–1640	–1910	–1760	–1610	
	(V_{OLS} = V_{CC} – 0.4 V)	–1270	–1210	–1150	–1235	–1175	–1115	–1210	–1150	–1090	
	(V_{OLS} = V_{CC} – 0.8 V, OLS = FLOAT)	–1750	–1630	–1510	–1715	–1595	–1475	–1685	–1565	–1445	
	(V_{OLS} = V_{CC} – 1.2 V)	–1040	–990	–940	–1010	–960	–910	–985	–935	–885	
	**(V_{OLS} = V_{EE})	–1515	–1425	–1335	–1480	–1390	–1300	–1450	–1360	–1270	
	–3.0 V < V_{EE} ≤ –2.375 V										
	(V_{OLS} = V_{CC})	–1945	–1795	–1645	–1905	–1755	–1605	–1875	–1725	–1575	
	(V_{OLS} = V_{CC} – 0.4 V)	–1265	–1205	–1145	–1230	–1170	–1110	–1205	–1145	–1085	
	(V_{OLS} = V_{CC} – 0.8 V, OLS = FLOAT)	–1725	–1605	–1485	–1690	–1570	–1450	–1660	–1540	–1420	
	(V_{OLS} = V_{CC} – 1.2 V)	–1045	–995	–945	–1010	–960	–910	–990	–940	–890	
	(V_{OLS} = V_{EE})	–1495	–1405	–1315	–1460	–1370	–1280	–1435	–1345	–1255	
V_{outpp}	Output p–p Voltage										mV
	–3.465 V ≤ V_{EE} ≤ –3.0 V										
	(V_{OLS} = V_{CC})	750	840		740	830		735	825		
	(V_{OLS} = V_{CC} – 0.4 V)	130	220		125	215		125	215		
	(V_{OLS} = V_{CC} – 0.8 V, OLS = FLOAT)	550	640		545	635		540	630		
	(V_{OLS} = V_{CC} – 1.2 V)	0	0		0	0		0	0		
	**(V_{OLS} = V_{EE})	345	435		340	430		335	425		
	–3.0 V < V_{EE} ≤ –2.375 V										
	(V_{OLS} = V_{CC})	715	805		705	795		700	790		
	(V_{OLS} = V_{CC} – 0.4 V)	125	215		120	210		120	210		
	(V_{OLS} = V_{CC} – 0.8 V, OLS = FLOAT)	525	615		520	610		515	605		
	(V_{OLS} = V_{CC} – 1.2 V)	0	5		0	0		0	5		
	(V_{OLS} = V_{EE})	325	415		320	410		320	410		
V_{IH}	Input HIGH Voltage (Single–Ended) (Notes 19 and 21) CLK, $\overline{CLK}$, D, $\overline{D}$	V_{EE} + 1275	V_{CC} – 1000*	V_{CC}	V_{EE} + 1275	V_{CC} – 1000*	V_{CC}	V_{EE} + 1275	V_{CC} – 1000*	V_{CC}	mV
V_{IL}	Input LOW Voltage (Single–Ended) (Notes 20 and 21) CLK, $\overline{CLK}$, D, $\overline{D}$	V_{IH}– 2600	V_{CC}– 1400*	V_{IH}– 150	V_{IH}– 2600	V_{CC}– 1400*	V_{IH}– 150	V_{IH}– 2600	V_{CC}– 1400*	V_{IH}– 150	mV
V_{IH}	Input High Voltage (Single–Ended) R, SEL	–1210		–885	–1145		–820	–1085		–760	mV
V_{IL}	Input Low Voltage (Single–Ended) R, SEL	–1935		–1610	–1870		–1545	–1810		–1485	mV
V_{THR}	Input Threshold Voltage (Single–Ended) (Note 21)	V_{EE}+ 1125		V_{CC}– 75	V_{EE}+ 1125		V_{CC}– 75	V_{EE}+ 1125		V_{CC}– 75	mV
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential) (Note 18)	V_{EE} + 1.2		0.0	V_{EE} + 1.2		0.0	V_{EE} + 1.2		0.0	V
I_{IH}	Input HIGH Current (@V_{IH})										μA
	R, SEL		35	100		35	100		35	100	
	CLK, $\overline{CLK}$, D, $\overline{D}$		5	50		5	50		5	50	

NOTE: GigaComm circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse airflow greater than 500 lfpm is maintained.

16. Input and output parameters vary 1:1 with V_{CC}.
17. All outputs loaded with 50 Ω to V_{CC} – 2.0 volts.
18. V_{IHCMR} min varies 1:1 with V_{EE}, V_{IHCMR} max varies 1:1 with V_{CC}. The V_{IHCMR} range is referenced to the most positive side of the differential input signal.
19. V_{IH} cannot exceed V_{CC}. $|V_{IH} – V_{THR}| < 2600$ mV.
20. V_{IL} always ≥ V_{EE}. $|V_{IL} – V_{THR}| < 2600$ mV.
21. V_{THR} is the voltage applied to one input when running in single–ended mode.

*Typicals used for testing purposes.

**When an output level of 400 mV is desired an $V_{CC} – V_{EE} > 3.0$ V, a 2 kΩ resistor should be connected from OLS to V_{EE}.

DC CHARACTERISTICS, NECL INPUT WITH NECL OUTPUT V_{CC} = 0 V; V_{EE} = –3.465 V to –2.375 V (Note 16)

Symbol	Characteristic	–40°C			25°C			70°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{IL}	Input LOW Current (@V_{IL})										μA
	R, SEL		20	100		20	100		20	100	
	CLK, $\overline{CLK}$, D, $\overline{D}$		5	50		5	50		5	50	
I_{OLS}	OLS Input Current (See Figure 11)										μA
	(OLS = V_{CC})		300	900		300	900		300	900	
	(OLS = V_{CC} – 0.4 V)		100	300		100	300		100	300	
	(OLS = V_{CC} – 0.8 V, OLS = FLOAT)		5	100		5	100		5	100	
	(OLS = V_{CC} – 1.2 V)	–300	–100		–300	–100		–300	–100		
	–3.465 V ≤ V_{EE} ≤ –3.0 V										
	*(OLS = V_{EE})	–1500	–600		–1500	–600		–1500	–600		
	–3.0 V < V_{EE} ≤ –2.375 V										
	(OLS = V_{EE})	–1000	–400		–1000	–400		–1000	–400		

NOTE: GigaComm circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse airflow greater than 500 lfpm is maintained.

16. Input and output parameters vary 1:1 with V_{CC}.
17. All outputs loaded with 50 Ω to V_{CC} – 2.0 volts.
18. V_{IHCMR} min varies 1:1 with V_{EE}, V_{IHCMR} max varies 1:1 with V_{CC}. The V_{IHCMR} range is referenced to the most positive side of the differential input signal.
19. V_{IH} cannot exceed V_{CC}. $|V_{IH} – V_{THR}| < 2600$ mV.
20. V_{IL} always ≥ V_{EE}. $|V_{IL} – V_{THR}| < 2600$ mV.
21. V_{THR} is the voltage applied to one input when running in single–ended mode.

*Typicals used for testing purposes.

**When an output level of 400 mV is desired an $V_{CC} – V_{EE} > 3.0$ V, a 2 kΩ resistor should be connected from OLS to V_{EE}.

AC CHARACTERISTICS V_{CC} = 0 V; V_{EE} = –3.465 V to –2.375 V or V_{CC} = 2.375 V to 3.465 V; V_{EE} = 0 V

		–40°C			25°C			70°C			
Symbol	**Characteristic**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
f_{max}	Maximum Frequency (See Figures 3, 5, 7, 9, and 10) DFF (See Figures 4, 6, 8, 9, and 10) (Note 22) DIV/2		> 8 > 10			> 8 > 10			> 8 > 10		GHz
t_{PLH}, t_{PHL}	Propagation Delay to Output Differential CLK→Q, $\overline{Q}$										ps
	(OLS = V_{CC})	160	210	260	160	215	270	165	220	275	
	(OLS = V_{CC} – 0.4 V)	150	200	250	155	205	255	160	210	260	
	(OLS = V_{CC} – 0.8 V, OLS = FLOAT)	155	205	255	160	210	260	160	215	270	
	**(OLS = V_{EE})	155	205	255	160	210	260	160	215	270	
	SEL→Q, $\overline{Q}$										
	(OLS = V_{CC})	165	220	275	170	225	280	170	225	280	
	(OLS = V_{CC} – 0.4 V)	160	210	260	160	210	260	160	210	260	
	(OLS = V_{CC} – 0.8 V, OLS = FLOAT)	160	215	270	165	220	275	165	220	275	
	**(OLS = V_{EE})	160	210	260	160	215	270	165	220	275	
	R→Q, $\overline{Q}$										
	(OLS = V_{CC}) DIV/2	220	295	370	225	300	375	225	300	375	
	(OLS = V_{CC}) DFF	200	270	340	205	275	345	205	275	345	
	(OLS = V_{CC} – 0.4 V) DIV/2	215	285	355	220	290	360	220	290	360	
	(OLS = V_{CC} – 0.4 V) DFF	195	260	325	200	265	330	200	265	330	
	(OLS = V_{CC} –0.8 V, OLS = FLOAT) DIV/2	220	290	360	220	295	370	220	295	370	
	(OLS = V_{CC} – 0.8 V, OLS = FLOAT) DFF	200	265	330	200	270	340	200	270	340	
	**(OLS = V_{EE}) DIV/2	215	285	355	220	290	360	220	290	360	
	**(OLS = V_{EE}) DFF	195	260	325	200	265	330	200	265	330	
t_{SKEW}	Duty Cycle Skew (Notes 23 and 25) DFF		5	20		5	20		5	20	ps
t_{JITTER}	Output Random Jitter (RMS) DFF (See Figures 3 and 5) (Note 22)		0.5	< 1.5		0.5	< 1.5		0.5	< 1.5	ps
V_{INPP}	Input Voltage Swing/Sensitivity (Differential) (Note 24)	75		2600	75		2600	75		2600	mV
t_r t_f	Output Rise/Fall Times (20% – 80%) Q, $\overline{Q}$										ps
	(OLS = V_{CC})	30	50	65	30	50	65	30	50	65	
	(OLS = V_{CC} – 0.4 V)	20	40	60	20	40	60	20	40	60	
	(OLS = V_{CC} – 0.8 V, OLS = FLOAT)	25	45	65	25	45	65	25	45	65	
	**(OLS = V_{EE})	25	45	65	25	45	65	25	45	65	
t_s	Setup Time D→CLK	30	14		30	10		30	13		ps
t_h	Hold Time D→CLK	25	12		25	7		25	9		ps
t_{rr}	Reset Recovery DFF, DIV/2	40	9		40	12		40	10		ps

22. Measured using a 500 mV source, 50% duty cycle clock source. Repetitive 1010 input data pattern. All outputs loaded with 50 Ω to V_{CC} – 2.0 V.
23. See Figure 13. $t_{SKEW} = |t_{PLH} – t_{PHL}|$ for a nominal 50% differential clock input waveform.
24. V_{INPP} (MAX) cannot exceed $V_{CC} – V_{EE}$ (Applicable only when $V_{CC} – V_{EE}$ < 2600 mV).
25. See Figure 9. Duty Cycle % vs. Frequency.

**When an output level of 400 mV is desired an $V_{CC} – V_{EE}$ > 3.0 V, a 2 kΩ resistor should be connected from OLS to V_{EE}.

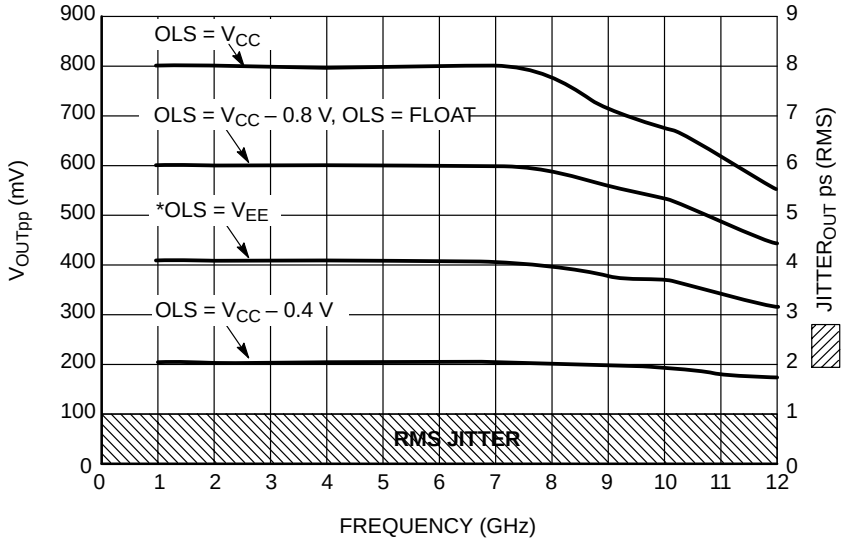


Figure 3. V_{OUT}/Jitter vs. Frequency for DFF Mode (V_{CC} − V_{EE} = 3.3 V @ 25°C; Repetitive 1010 Input Data Pattern)

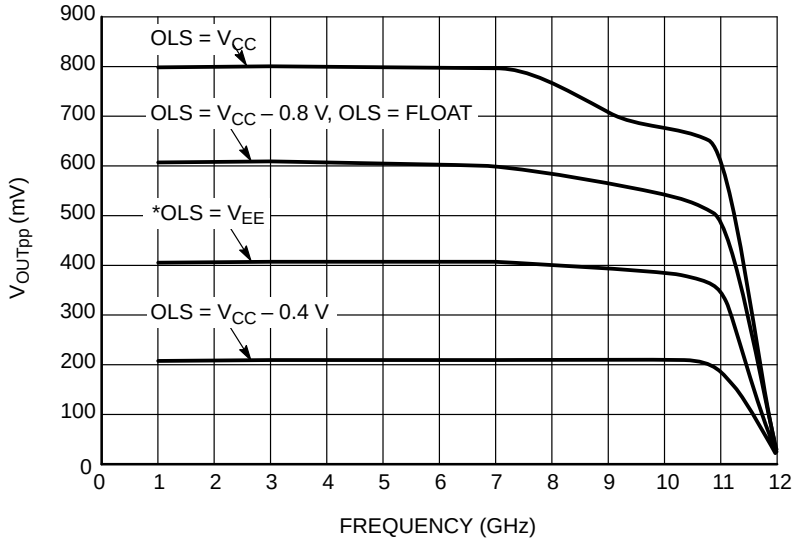


Figure 4. V_{OUT} vs. Frequency for DIV/2 Mode (V_{CC} − V_{EE} = 3.3 V @ 25°C)

*When an output level of 400 mV is desired an V_{CC} – V_{EE} > 3.0 V, a 2 kΩ resistor should be connected from OLS to V_{EE}.

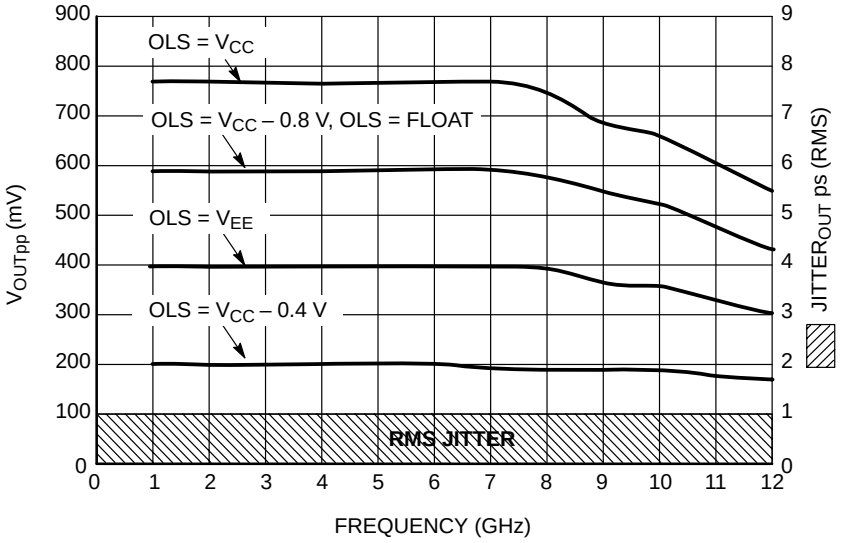


Figure 5. V_{OUT}/Jitter vs. Frequency for DFF Mode (V_{CC} − V_{EE} = 2.5 V @ 25°C; Repetitive 1010 Input Data Pattern)

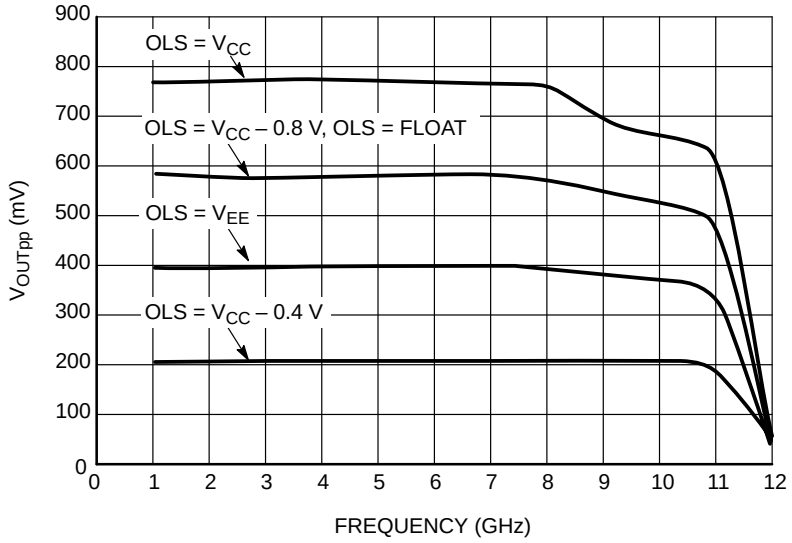


Figure 6. V_{OUT} vs. Frequency for DIV/2 Mode (V_{CC} − V_{EE} = 2.5 V @ 25°C)

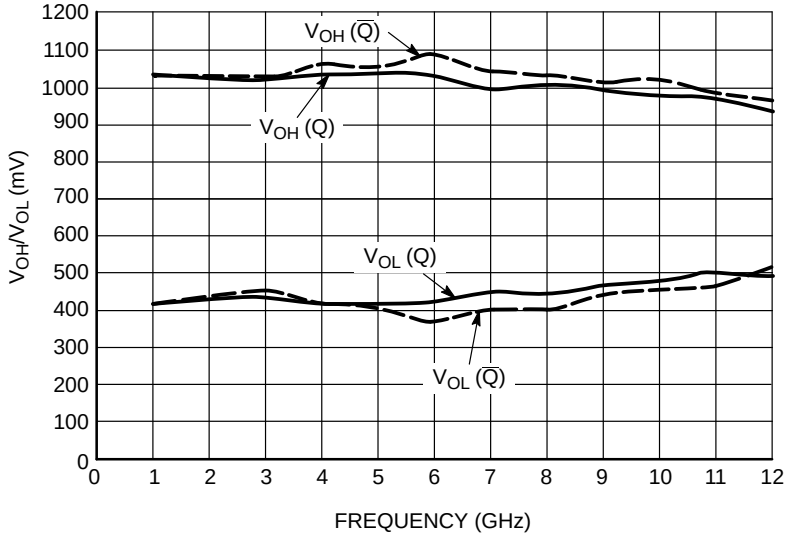


Figure 7. V_{OH}/V_{OL} (Q/$\overline{Q}$) vs. Frequency for DFF Mode ($V_{CC} - V_{EE}$ = 3.3 V @ 25°C and OLS = V_{CC} − 0.8 V, OLS = FLOAT)

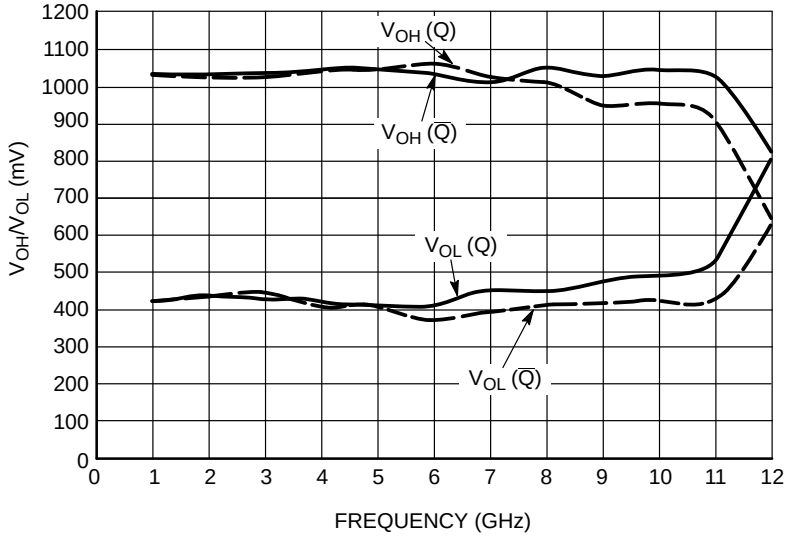


Figure 8. V_{OH}/V_{OL} (Q/$\overline{Q}$) vs. Frequency for DIV/2 Mode ($V_{CC} - V_{EE}$ = 3.3 V @ 25°C and OLS = V_{CC} − 0.8 V, OLS = FLOAT)

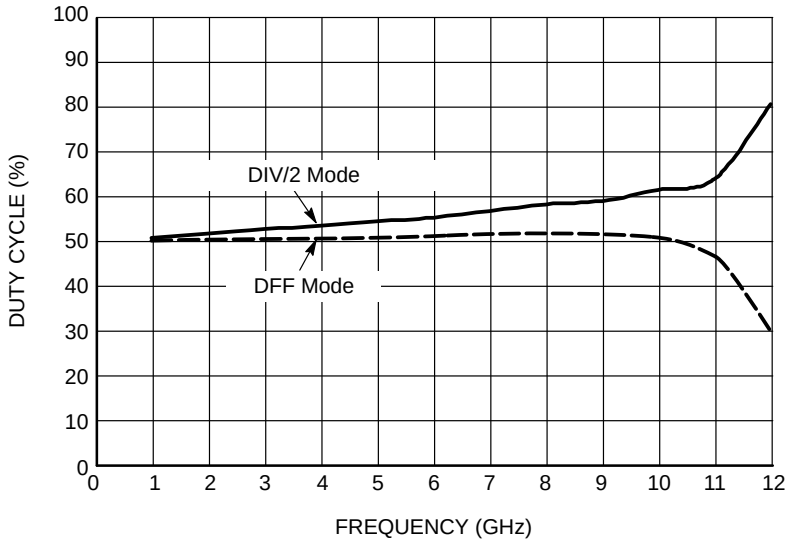


Figure 9. Duty Cycle % vs. Frequency
(V_{CC} − V_{EE} = 3.3 V @ 25°C)

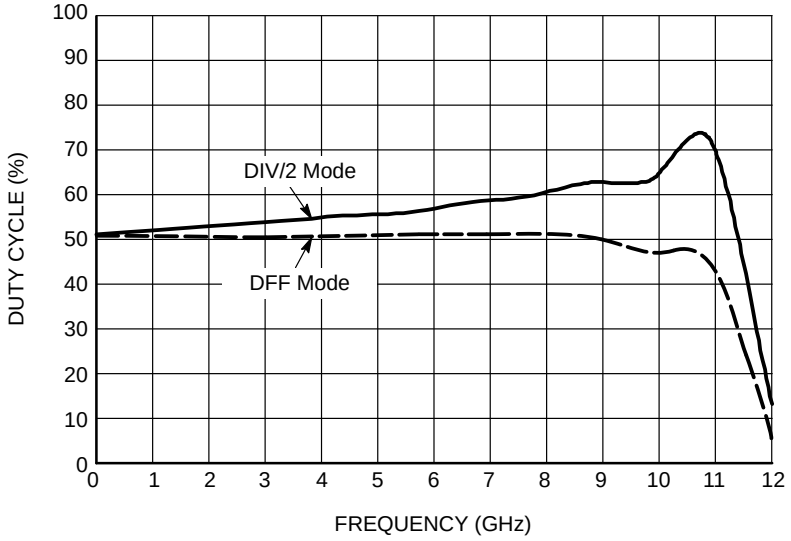


Figure 10. Duty Cycle % vs. Frequency
(V_{CC} − V_{EE} = 2.5 V @ 70°C)

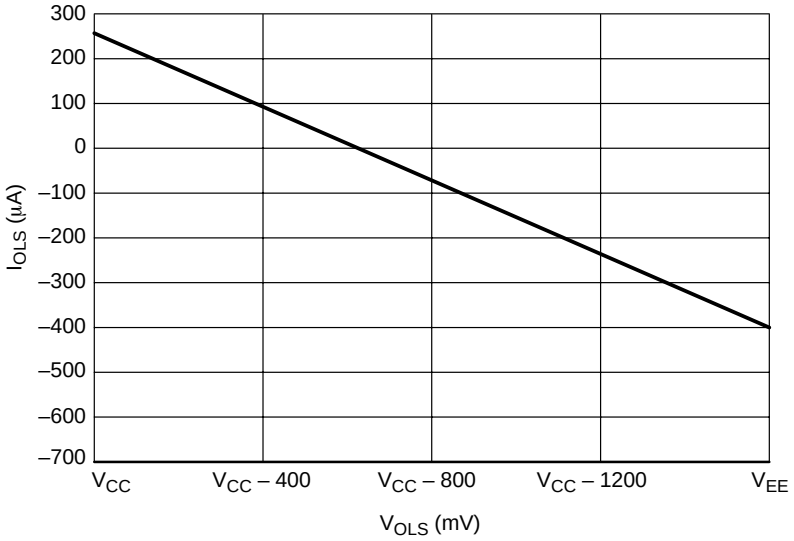


Figure 11. Typical OLS Input Current vs. OLS Input Voltage (V_{CC} − V_{EE} = 3.3 V @ 25°C)

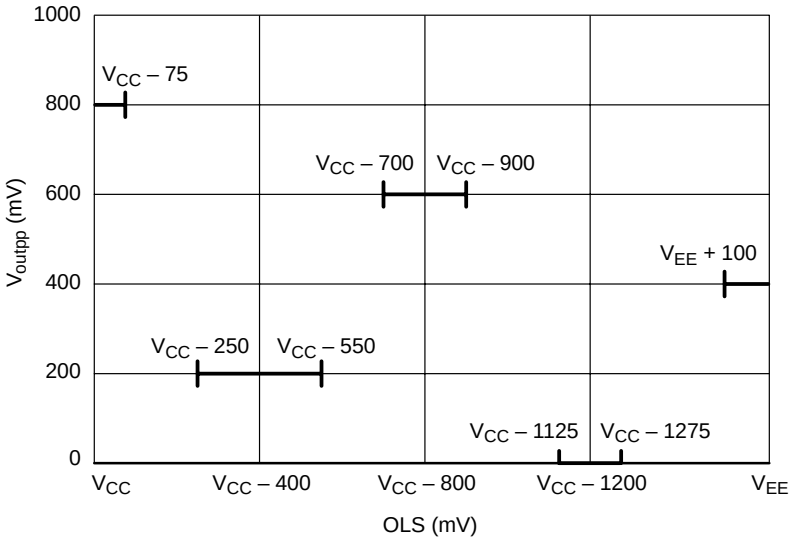


Figure 12. OLS Operating Area

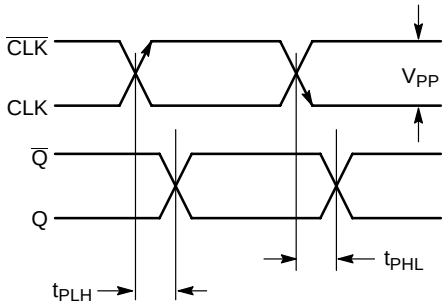


Figure 13. AC Reference Measurement

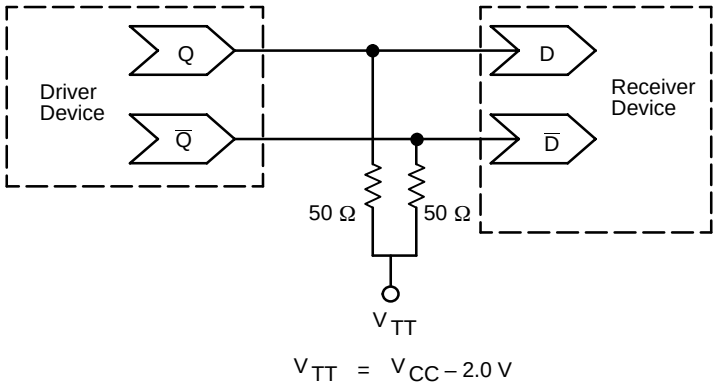
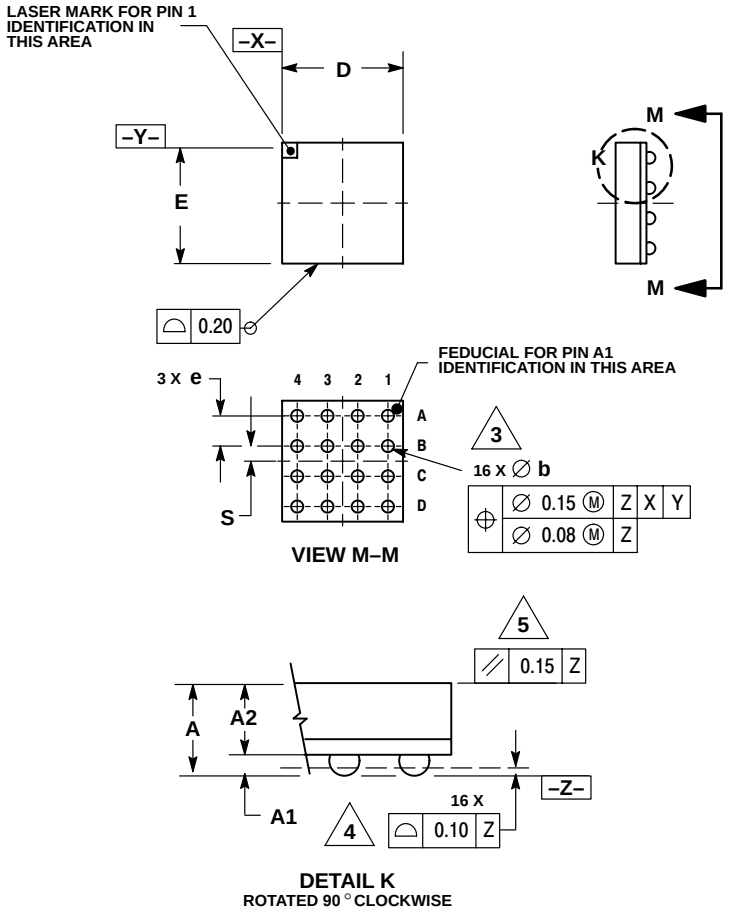


Figure 14. Typical Termination for Output Driver and Device Evaluation (Refer to Application Note AND8020 – Termination of ECL Logic Devices)

PACKAGE DIMENSIONS

FCBGA–16
BA SUFFIX
PLASTIC 4 X 4 (mm) BGA FLIP CHIP PACKAGE
CASE 489–01
ISSUE O



NOTES:
1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DIMENSION b IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO DATUM PLANE Z.
4. DATUM Z (SEATING PLANE) IS DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
5. PARALLELISM MEASUREMENT SHALL EXCLUDE ANY EFFECT OF MARK ON TOP SURFACE OF PACKAGE.

	MILLIMETERS	
DIM	MIN	MAX
A	1.40 MAX	
A1	0.25	0.35
A2	1.20 REF	
b	0.30	0.50
D	4.00 BSC	
E	4.00 BSC	
e	1.00 BSC	
S	0.50 BSC	

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