Rad-Hard 16 Channel BiCMOS Analog Multiplexer with High-Z Analog Input Protection

HS-1840ARH, HS-1840AEH, HS-1840BRH, HS-1840BEH

The HS-1840ARH, HS-1840AEH, HS-1840BRH and HS-1840BEH are radiation hardened, monolithic 16 channel multiplexers constructed with the Intersil Rad-Hard Silicon Gate, bonded wafer, Dielectric Isolation process. They are designed to provide a high input impedance to the analog source if device power fails (open), or the analog signal voltage inadvertently exceeds the supply by up to ±35V, regardless of whether the device is powered on or off. Excellent for use in redundant applications, since the secondary device can be operated in a standby unpowered mode affording no additional power drain. More significantly, a very high impedance exists between the active and inactive devices preventing any interaction. One of sixteen channel selections is controlled by a 4-bit binary address plus an Enable-Inhibit input which conveniently controls the ON/OFF operation of several multiplexers in a system. All inputs have electrostatic discharge protection. The HS-1840ARH, HS-1840AEH, HS-1840BRH and HS-1840BEH are processed and screened in full compliance with MIL-PRF-38535 and QML standards. The devices are available in a 28 Ld SBDIP and a 28 Ld Ceramic Flatpack.

Specifications for Rad Hard QML devices are controlled by the Defense Logistics Agency Land and Maritime (DLA). The SMD numbers listed here must be used when ordering.

Detailed Electrical Specifications for these devices are contained in SMD 5962-95630. A "hot-link" is provided on our homepage for downloading:
http://www.landandmaritime.dla.mil/Downloads/MilSpec/Smd/95630.pdf

Features

- Electrically Screened to SMD # 5962-95630
- QML Qualified per MIL-PRF-38535 Requirements
- Pin-to-Pin for Intersil's HS-1840RH and HS-1840/883S
- Improved Radiation Performance
  - Gamma Dose (γ) $3x10^5$RAD(Si)
- Improved $r_{DS(ON)}$ Linearity
- Improved Access Time 1.5µs (Max) Over Temp and Post Rad
- High Analog Input Impedance 500MΩ During Power Loss (Open)
- ±35V Input Overvoltage Protection (Power On or Off)
- Dielectrically Isolated Device Islands
- Excellent in Hi-Rel Redundant Systems
- Break-Before-Make Switching
- No Latch-Up

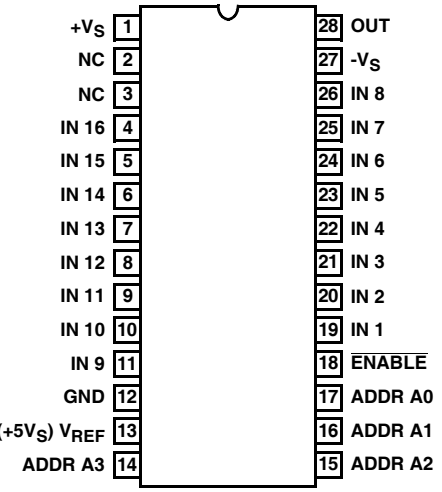
Ordering Information

ORDERING NUMBER	INTERNAL MKT. NUMBER (Note)	TEMP. RANGE (°C)	PART MARKING NO.	PACKAGE (RoHS Compliant)
5962F9563002QXC	HS1-1840ARH-8	-55 to +125	Q 5962F95 63002QXC	28 Ld SBDIP
5962F9563002QYC	HS9-1840ARH-8	-55 to +125	Q 5962F95 63002QYC	28 Ld Flatpack
5962F9563002VXC	HS1-1840ARH-Q	-55 to +125	Q 5962F95 63002VXC	28 Ld SBDIP
5962F9563002VYC	HS9-1840ARH-Q	-55 to +125	Q 5962F95 63002VYC	28 Ld Flatpack
HS1-1840ARH/PROTO	HS1-1840ARH/PROTO	-55 to +125	HS1- 1840ARH /PROTO	28 Ld SBDIP
HS9-1840ARH/PROTO	HS9-1840ARH/PROTO	-55 to +125	HS9- 1840ARH /PROTO	28 Ld Flatpack
HS1-1840ARH-T	HS1-1840ARH-T	-55 to +125	Q 5962R95 63002TXC	28 Ld SBDIP
5962F9563002V9A	HS0-1840ARH-Q	-55 to +125		
5962F9563004V9A	HS0-1840AEH-Q	-55 to +125		
5962F9563004VXC	HS1-1840AEH-Q	-55 to +125	Q 5962F95 63004VXC	28 Ld SBDIP
5962F9563004VYC	HS9-1840AEH-Q	-55 to +125	Q 5962F95 63004VYC	28 Ld Flatpack
5962F9563005V9A	HS0-1840BEH-Q	-55 to +125		
5962F9563005VXC	HS1-1840BEH-Q	-55 to +125	Q 5962F95 63005VXC	28 Ld SBDIP
5962F9563005VYC	HS9-1840BEH-Q	-55 to +125	Q 5962F95 63005VYC	28 Ld Flatpack
5962F9563003QXC	HS1-1840BRH-8	-55 to +125	Q 5962F95 63003QXC	28 Ld SBDIP
5962F9563003QYC	HS9-1840BRH-8	-55 to +125	Q 5962F95 63003QYC	28 Ld Flatpack
5962F9563003VXC	HS1-1840BRH-Q	-55 to +125	Q 5962F95 63003VXC	28 Ld SBDIP
5962F9563003VYC	HS9-1840BRH-Q	-55 to +125	Q 5962F95 63003VYC	28 Ld Flatpack
HS1-1840BRH/PROTO	HS1-1840BRH/PROTO	-55 to +125	HS1- 1840BRH /PROTO	28 Ld SBDIP
HS9-1840BRH/PROTO	HS9-1840BRH/PROTO	-55 to +125	HS9- 1840BRH /PROTO	28 Ld Flatpack
5962F9563003V9A	HS0-1840BRH-Q	-55 to +125		

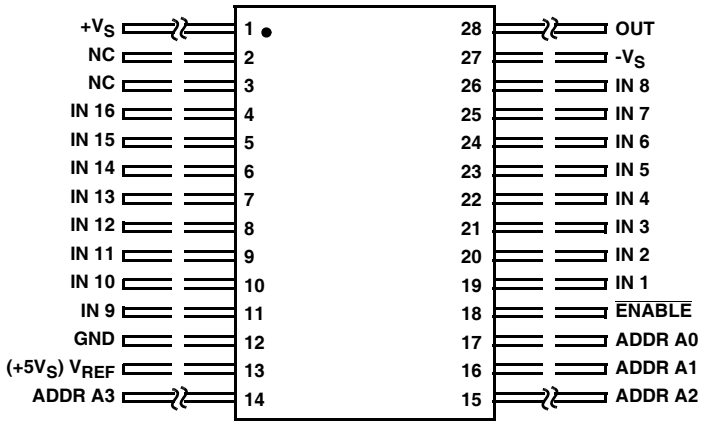
NOTE: These Intersil Pb-free Hermetic packaged products employ 100% Au plate - e4 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations.

Pin Configurations

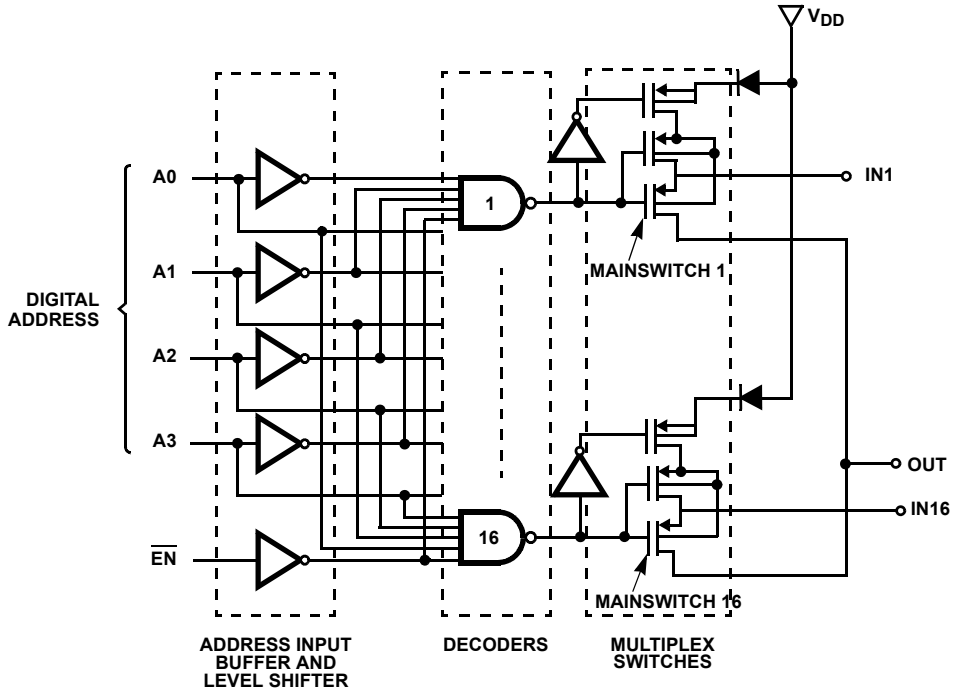
HS1-1840ARH, HS1-1840AEH, HS1-1840BRH
(28 LD SBDIP) CDIP2-T28
TOP VIEW



HS9-1840ARH, HS9-1840AEH, HS9-1840BRH
(28 LD FLATPACK) CDFP3-F28
TOP VIEW



Functional Diagram

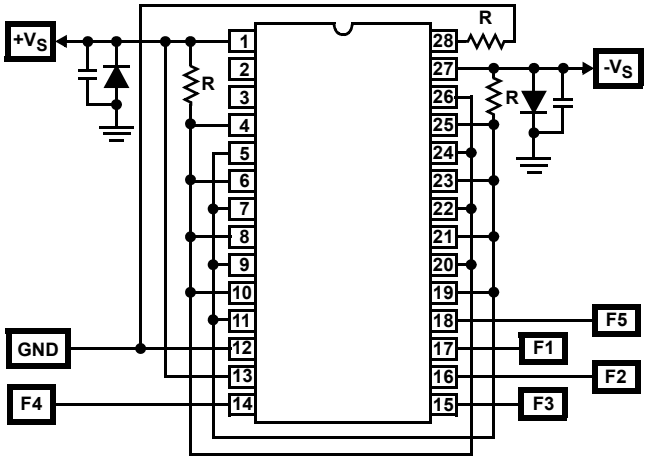


NOTE: MAINSWITCH INXX: SWITCH ON, BODY TIED TO SOURCE
SWITCH OFF, BODY TIED TO VCC-0.7V

TABLE 1. TRUTH TABLE

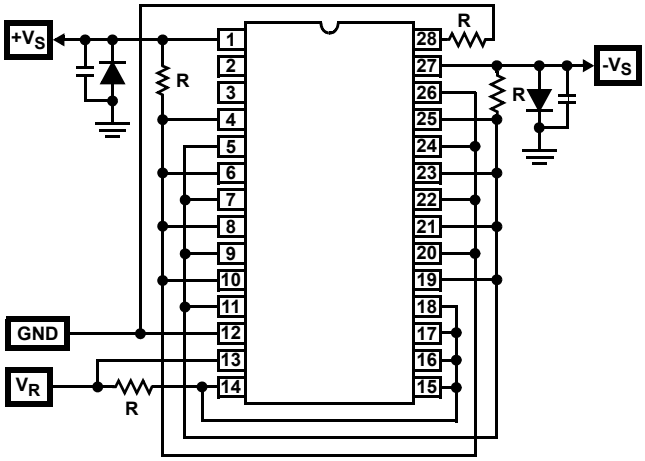
A3	A2	A1	A0	$\overline{EN}$	"ON" CHANNEL
X	X	X	X	H	None
L	L	L	L	L	1
L	L	L	H	L	2
L	L	H	L	L	3
L	L	H	H	L	4
L	H	L	L	L	5
L	H	L	H	L	6
L	H	H	L	L	7
L	H	H	H	L	8
H	L	L	L	L	9
H	L	L	H	L	10
H	L	H	L	L	11
H	L	H	H	L	12
H	H	L	L	L	13
H	H	L	H	L	14
H	H	H	L	L	15
H	H	H	H	L	16

Burn-In/Life Test Circuits



NOTE:
V_S+ = +15.5V ±0.5V, V_S- = -15.5V ±0.5V.
R = 1kΩ ±5%.
$C_1 = C_2$ = 0.01µF ±10%, 1 EACH PER SOCKET, MINIMUM.
$D_1 = D_2$ = 1N4002, 1 EACH PER BOARD, MINIMUM.
INPUT SIGNALS:
SQUARE WAVE, 50% DUTY CYCLE, 0V TO 15V PEAK ±10%.
F1 = 100kHz; F2 = F1/2; F3 = F1/4; F4 = F1/8; F5 = F1/16.

FIGURE 1. DYNAMIC BURN-IN AND LIFE TEST CIRCUIT



NOTE:
R = 1kΩ ±5%, 1/4W.
$C_1 = C_2$ = 0.01µF MINIMUM, 1 EACH PER SOCKET, MINIMUM.
V_S+ = 15.5V ±0.5V, V_S- = -15.5V ±0.5V, V_R = 15.5 ±0.5V

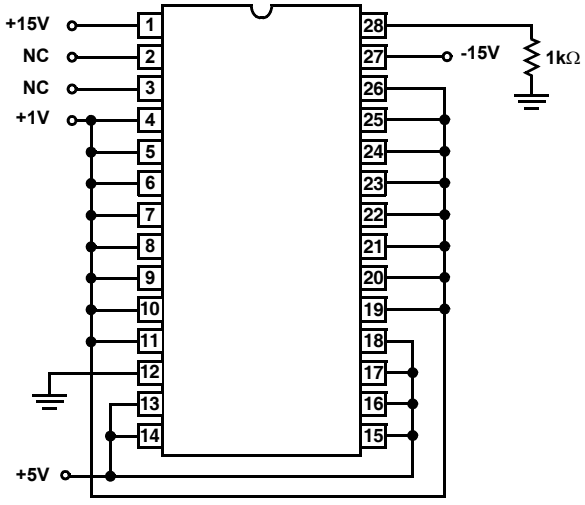
FIGURE 2. .STATIC BURN-IN TEST CIRCUIT

NOTES:

1. The above test circuits are utilized for all package types.
2. The Dynamic Test Circuit is utilized for all life testing.

Irradiation Circuit

HS-1840ARH, HS-1840AEH, HS-1840BRH



NOTE:

3. All irradiation testing is performed in the 28 lead CERDIP package.

Die Characteristics

DIE DIMENSIONS:

(2820µmx4080µm x 483µm ±25.4µm)
111 milsx161 milsx19 mils ±1 mil

INTERFACE MATERIALS:

Glassivation:

Type: PSG (Phosphorus Silicon Glass)
Thickness: 8.0kÅ ±1kÅ

Top Metallization:

Type: AlSiCu
Thickness: 16.0kÅ ±2kÅ

Backside Finish:

Silicon

ASSEMBLY RELATED INFORMATION:

Substrate Potential:

Unbiased (DI)

ADDITIONAL INFORMATION:

Worst Case Current Density:

Modified SEM

Transistor Count:

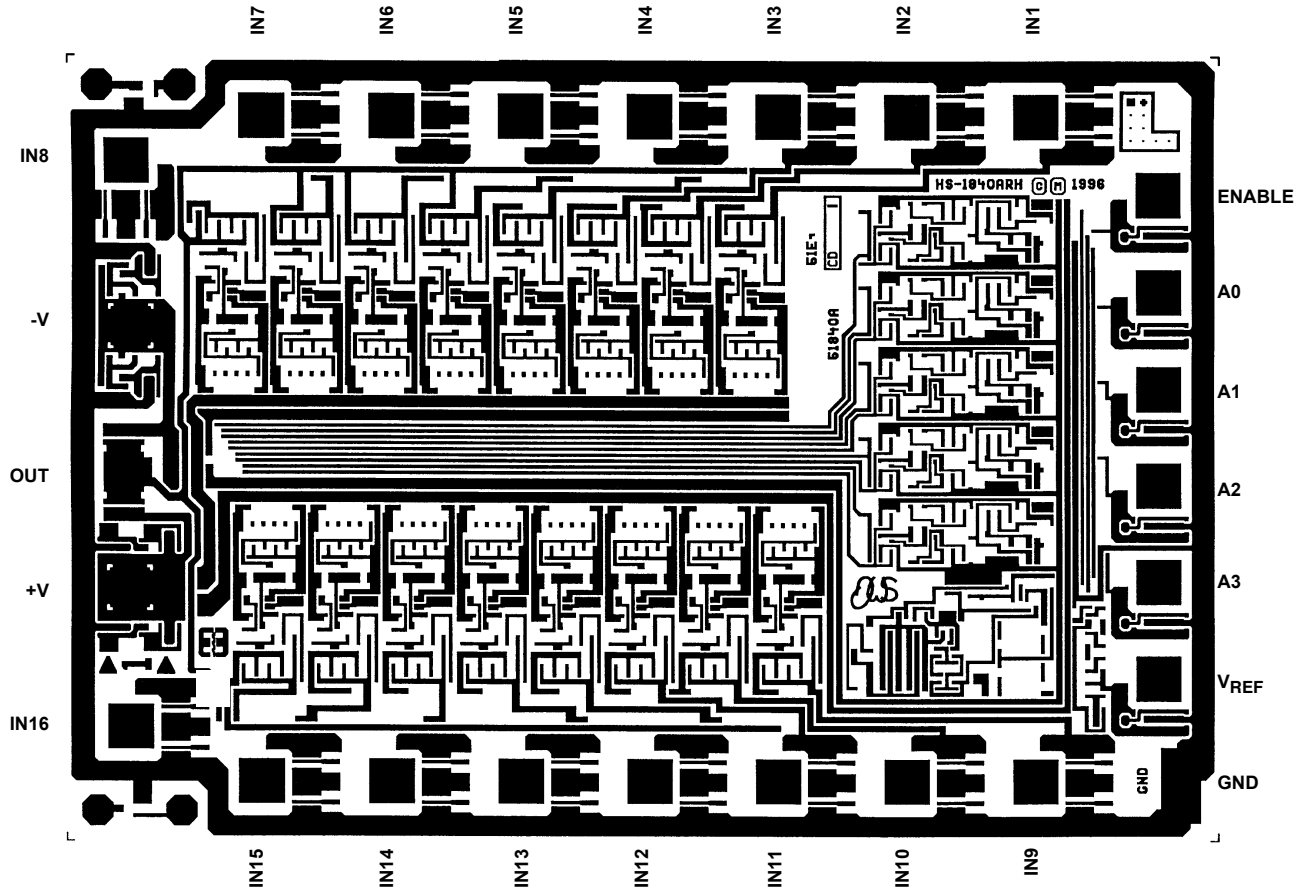
407

Process:

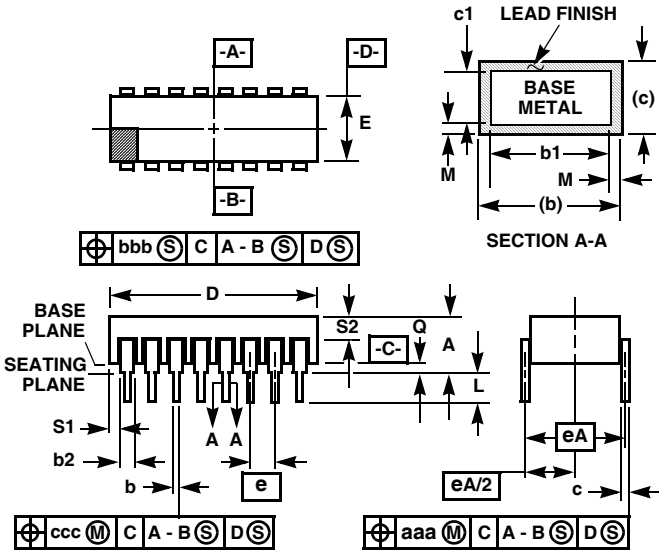
Radiation Hardened Silicon Gate,
DI Wafer, Dielectric Isolation

Metallization Mask Layout

HS-1840ARH, HS-1840BRH



Ceramic Dual-In-Line Metal Seal Packages (SBDIP)



NOTES:

1. Index area: A notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark.
2. The maximum limits of lead dimensions b and c or M shall be measured at the centroid of the finished lead surfaces, when solder dip or tin plate lead finish is applied.
3. Dimensions b1 and c1 apply to lead base metal only. Dimension M applies to lead plating and finish thickness.
4. Corner leads (1, N, N/2, and N/2+1) may be configured with a partial lead paddle. For this configuration dimension b3 replaces dimension b2.
5. Dimension Q shall be measured from the seating plane to the base plane.
6. Measure dimension S1 at all four corners.
7. Measure dimension S2 from the top of the ceramic body to the nearest metallization or lead.
8. N is the maximum number of terminal positions.
9. Braze fillets shall be concave.
10. Dimensioning and tolerancing per ANSI Y14.5M - 1982.
11. Controlling dimension: INCH.

D28.6 MIL-STD-1835 CDIP2-T28 (D-10, CONFIGURATION C)
28 LEAD CERAMIC DUAL-IN-LINE METAL SEAL PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.232	-	5.92	-
b	0.014	0.026	0.36	0.66	2
b1	0.014	0.023	0.36	0.58	3
b2	0.045	0.065	1.14	1.65	-
b3	0.023	0.045	0.58	1.14	4
c	0.008	0.018	0.20	0.46	2
c1	0.008	0.015	0.20	0.38	3
D	-	1.490	-	37.85	-
E	0.500	0.610	12.70	15.49	-
e	0.100 BSC		2.54 BSC		-
eA	0.600 BSC		15.24 BSC		-
eA/2	0.300 BSC		7.62 BSC		-
L	0.125	0.200	3.18	5.08	-
Q	0.015	0.060	0.38	1.52	5
S1	0.005	-	0.13	-	6
S2	0.005	-	0.13	-	7
α	90^o	105^o	90^o	105^o	-
aaa	-	0.015	-	0.38	-
bbb	-	0.030	-	0.76	-
ccc	-	0.010	-	0.25	-
M	-	0.0015	-	0.038	2
N	28		28		8

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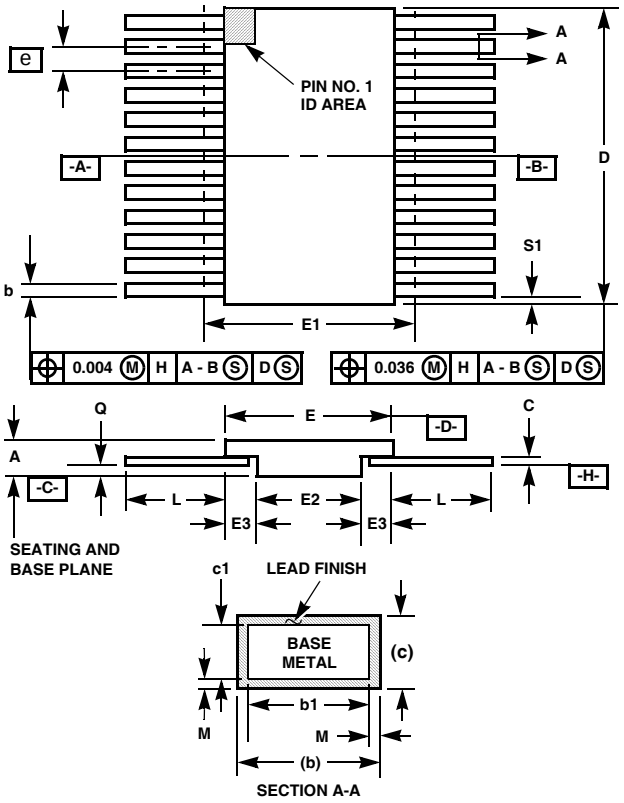
Ceramic Metal Seal Flatpack Packages (Flatpack)



K28.A MIL-STD-1835 CDFP3-F28 (F-11A, CONFIGURATION B)
28 LEAD CERAMIC METAL SEAL FLATPACK PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.045	0.115	1.14	2.92	-
b	0.015	0.022	0.38	0.56	-
b1	0.015	0.019	0.38	0.48	-
c	0.004	0.009	0.10	0.23	-
c1	0.004	0.006	0.10	0.15	-
D	-	0.740	-	18.80	3
E	0.460	0.520	11.68	13.21	-
E1	-	0.550	-	13.97	3
E2	0.180	-	4.57	-	-
E3	0.030	-	0.76	-	7
e	0.050 BSC		1.27 BSC		-
k	0.008	0.015	0.20	0.38	2
L	0.250	0.370	6.35	9.40	-
Q	0.026	0.045	0.66	1.14	8
S1	0.00	-	0.00	-	6
M	-	0.0015	-	0.04	-
N	28		28		-

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NOTES:

1. Index area: A notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark. Alternately, a tab (dimension k) may be used to identify pin one.
2. If a pin one identification mark is used in addition to a tab, the limits of dimension k do not apply.
3. This dimension allows for off-center lid, meniscus, and glass overrun.
4. Dimensions b1 and c1 apply to lead base metal only. Dimension M applies to lead plating and finish thickness. The maximum limits of lead dimensions b and c or M shall be measured at the centroid of the finished lead surfaces, when solder dip or tin plate lead finish is applied.
5. N is the maximum number of terminal positions.
6. Measure dimension S1 at all four corners.
7. For bottom-brazed lead packages, no organic or polymeric materials shall be molded to the bottom of the package to cover the leads.
8. Dimension Q shall be measured at the point of exit (beyond the meniscus) of the lead from the body. Dimension Q minimum shall be reduced by 0.0015 inch (0.038mm) maximum when solder dip lead finish is applied.
9. Dimensioning and tolerancing per ANSI Y14.5M - 1982.
10. Controlling dimension: INCH.