National Semiconductor Corporation

**ADVANCED INFORMATION**

microCMOS

# NMC27C1023
# 1,048,576-Bit (128k x 8) UV Erasable CMOS PROM

## General Description

The NMC27C1023 is a high-speed 1024k UV erasable and electrically reprogrammable CMOS EPROM, ideally suited for applications where fast turnaround, pattern experimentation and low power consumption are important requirements.

The NMC27C1023 is designed to operate with a single +5V power supply with ±10% tolerance. The CMOS design allows the part to operate over Extended and Military Temperature Ranges.

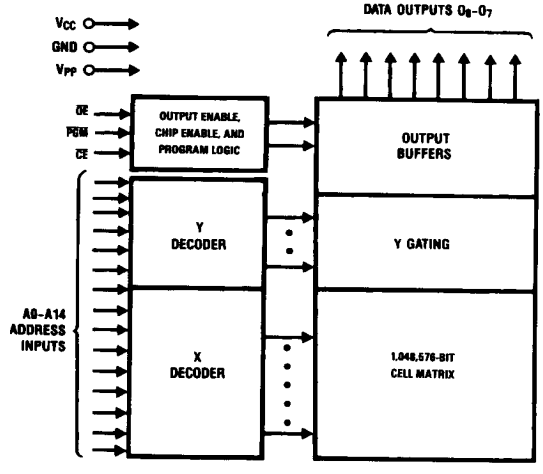
The NMC27C1023 is packaged in a 32-pin dual in-line package with transparent lid. The transparent lid allows the user to expose the chip to ultraviolet light to erase the bit pattern. A new pattern can then be written electrically into the device by following the programming procedure.

These EPROMs are fabricated with National's proprietary, time proven microCOMS double-poly silicon gate technology which combines high performance and high density with low power consumption and excellent reliability.

## Features

- Clocked sense amps for fast access time down to 90 ns
- Low CMOS power consumption
  - — Active Power: 165 mW max
  - — Standby Power: 0.55 mW max
- Performance compatible to NSC800 CMOS microprocessor
- Single 5V power supply
- Extended temperature range (NMC27C1023QE120), −40°C to 85°C and military temperature range (NMC27C1023QM150), −55°C to 125°C, available
- Pin compatible with NMOS bytewide 1024k EPROMs
- Fast and reliable programming (0.5 ms for most bytes)
- Static operation—no clocks required
- TTL, CMOS compatible inputs/outputs
- TRI-STATE® output

## Block Diagram

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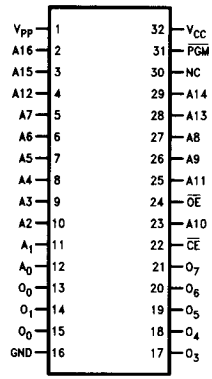
**Pin Names**

| | |
|---|---|
| A0–A16 | Addresses |
| $\overline{CE}$ | Chip Enable |
| $\overline{OE}$ | Output Enable |
| $O_0$–$O_7$ | Outputs |
| $\overline{PGM}$ | Program |
| NC | No Connect |

## Connection Diagram

| 27C512 27512 | 27C256 27256 | 27C128 27128 | 27C64 2764 |
|---|---|---|---|
| A15 | $V_{PP}$ | $V_{PP}$ | $V_{PP}$ |
| A12 | A12 | A12 | A12 |
| A7 | A7 | A7 | A7 |
| A6 | A6 | A6 | A6 |
| A5 | A5 | A5 | A5 |
| A4 | A4 | A4 | A4 |
| A3 | A3 | A3 | A3 |
| A2 | A2 | A2 | A2 |
| A1 | A1 | A1 | A1 |
| A0 | A0 | A0 | A0 |
| $O_0$ | $O_0$ | $O_0$ | $O_0$ |
| $O_1$ | $O_1$ | $O_1$ | $O_1$ |
| $O_2$ | $O_2$ | $O_2$ | $O_2$ |
| GND | GND | GND | GND |

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| 27C64 2764 | 27C128 27128 | 27C256 27256 | 27C512 27512 |
|---|---|---|---|
| $V_{CC}$ | $V_{CC}$ | $V_{CC}$ | $V_{CC}$ |
| $\overline{PGM}$ | $\overline{PGM}$ | A14 | A14 |
| NC | A13 | A13 | A13 |
| A8 | A8 | A8 | A8 |
| A9 | A9 | A9 | A9 |
| A11 | A11 | A11 | A11 |
| $\overline{OE}$ | $\overline{OE}$ | $\overline{OE}$ | $\overline{OE}/V_{PP}$ |
| A10 | A10 | A10 | A10 |
| $\overline{CE}$ | $\overline{CE}$ | $\overline{CE}/\overline{PGM}$ | $\overline{CE}$ |
| $O_7$ | $O_7$ | $O_7$ | $O_7$ |
| $O_6$ | $O_6$ | $O_6$ | $O_6$ |
| $O_5$ | $O_5$ | $O_5$ | $O_5$ |
| $O_4$ | $O_4$ | $O_4$ | $O_4$ |
| $O_3$ | $O_3$ | $O_3$ | $O_3$ |

**Order Number NMC27C1023Q**

**Note:** National's socket compatible EPROM pin configurations are shown in the blocks adjacent to the NMC27C1023 pins.

**Commercial Temperature Range (0°C to +70°C)**

$V_{CC}$ = 5V ±10%

| Parameter/Order Number | Access Time (ns) |
|---|---|
| NMC27C1023Q90 | 90 |
| NMC27C1023Q120 | 120 |
| NMC27C1023Q150 | 150 |
| NMC27C1023Q200 | 200 |

**Extanded Temp Range (−40°C to +85°C)**

$V_{CC}$ = 5V ±10%

| Parameter/Order Number | Access Time (ns) |
|---|---|
| NMC27C1023QE120 | 120 |

**Military Temp Range (−55°C to +125°C)**

$V_{CC}$ = 5V ±10%

| Parameter/Order Number | Access Time (ns) |
|---|---|
| NMC27C1023QM150 | 150 |

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## Absolute Maximum Ratings (Note 1)

**Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.**

| | |
|---|---|
| Temperature Under Bias | −10°C to +80°C |
| Storage Temperature | −65°C to +125°C |
| All Input Voltages and A9 with Respect to Ground | +6.5V to −0.6V |
| All Output Voltages with Respect to Ground | $V_{CC}$ + 0.3 to GND − 0.6V |
| $V_{PP}$ Supply Voltage and A9 with Respect to Ground | +13.0V to −0.6V |
| Power Dissipation | 1.0W |
| Lead Temperature (Soldering, 10 sec.) | 300°C |

ESD Rating to be determined.

## Operating Conditions (Note 7)

| | |
|---|---|
| $V_{CC}$ Power Supply | 5V ±10% |
| Temperature Range | |
| NMC27C1023Q90, 120, 150, 200 | 0°C to +70°C |
| NMC27C1023QE120 | −40°C to +85°C |
| NMC27C1023QM150 | −55°C to + 125°C |

## Read Operation

## DC Electrical Characteristics

| Symbol | Parameter | Conditions | Min | Typ (Note 2) | Max | Units |
|---|---|---|---|---|---|---|
| $I_{LI}$ | Input Load Current | $V_{IN} = V_{CC}$ or GND | | | 10 | μA |
| $I_{LO}$ | Output Leakage Current | $V_{OUT} = V_{CC}$ or GND $\overline{CE} = V_{IH}$ | | | 10 | μA |
| $I_{CC1}$ (Note 10) | $V_{CC}$ Current (Active) TTL Inputs | $\overline{CE} = V_{IL}$, f = 5 MHz All Inputs = $V_{IH}$ or $V_{IL}$, I/O = 0 mA | | 15 | 60 | mA |
| $I_{CC2}$ (Note 10) | $V_{CC}$ Current (Active) CMOS Inputs | $\overline{CE}$ = GND, f = 5 MHz All Inputs = $V_{CC}$ or GND, I/O = 0 mA | | 10 | 40 | mA |
| $I_{CCSB1}$ | $V_{CC}$ Current (Standby) TTL Inputs | $\overline{CE} = V_{IH}$ | | 0.1 | 1 | mA |
| $I_{CCSB2}$ | $V_{CC}$ Current (Standby) CMOS Inputs | $\overline{CE} = V_{CC}$ | | 0.5 | 100 | μA |
| $V_{IL}$ | Input Low Voltage | | −0.1 | | 0.8 | V |
| $V_{IH}$ | Input High Voltage | | 2.0 | | $V_{CC}$ + 1 | V |
| $V_{OL1}$ | Output Low Voltage | $I_{OL}$ = 2.1 mA | | | 0.45 | V |
| $V_{OH1}$ | Output High Voltage | $I_{OH}$ = −400 μA | 2.4 | | | V |
| $V_{OL2}$ | Output Low Voltage | $I_{OL}$ = 0 μA | | | 0.1 | V |
| $V_{OH2}$ | Output High Voltage | $I_{OH}$ = 0 μA | $V_{CC}$ − 0.1 | | | V |

## AC Electrical Characteristics

| Symbol | Parameter | Conditions | NMC27C1023 90 | | NMC27C1023 120 E120 | | NMC27C1023 150 M150 | | NMC27C1023 200 | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | Min | Max | Min | Max | Min | Max | Min | Max | |
| $t_{ACC}$ | Address to Output Delay | $\overline{CE} = \overline{OE} = V_{IL}$ | | 90 | | 120 | | 150 | | 200 | ns |
| $t_{CE}$ | $\overline{CE}$ to Output Delay | $\overline{OE} = V_{IL}$ | | 90 | | 120 | | 150 | | 200 | ns |
| $t_{OE}$ | $\overline{OE}$ to Output Delay | $\overline{CE} = V_{IL}$ | | 40 | | 50 | | 60 | | 75 | ns |
| $t_{DF}$ | $\overline{OE}$ High to Output Float | $\overline{CE} = V_{IL}$ | 0 | 40 | 0 | 40 | 0 | 50 | | 60 | ns |
| $t_{OH}$ | Output Hold from Addresses, $\overline{CE}$ or $\overline{OE}$, Whichever Occurred First | $\overline{CE} = \overline{OE} = V_{IL}$ | 0 | | 0 | | 0 | | 0 | | ns |

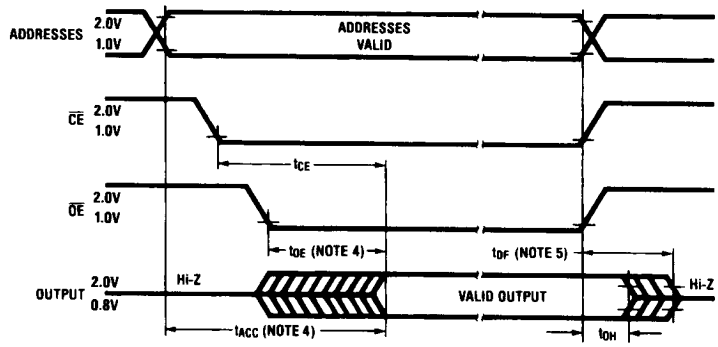
## Capacitance $T_A = +25°C$, f = 1 MHz (Note 3)

| Symbol | Parameter | Conditions | Typ | Max | Units |
|---|---|---|---|---|---|
| $C_{IN}$ | Input Capacitance | $V_{IN} = 0V$ | 4 | 6 | pF |
| $C_{OUT}$ | Output Capacitance | $V_{OUT} = 0V$ | 8 | 12 | pF |

## AC Test Conditions

| | |
|---|---|
| Output Load<br>$C_L$ = 100 pF | 1 TTL Gate and (Note 9) |
| Input Rise and Fall Times | ≤ 5 ns |
| Input Pulse Levels | 0.45V to 2.4V |
| Timing Measurement Reference Level | |
| Inputs | 1V and 2V |
| Outputs | 0.8V and 2V |

## AC Waveforms

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**Note 1:** Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**Note 2:** Typical values are for $T_A = +25°C$ and nominal supply voltages.

**Note 3:** This parameter is only sampled and is not 100% tested.

**Note 4:** $\overline{OE}$ may be delayed up to $t_{ACC} - t_{OE}$ after the falling edge of $\overline{CE}$ without impacting $t_{ACC}$.

**Note 5:** The $t_{OHZ}$ compare level is determined as follows:

High to TRI-STATE, the measured $V_{OH1}$ (DC) − 0.10V

Low to TRI-STATE, the measured $V_{OL1}$ (DC) + 0.10V

**Note 6:** TRI-STATE may be attained using $\overline{OE}$ or $\overline{CE}$.

**Note 7:** The power switching characteristics of EPROMs require careful device decoupling. It is recommended that at least a 0.1 μF ceramic capacitor be used on every device between $V_{CC}$ and GND.

**Note 8:** The outputs must be restricted to $V_{CC}$ + 0.3V to avoid latch-up and device damage.

**Note 9:** 1 TTL Gate: $I_{OL} = 1.6$ mA, $I_{OH} = -400$ μA.

$C_L$: 100 pF includes fixture capacitance.

**Note 10:** $V_{PP}$ may be connected to $V_{CC}$ except during programming.

## Programming Characteristics

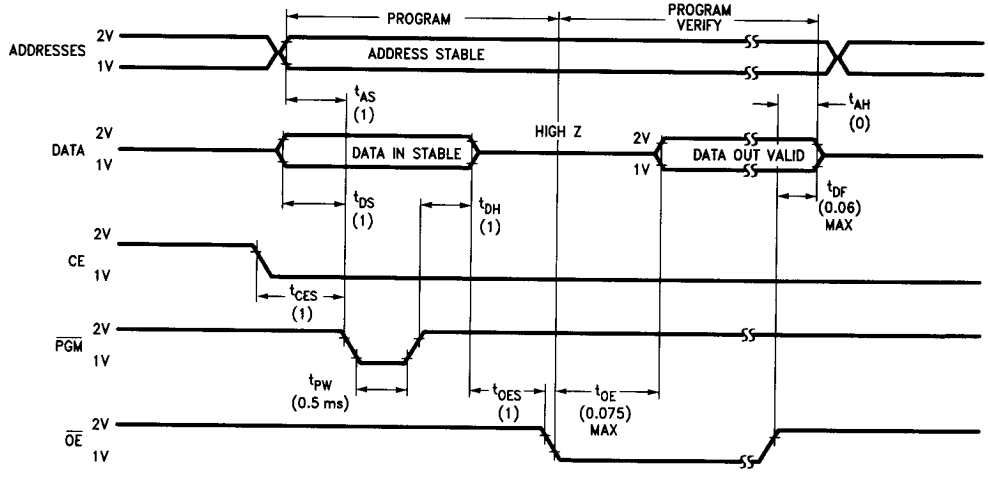
$T_A$ = +25°C ±5°C, $V_{CC}$ = 6V ±0.25V, $V_{PP}$ = 12.5 ±0.3V (Notes 2, 3, & 4)

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $t_{AS}$ | Address Set-Up Time | | 1 | | | μs |
| $t_{OES}$ | $\overline{OE}$ Set-Up Time | | 1 | | | μs |
| $t_{DS}$ | Data Set-Up Time | | 1 | | | μs |
| $t_{AH}$ | Address Hold Time | | 0 | | | μs |
| $t_{DH}$ | Data Hold Time | | 1 | | | μs |
| $t_{CES}$ | $\overline{CE}$ Set-Up Time | | 1 | | | μs |
| $t_{ACC}$ | Address to Output Delay | | | | 200 | ns |
| $t_{DF}$ | Output Enable to Output Float Delay | $\overline{CE}$ = $V_{IL}$ | 0 | | 60 | ns |
| $t_{OE}$ | Output Enable to Output Delay | $\overline{CE}$ = $V_{IL}$ | | | 75 | ns |
| $t_{PW}$ | Program Pulse Width | | 0.5 | 0.5 | 10 | ms |
| $I_{PP}$ | $V_{PP}$ Supply During Programming Pulse | $\overline{CE}$ = $V_{IL}$ | | | 30 | mA |
| $I_{CC}$ | $V_{CC}$ Supply Current | | | | 10 | mA |

## AC Test Conditions

| | | | |
|---|---|---|---|
| $V_{CC}$ | 6V ±0.25V | Input Pulse Levels | 0.45V to 2.4V |
| $V_{PP}$ | 12.5V ±0.3V | Timing Measurement Reference Level | |
| Input Rise and Fall Times | ≤ 5 ns | Inputs | 1V and 2V |
| | | Outputs | 0.8V and 2V |

## Programming Waveforms (Note 3)

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**Note:** All times shown in parentheses are minimum and in μs unless otherwise specified.

$T_{OE}$ and $T_{DF}$ are characteristics of the device but must be accommodated by the programmer.

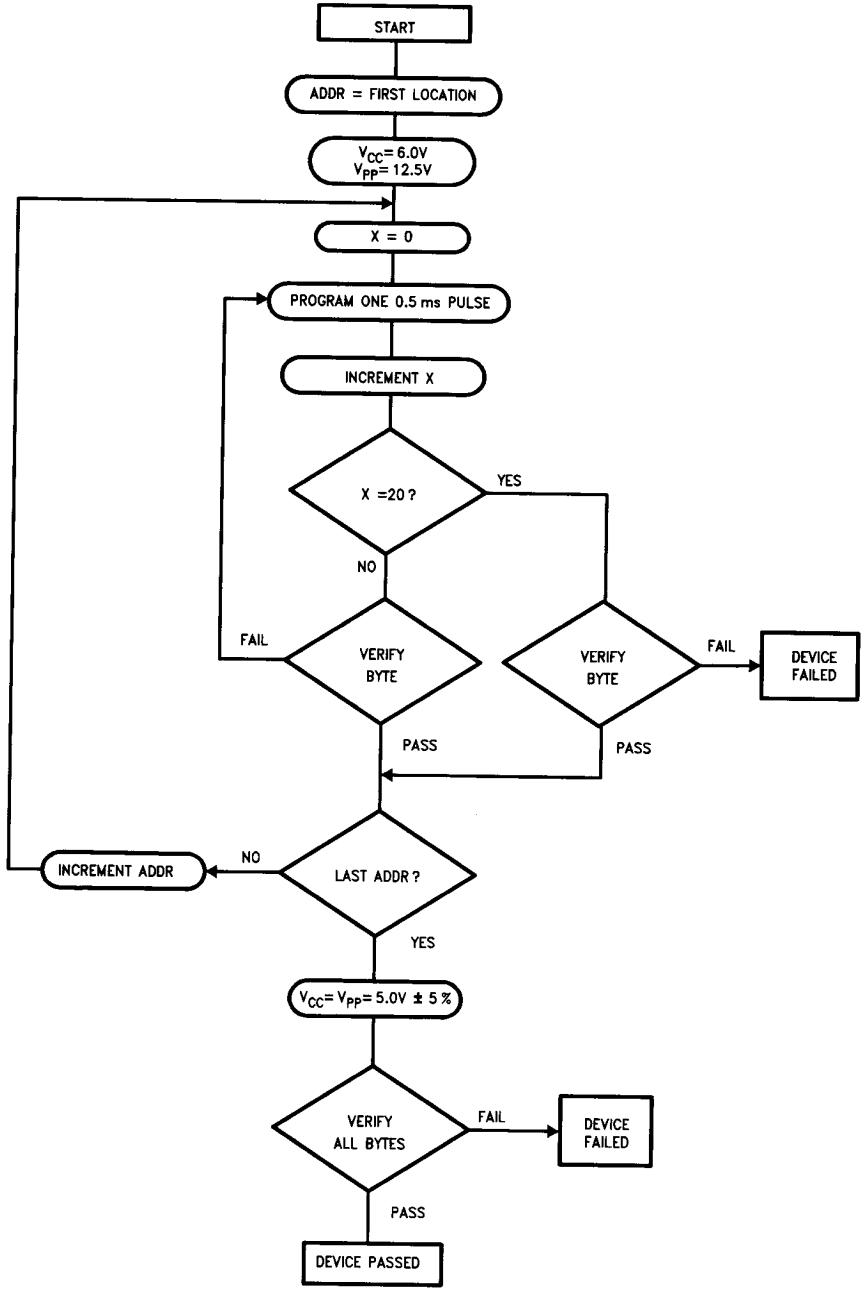
**Note 1:** National's standard product warranty applies only to devices programmed to specifications described herein.

**Note 2:** $V_{CC}$ must be applied simultaneously or before $V_{PP}$ and removed simultaneously or after $V_{PP}$. The EPROM must not be inserted into or removed from a board with voltage applied to $V_{PP}$ or $V_{CC}$.

**Note 3:** The maximum allowable voltage which may be applied to the $V_{PP}$ pin during programming is 13V. Care must be taken when switching the $V_{PP}$ supply to prevent overshoot exceeding this 13V maximum specification. At least a 0.1 μF capacitor is required across $V_{PP}$, $V_{CC}$ to GND to suppress spurious voltage transients which may damage the device.

**Note 4:** Programming and program verify are tested at nominal power supply voltages.

**Interactive Programming Flow Chart**

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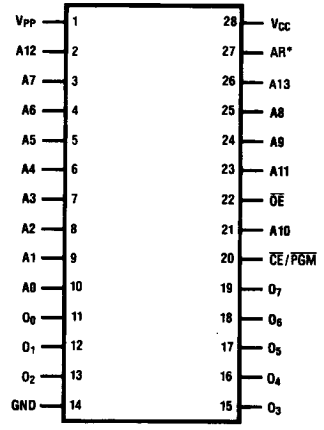
## Connection Diagram

| 27C512<br>27512 | 27C256<br>27256 | 27C64<br>2764 | 27C32<br>2732 | 27C16<br>2716 |
|---|---|---|---|---|
| A15 | $V_{PP}$ | $V_{PP}$ | | |
| A12 | A12 | A12 | | |
| A7 | A7 | A7 | A7 | A7 |
| A6 | A6 | A6 | A6 | A6 |
| A5 | A5 | A5 | A5 | A5 |
| A4 | A4 | A4 | A4 | A4 |
| A3 | A3 | A3 | A3 | A3 |
| A2 | A2 | A2 | A2 | A2 |
| A1 | A1 | A1 | A1 | A1 |
| A0 | A0 | A0 | A0 | A0 |
| $O_0$ | $O_0$ | $O_0$ | $O_0$ | $O_0$ |
| $O_1$ | $O_1$ | $O_1$ | $O_1$ | $O_1$ |
| $O_2$ | $O_2$ | $O_2$ | $O_2$ | $O_2$ |
| GND | GND | GND | GND | GND |

**Dual-In-Line Package**

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| 27C16<br>2716 | 27C32<br>2732 | 27C64<br>2764 | 27C256<br>27256 | 27C512<br>27512 |
|---|---|---|---|---|
| | | $V_{CC}$ | $V_{CC}$ | $V_{CC}$ |
| | | $\overline{PGM}$ | A14 | A14 |
| $V_{CC}$ | $V_{CC}$ | NC | A13 | A13 |
| A8 | A8 | A8 | A8 | A8 |
| A9 | A9 | A9 | A9 | A9 |
| $V_{PP}$ | A11 | A11 | A11 | A11 |
| $\overline{OE}$ | $\overline{OE}/V_{PP}$ | $\overline{OE}$ | $\overline{OE}$ | $\overline{OE}/V_{PP}$ |
| A10 | A10 | A10 | A10 | A10 |
| $\overline{CE}/\overline{PGM}$ | $\overline{CE}$ | $\overline{CE}$ | $\overline{CE}/\overline{PGM}$ | $\overline{CE}$ |
| $O_7$ | $O_7$ | $O_7$ | $O_7$ | $O_7$ |
| $O_6$ | $O_6$ | $O_6$ | $O_6$ | $O_6$ |
| $O_5$ | $O_5$ | $O_5$ | $O_5$ | $O_5$ |
| $O_4$ | $O_4$ | $O_4$ | $O_4$ | $O_4$ |
| $O_3$ | $O_3$ | $O_3$ | $O_3$ | $O_3$ |

*AR held at $V_{IH}$

**Note:** National's socket compatible EPROM pin configurations are shown in the blocks adjacent to the NMC27CP128 pins.

**Order Number NMC27CP128Q**
**See NS Package Number J28A–Q**

**Commercial Temp Range (0°C to +70°C)**

$V_{CC}$ = 5V ±10%

| Parameter/Order Number | Access Time (ns) |
|---|---|
| NMC27CP128Q200 | 200 |
| NMC27CP128Q250 | 250 |
| NMC27CP128Q300 | 300 |

## Functional Description (Continued)

**TABLE I. Mode Selection**

| Pins / Mode | $\overline{CE}$ (22) | $\overline{OE}$ (24) | $\overline{PGM}$ (31) | $V_{PP}$ (1) | $V_{CC}$ (32) | Outputs (13–15, 17–21) |
|---|---|---|---|---|---|---|
| Read | $V_{IL}$ | $V_{IL}$ | $V_{IH}$ | $V_{CC}$ | 5 | $D_{OUT}$ |
| Standby | $V_{IH}$ | Don't Care | Don't Care | $V_{CC}$ | 5 | Hi-Z |
| Program | $V_{IL}$ | $V_{IH}$ | ⊓ | 11.5 | 6 | $D_{IN}$ |
| Program Verify | $V_{IL}$ | $V_{IL}$ | $V_{IH}$ | 11.5 | 6 | $D_{OUT}$ |
| Program Inhibit | $V_{IH}$ | Don't Care | Don't Care | 11.5 | 6 | Hi-Z |

**TABLE II. Manufacturer's Identification Code**

| Pins | $A_0$ (12) | $O_7$ (21) | $O_6$ (20) | $O_5$ (19) | $O_4$ (18) | $O_3$ (17) | $O_2$ (15) | $O_1$ (14) | $O_0$ (13) | Hex Data |
|---|---|---|---|---|---|---|---|---|---|---|
| Manufacturer Code | $V_{IL}$ | 1 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 8F |
| Device Code | $V_{IH}$ | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 86 |

The Manufacturer's Identification code, shown in Table II, specifically identifies the manufacturer and the device type. The code for the NMC27C1023 is "8F86", where "8F" designates that it is made by National Semiconductor, and "86" designates a 1Megabit byte-wide part.

The code is accessed by applying 11.4V to 12.0V to address pin A9. Addresses A1–A8, A10–A16, and all control pins are held at $V_{IL}$. Address pin A0 is held at $V_{IL}$ for the manufacturer's code, and held at $V_{IH}$ for the device code. The code is read on the eight data pins, $O_0$–$O_7$. Proper code access is only guaranteed at 25°C ±5°C.

### ERASURE CHARACTERISTICS

The erasure characteristics of the NMC27C1023 are such that erasure begins to occur when exposed to light with wavelengths shorter than approximately 4000 Angstroms (Å). It should be noted that sunlight and certain types of fluorescent lamps have wavelengths in the 3000Å–4000Å range. Data shows that constant exposure to room-level fluorescent lighting could erase the typical NMC27C1023 in approximately 3 years, while it would take approximately 1 week to cause erasure when exposed to direct sunlight. Opaque labels should be placed over the NMC27C1023 window to prevent unintentional erasure. Covering the window will also prevent temporary functional failure due to the generation of photo currents.

The recommended erasure procedure for the NMC27C1023 is exposure to short wave ultraviolet light which has a wavelength of 2537 Angstroms (Å). The integrated dose (i.e., UV intensity × exposure time) for erasure should be a minimum of 15W-sec/cm$^2$.

The NMC27C1023 should be placed within 1 inch of the lamp tubes during erasure. Some lamps have a filter on their tubes which should be removed before erasure. Table III shows the minimum NMC27C1023 erasure time for various light intensities.

An erasure system should be calibrated periodically. The distance from lamp to unit should be maintained at one inch. The erasure time increases as the square of the distance. (If distance is doubled the erasure time increases by a factor of 4.) Lamps lose intensity as they age. When a lamp is changed, the distance has changed, or the lamp has aged, the system should be checked to make certain full erasure is occurring. Incomplete erasure will cause symptoms that can be misleading. Programmers, components, and even system designs have been erroneously suspected when incomplete erasure was the problem.

### SYSTEM CONSIDERATION

The power switching characteristics of EPROMs require careful decoupling of the devices. The supply current, $I_{CC}$, has three segments that are of interest to the system designe)—the standby current level, the active current level, and the transient current peaks that are produced by voltage transitions on input pins. The magnitude of these transient current peaks is dependent on the output capacitance loading the device. The associated $V_{CC}$ transient voltage peaks can be suppressed by properly selected decoupling capacitors. It is recommended that at least a 0.1 μF ceramic capacitor be used on every device between $V_{CC}$ and GND. This should be a high frequency capacitor of low inherent inductance. In addition, at least a 4.7 μF bulk electrolytic capacitor should be used between $V_{CC}$ and GND for each eight devices. The bulk capacitor should be located near where the power supply is connected to the array. The purpose of the bulk capacitor is to overcome the voltage drop caused by the inductive effects of the PC board traces.

**TABLE III. NMC27C1023 Minimum Erasure Time**

| Light Intensity (Micro-Watts/cm$^2$) | Erasure Time (Minutes) |
|---|---|
| 15,000 | 20 |
| 10,000 | 25 |
| 5,000 | 50 |