19-3432; Rev 0; 11/04

EVALUATION KIT AVAILABLE

12-Bit, 125Msps ADC with CMOS Outputs for Wideband Applications

General Description

The MAX19541 monolithic 12-bit, 125Msps analog-to-digital converter (ADC) is optimized for outstanding dynamic performance at high-IF frequencies of 300MHz and beyond. This device operates with conversion rates up to 125Msps while consuming only 861mW.

At 125Msps and an input frequency of 240MHz, the MAX19541 achieves a spurious-free dynamic range (SFDR) of 71.5dBc. The MAX19541 features an excellent signal-to-noise ratio (SNR) of 65.4dB at 10MHz that remains flat (within 3dB) for input tones up to 250MHz. This makes the MAX19541 ideal for wideband applications such as power-amplifier predistortion in cellular base-station transceiver systems.

The MAX19541 operates in either parallel mode where the data outputs appear on a single parallel port at the sampling rate, or in demux parallel mode, where the outputs appear on two separate parallel ports at one-half the sampling rate. See the *Mode of Operation* section.

The MAX19541 operates on a single 1.8V supply. The analog input is differential and can be AC- or DC-coupled. The ADC also features a selectable on-chip divide-by-2 clock circuit that allows clock frequencies as high as 250MHz. This helps to reduce the phase noise of the input clock source, allowing for higher dynamic performance. For best performance, a differential LVPECL sampling clock is recommended. The digital outputs are CMOS compatible and the data format can be selected to be either two's complement or offset binary.

A pin-compatible, 12-bit, 170Msps version of the MAX19541 is also available. Refer to the MAX19542 data sheet for more information.

The MAX19541 is available in a 68-pin QFN with exposed paddle (EP) and is specified over the extended (-40°C to +85°C) temperature range.

Applications

Base-Station Power Amplifier Linearization

Cable Head-End Receivers

Wireless and Wired Broadband Communication

Communications Test Equipment

Radar and Satellite Subsystems

Features

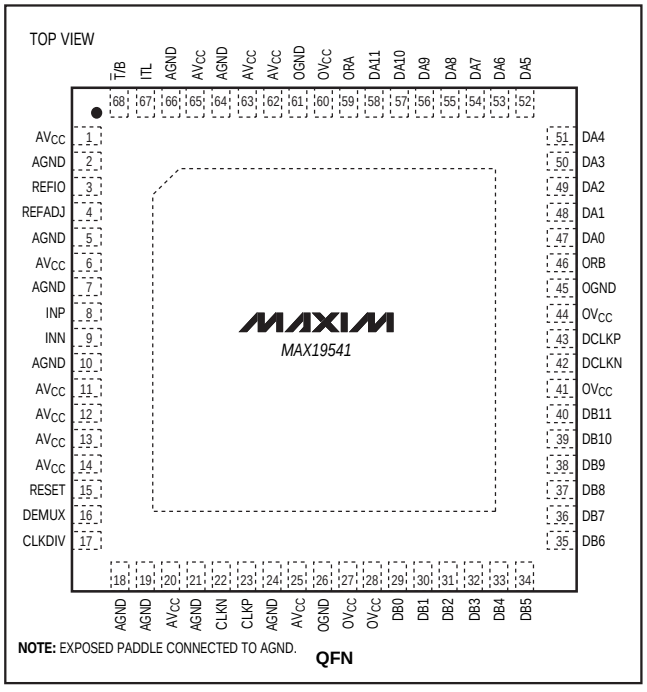
- **125Msps Conversion Rate**
- **SNR = 65dB, f_{IN} = 100MHz at 125Msps**
- **SFDR = 77dBc, f_{IN} = 100MHz at 125Msps**
- **±0.7 LSB INL, ±0.25 DNL (typ)**
- **861mW Power Dissipation at 125Msps**
- **On-Chip Selectable Divide-by-2 Clock Input**
- **Parallel or Demux Parallel Digital CMOS Outputs**
- **Reset Option for Synchronizing Multiple ADCs**
- **Data Clock Output**
- **Offset Binary or Two's-Complement Output**
- **Evaluation Kit Available (MAX19541EVKIT)**

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE	PKG CODE
MAX19541EGK	-40°C to +85°C	68 QFN-EP*	G6800-4

EP = Exposed paddle.

Pin Configuration



NOTE: EXPOSED PADDLE CONNECTED TO AGND.

QFN

12-Bit, 125Msps ADC with CMOS Outputs for Wideband Applications

ABSOLUTE MAXIMUM RATINGS

AV_{CC} to AGND .....-0.3V to +2.1V
OV_{CC} to OGND .....-0.3V to +2.1V
AV_{CC} to OV_{CC} .....-0.3V to +2.1V
AGND to OGND .....-0.3V to +0.3V
Analog Inputs (INP, INN) to AGND .....-0.3V to (AV_{CC} + 0.3V)
All Digital Inputs to AGND.....-0.3V to (AV_{CC} + 0.3V)
REFIO, REFADJ to AGND.....-0.3V to (AV_{CC} + 0.3V)
All Digital Outputs to OGND.....-0.3V to (OV_{CC} + 0.3V)
Maximum Current into Any Pin .....±50mA
ESD on All Pins (Human Body Model).....±2000V
Continuous Power Dissipation (T_A = +70°C)
68-Pin QFN (derate 41.7mW/°C above +70°C) 3333mW
Operating Temperature Range .....-40°C to +85°C
Junction Temperature.....+150°C
Storage Temperature Range .....-60°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(AV_{CC} = OV_{CC} = 1.8V, AGND = OGND = 0, f_{SAMPLE} = 125MHz, DEMUX = 0, differential LVPECL clock input drive, 0.1µF capacitor on REFIO, internal reference, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. $T_A \geq$ +25°C guaranteed by production test, $T_A <$ +25°C guaranteed by design and characterization. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DC ACCURACY						
Resolution			12			Bits
Integral Nonlinearity	INL	f_{IN} = 10MHz (Note 1)	-2.5	±0.7	+2.5	LSB
Differential Nonlinearity	DNL	f_{IN} = 10MHz, no missing codes (Note 1)	-0.75	±0.25	+0.75	LSB
Transfer Curve Offset	V_{OS}	(Note 1)	-3		+3	mV
Offset Temperature Drift				40		mV/°C
ANALOG INPUTS (INP, INN)						
Full-Scale Input Voltage Range	V_{FS}	(Note 1)	1300	1410	1510	mV_{P-P}
Full-Scale Range Temperature Drift				130		ppm/°C
Common-Mode Input Range	V_{CM}			1.365 ±0.15		V
Input Capacitance	C_{IN}			3		pF
Differential Input Resistance	R_{IN}		3.00	4.3	6.25	kΩ
Full-Power Analog Bandwidth	FPBW			900		MHz
REFERENCE (REFIO, REFADJ)						
Reference Output Voltage	V_{REFIO}		1.22	1.245	1.27	V
Reference Temperature Drift				90		ppm/°C
REFADJ Input High Voltage	V_{REFADJ}	Used to disable the internal reference	AV_{CC} - 0.3			V
SAMPLING CHARACTERISTICS						
Maximum Sampling Rate	f_{SAMPLE}		125			MHz
Minimum Sampling Rate	f_{SAMPLE}			20		MHz
Clock Duty Cycle		Set by clock-management circuit		40 to 60		%
Aperture Delay	t_{AD}	Figure 4		620		ps
Aperture Jitter	t_{AJ}			0.2		ps_{RMS}

ELECTRICAL CHARACTERISTICS (continued)

(AV_{CC} = OV_{CC} = 1.8V, AGND = OGND = 0, f_{SAMPLE} = 125MHz, DEMUX = 0, differential LVPECL clock input drive, 0.1µF capacitor on REFIO, internal reference, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. $T_A \geq +25°C$ guaranteed by production test, $T_A < +25°C$ guaranteed by design and characterization. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
CLOCK INPUTS (CLKP, CLKN)						
Differential Clock Input Amplitude		(Note 2)	200	500		mV_{P-P}
Clock Input Common-Mode Voltage Range				1.15 ±0.25		V
Clock Differential Input Resistance	R_{CLK}			11 ±25%		kΩ
Clock Differential Input Capacitance	C_{CLK}			5		pF
DYNAMIC CHARACTERISTICS (at -2dBFS)						
Signal-to-Noise Ratio	SNR	f_{IN} = 10MHz	63.7	65.4		dB
		f_{IN} = 100MHz	63.3	65		
		f_{IN} = 180MHz		64.1		
		f_{IN} = 240MHz		63.4		
Signal-to-Noise and Distortion	SINAD	f_{IN} = 10MHz	63.1	65.2		dB
		f_{IN} = 100MHz	62.5	64.2		
		f_{IN} = 180MHz		63.4		
		f_{IN} = 240MHz		62.7		
Spurious-Free Dynamic Range	SFDR	f_{IN} = 10MHz	72	82		dBc
		f_{IN} = 100MHz	70.5	77		
		f_{IN} = 180MHz		75		
		f_{IN} = 240MHz		71.5		
Worst Harmonics (HD2 or HD3)		f_{IN} = 10MHz		-88.7	-72	dBc
		f_{IN} = 100MHz		-73.1	-70.5	
		f_{IN} = 180MHz		-72.8		
		f_{IN} = 240MHz		-71.5		
Two-Tone Intermodulation Distortion	IMD_{100}	f_{IN1} = 150MHz at -7dBFS, f_{IN2} = 153MHz at -7dBFS, f_{SAMPLE} = 125MHz		-75		dBc
CMOS DIGITAL OUTPUTS (DA0–DA11, DB0–DB11, ORA, ORB)						
Logic-High Output Voltage	V_{OH}		OV_{CC} - 0.1			V
Logic-Low Output Voltage	V_{OL}				0.1	V
LVCMOS DIGITAL INPUTS (CLKDIV, $\overline{T}$/B, DEMUX, ITL)						
Digital Input-Voltage Low	V_{IL}				0.2 x AV_{CC}	V
Digital Input-Voltage High	V_{IH}		0.8 x AV_{CC}			V

12-Bit, 125Msps ADC with CMOS Outputs for Wideband Applications

ELECTRICAL CHARACTERISTICS (continued)

(AV_{CC} = OV_{CC} = 1.8V, AGND = OGND = 0, f_{SAMPLE} = 125MHz, DEMUX = 0, differential LVPECL clock input drive, 0.1µF capacitor on REFIO, internal reference, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. $T_A \geq +25°C$ guaranteed by production test, $T_A < +25°C$ guaranteed by design and characterization. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Resistance	R_{IN}			46.5		kΩ
Input Capacitance	C_{IN}			5		pF
TIMING CHARACTERISTICS						
CLKP-to-DA0–DA11 Propagation Delay	t_{PDL}	Figures 5, 6, 7		2.5		ns
CLK-to-DCLKP Propagation Delay	t_{CPDL}	Figures 5, 6, 7		2.1		ns
DCLKP Rising Edge to DA0–DA11	t_{PDL} - t_{CPDL}	Figures 5, 6, 7 (Note 2)	180	400	710	ns
CMOS Output Rise Time	t_{RISE}	20% to 80%, C_L = 5pF		1		ns
CMOS Output Fall Time	t_{FALL}	20% to 80%, C_L = 5pF		1		ns
RESET Hold	t_{HR}	Figure 4		100		ps
RESET Setup	t_{SR}	Figure 4		500		ps
Output Data Pipeline Delay	$t_{LATENCY}$	Figure 4		11		Clock cycles
POWER REQUIREMENTS						
Analog Supply Voltage Range	AV_{CC}		1.7	1.8	1.9	V
Digital Supply Voltage Range	OV_{CC}		1.7	1.8	1.9	V
Analog Supply Current	I_{AVCC}	f_{IN} = 100MHz		460	500	mA
Digital Supply Current	I_{OVCC}	f_{IN} = 100MHz		18	25	mA
Analog Power Dissipation	P_{DISS}	f_{IN} = 100MHz		861	945	mW
Power-Supply Rejection Ratio	PSRR	Offset (Note 3)		1.8		mV/V
		Gain (Note 3)		1.5		%FS/V

Note 1: Static linearity and offset parameters are computed from a straight line drawn between the end points of the code transition transfer function. The full-scale range (FSR) is defined as 4096 x slope of the line.

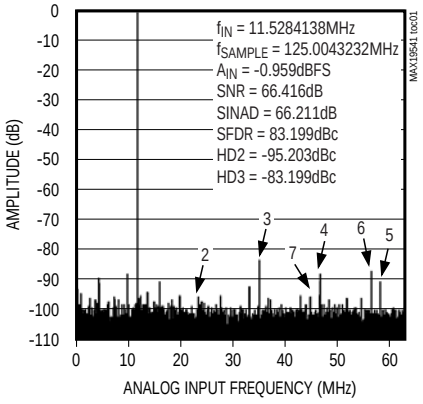
Note 2: Parameter guaranteed by design and characterization; T_A = T_{MIN} to T_{MAX}.

Note 3: PSRR is measured with both analog and digital supplies connected to the same potential.

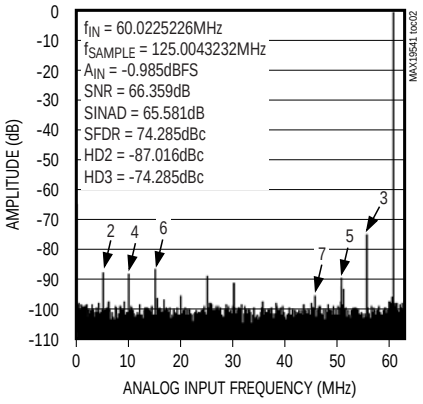
Typical Operating Characteristics

(AV_{CC} = OV_{CC} = 1.8V, AGND = OGND = 0, f_{SAMPLE} = 125MHz, A_{IN} = -1dBFS; see TOCs for detailed information on test conditions, differential input drive, differential LVPECL clock input drive, 0.1µF capacitor on REFIO, internal reference, digital outputs differential R_L = 100Ω, T_A = +25°C.)

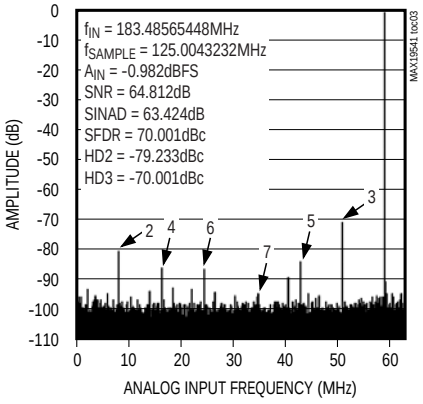
FFT PLOT (16,384-POINT DATA RECORD)



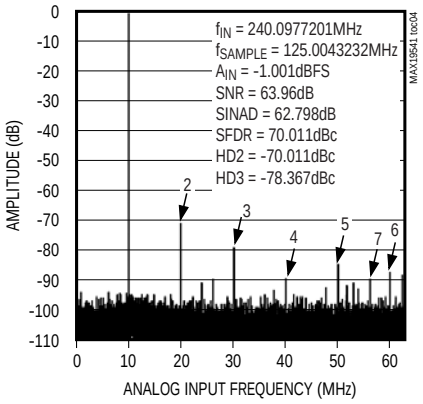
FFT PLOT (16,384-POINT DATA RECORD)



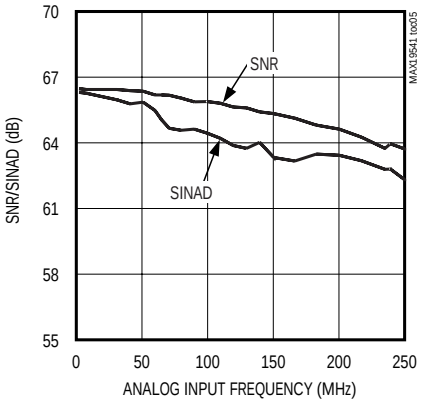
FFT PLOT (16,384-POINT DATA RECORD)



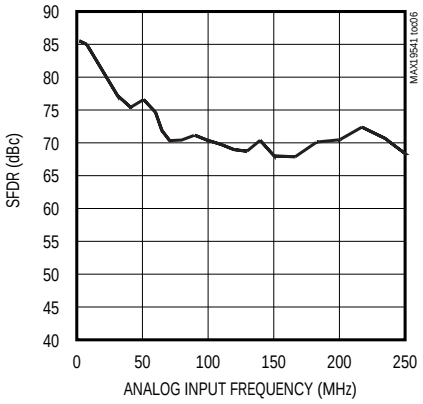
FFT PLOT (16,384-POINT DATA RECORD)



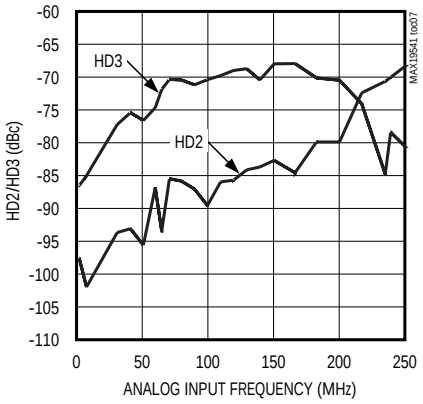
SNR/SINAD vs. ANALOG INPUT FREQUENCY (f_{SAMPLE} = 125.0043MHz, A_{IN} = -1dBFS)



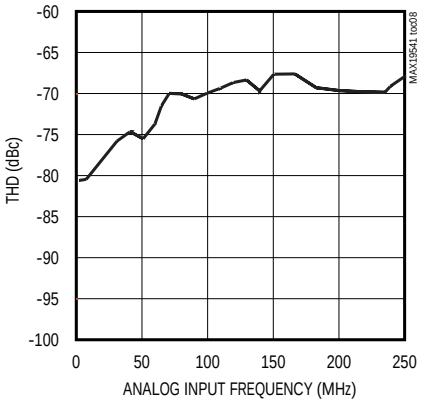
SFDR vs. ANALOG INPUT FREQUENCY (f_{SAMPLE} = 125.0043MHz, A_{IN} = -1dBFS)



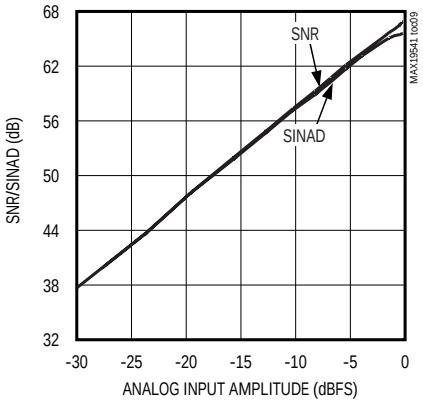
HD2/HD3 vs. ANALOG INPUT FREQUENCY (f_{SAMPLE} = 125.0043MHz, A_{IN} = -1dBFS)



THD vs. ANALOG INPUT FREQUENCY (f_{SAMPLE} = 125.0043MHz, A_{IN} = -1dBFS)



SNR/SINAD vs. ANALOG INPUT AMPLITUDE (f_{SAMPLE} = 125.0043MHz, f_{IN} = 60.0225MHz)

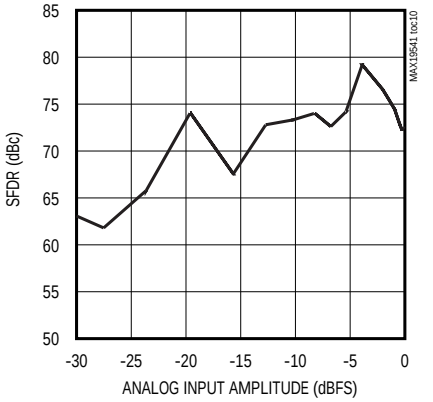


12-Bit, 125Msps ADC with CMOS Outputs for Wideband Applications

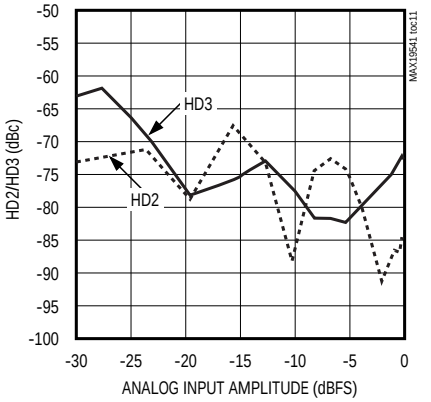
Typical Operating Characteristics (continued)

(AV_{CC} = OV_{CC} = 1.8V, AGND = OGND = 0, f_{SAMPLE} = 125MHz, A_{IN} = -1dBFS; see TOCs for detailed information on test conditions, differential input drive, differential LVPECL clock input drive, 0.1µF capacitor on REFIO, internal reference, digital outputs differential R_L = 100Ω, T_A = +25°C.)

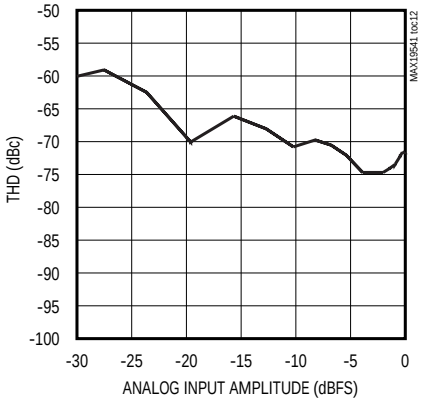
SFDR vs. ANALOG INPUT AMPLITUDE (f_{SAMPLE} = 125.0043MHz, f_{IN} = 60.0225MHz)



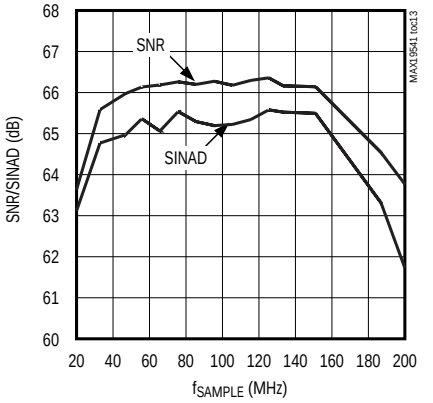
HD2/HD3 vs. ANALOG INPUT AMPLITUDE (f_{SAMPLE} = 125.0043MHz, f_{IN} = 60.0225MHz)



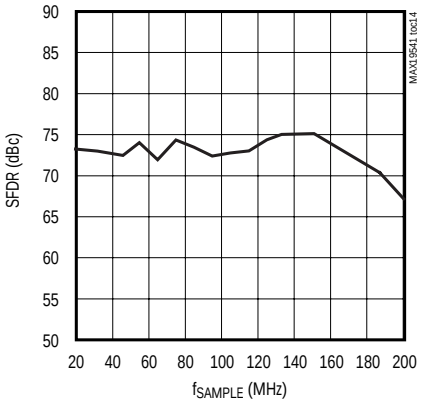
THD vs. ANALOG INPUT AMPLITUDE (f_{SAMPLE} = 125.0043MHz, f_{IN} = 60.0225MHz)



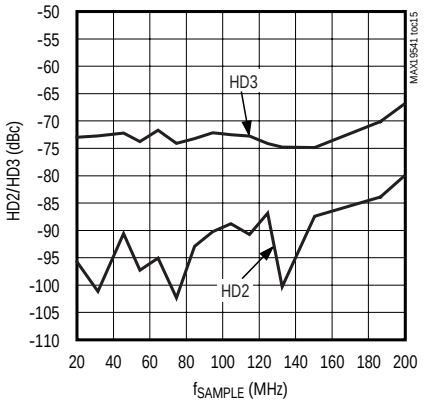
SNR/SINAD vs. f_{SAMPLE} (f_{IN} = 60.0225MHz. A_{IN} = -1dBFS)



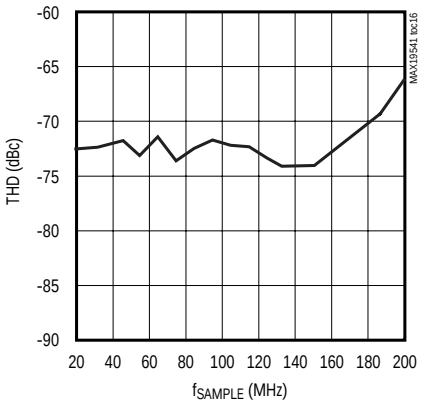
SFDR vs. f_{SAMPLE} (f_{IN} = 60.0225MHz, A_{IN} = -1dBFS)



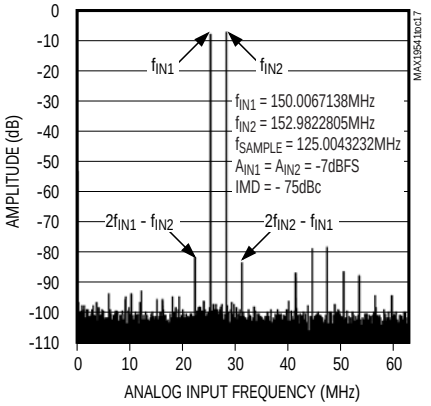
HD2/HD3 vs. f_{SAMPLE} (f_{IN} = 65.0225MHz, A_{IN} = -1dBFS)



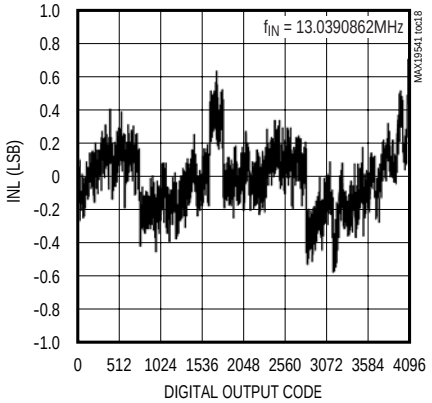
THD vs. f_{SAMPLE} (f_{IN} = 60.0225MHz, A_{IN} = -1dBFS)



TWO-TONE IMD PLOT (16,384-POINT DATA RECORD)



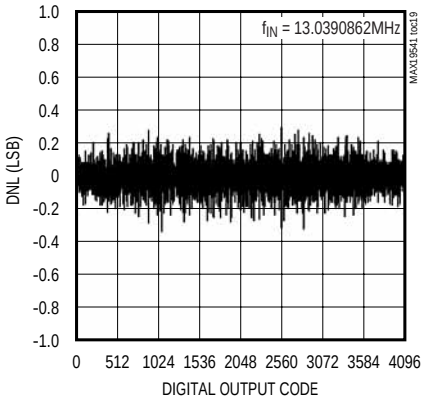
INL vs. DIGITAL OUTPUT CODE (512k-POINT DATA RECORD)



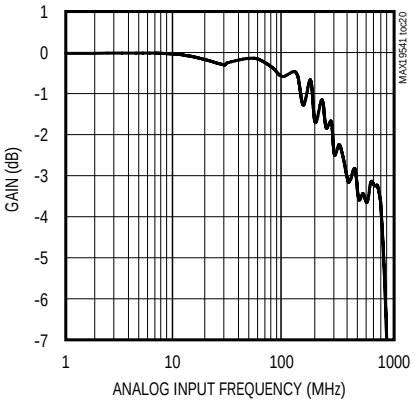
Typical Operating Characteristics (continued)

(AV_{CC} = OV_{CC} = 1.8V, AGND = OGND = 0, f_{SAMPLE} = 125MHz, A_{IN} = -1dBFS; see TOCs for detailed information on test conditions, differential input drive, differential LVPECL clock input drive, 0.1µF capacitor on REFIO, internal reference, digital outputs differential R_L = 100Ω, T_A = +25°C.)

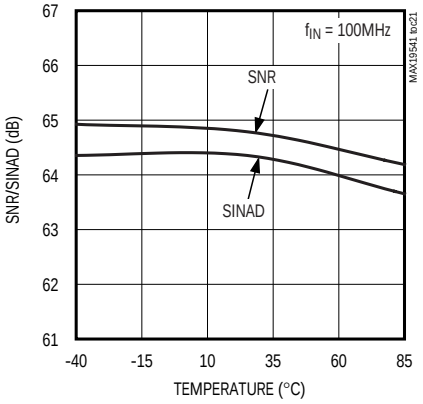
DNL vs. DIGITAL OUTPUT CODE (524k-POINT DATA RECORD)



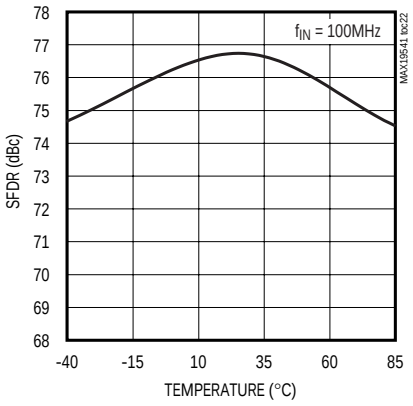
GAIN BANDWIDTH PLOT (f_{SAMPLE} = 125.0043232MHz, A_{IN} = -1dBFS)



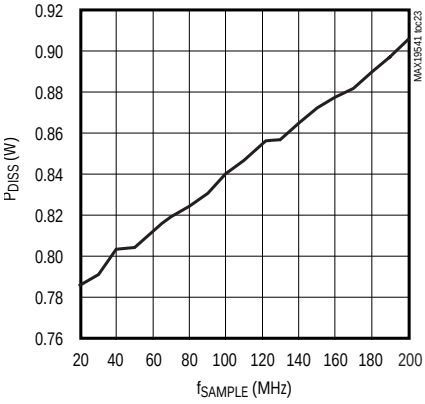
SNR/SINAD vs. TEMPERATURE (f_{SAMPLE} = 125MHz, A_{IN} = -2dBFS)



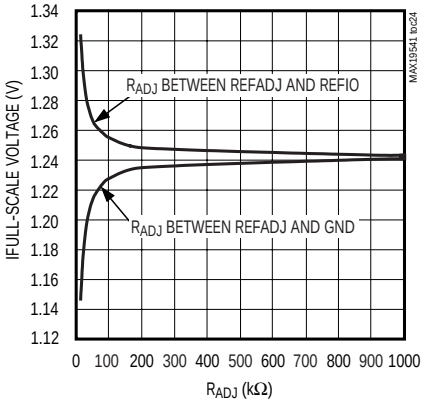
SFDR vs. TEMPERATURE (f_{SAMPLE} = 125MHz, A_{IN} = -2dBFS)



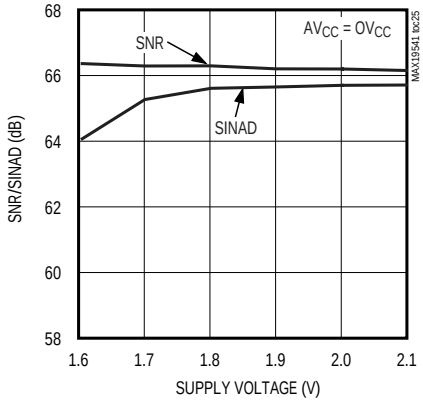
TOTAL POWER DISSIPATION vs. f_{SAMPLE} (f_{IN} = 60MHz, A_{IN} = -1dBFS)



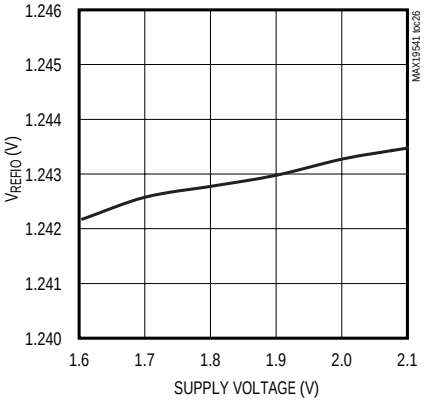
FULL-SCALE ADJUSTMENT RANGE vs. ADJUSTMENT RESISTANCE



SNR/SINAD vs. SUPPLY VOLTAGE (f_{IN} = 60.0225MHz, A_{IN} = -1dBFS)



INTERNAL REFERENCE vs. SUPPLY VOLTAGE



Pin Description

PIN	NAME	FUNCTION
1, 6, 11–14, 20, 25, 62, 63, 65	AV_{CC}	Analog Supply Voltage. Bypass each AV_{CC} pin with a 0.1µF capacitor for best decoupling results. Additional board decoupling might be required. See the *Grounding, Bypassing, and Layout Considerations* section.
2, 5, 7, 10, 18, 19, 21, 24, 64, 66	AGND	Analog Converter Ground. Connect the converter's exposed paddle (EP) to AGND.
3	REFIO	Reference Input/Output. Drive REFADJ high to allow an external reference source to be connected to the MAX19541. Drive REFADJ low to activate the internal 1.23V bandgap reference. Connect a 0.1µF capacitor from REFIO to AGND.
4	REFADJ	Reference Adjust Input. REFADJ allows for full-scale range adjustments by placing a resistor or trim potentiometer between REFADJ and AGND (decreases FS range) or REFADJ and REFIO (increases FS range). If REFADJ is connected to AV_{CC}, the internal reference can be overdriven with an external source connected to REFIO. If REFADJ is connected to AGND, the internal reference is used to determine the full-scale range of the data converter.
8	INP	Positive Analog Input Terminal
9	INN	Negative Analog Input Terminal
15	RESET	Active-High RESET Input. RESET controls the latency of the MAX19541. RESET has an internal pulldown resistor. See the *Reset Operation* section.
16	DEMUX	Output-Mode-Select Input. Drive DEMUX low for the parallel output mode (full-rate CMOS outputs on A ports only). Drive DEMUX high for the demux parallel or demux interleaved modes (half-rate outputs on both ports A and B) depending on the state of the ITL input. See the *Modes of Operation* section.
17	CLKDIV	Clock-Divider Input. CLKDIV is an LVCMOS-compatible input that controls the sampling frequency relative to the input clock frequency. CLKDIV has an internal pulldown resistor: CLKDIV = 0: sampling frequency is 1/2 the input clock frequency. CLKDIV = 1: sampling frequency is equal to the input clock frequency.
22	CLKN	Complementary Clock Input. CLKN ideally requires an LVPECL-compatible input level to maintain the converter's excellent performance.
23	CLKP	True Clock Input. CLKP ideally requires an LVPECL-compatible input level to maintain the converter's excellent performance.
26, 45, 61	OGND	Digital Converter Ground. Ground connection for digital circuitry and output drivers.
27, 28, 41, 44, 60	OV_{CC}	Digital Supply Voltage. Bypass OV_{CC} with a 0.1µF capacitor for best decoupling results. Additional board decoupling might be required. See the *Grounding, Bypassing, and Layout Considerations* section.
29	DB0	Port B CMOS Digital Output Bit 0 (LSB)
30	DB1	Port B CMOS Digital Output Bit 1
31	DB2	Port B CMOS Digital Output Bit 2
32	DB3	Port B CMOS Digital Output Bit 3
33	DB4	Port B CMOS Digital Output Bit 4
34	DB5	Port B CMOS Digital Output Bit 5
35	DB6	Port B CMOS Digital Output Bit 6
36	DB7	Port B CMOS Digital Output Bit 7
37	DB8	Port B CMOS Digital Output Bit 8

Pin Description (continued)

PIN	NAME	FUNCTION
38	DB9	Port B CMOS Digital Output Bit 9
39	DB10	Port B CMOS Digital Output Bit 10
40	DB11	Port B CMOS Digital Output Bit 11 (MSB)
42	DCLKN	Inverted CMOS Digital Clock Output. DCLKN provides a CMOS-compatible output level and can be used to synchronize external devices to the converter clock. When DEMUX is high, the frequency at DCLKN is half the sampling clock's frequency.
43	DCLKP	True CMOS Digital Clock Output. DCLKP provides a CMOS-compatible output level and can be used to synchronize external devices to the converter clock. When DEMUX is high, the frequency at DCLKP is half the sampling clock's frequency.
46	ORB	Port B CMOS Digital Output Overrange
47	DA0	Port A CMOS Digital Output Bit 0 (LSB)
48	DA1	Port A CMOS Digital Output Bit 1
49	DA2	Port A CMOS Digital Output Bit 2
50	DA3	Port A CMOS Digital Output Bit 3
51	DA4	Port A CMOS Digital Output Bit 4
52	DA5	Port A CMOS Digital Output Bit 5
53	DA6	Port A CMOS Digital Output Bit 6
54	DA7	Port A CMOS Digital Output Bit 7
55	DA8	Port A CMOS Digital Output Bit 8
56	DA9	Port A CMOS Digital Output Bit 9
57	DA10	Port A CMOS Digital Output Bit 10
58	DA11	Port A CMOS Digital Output Bit 11 (MSB)
59	ORA	Port A CMOS Digital Output Overrange
67	ITL	Interleaved/Parallel-Select Input. Drive ITL low for the demux parallel mode. Drive ITL high for the demux interleaved mode.
68	$\overline{T}$/B	Output-Format-Select Input. $\overline{T}$/B is an LVCMOS-compatible input that controls the digital output format of the MAX19541. $\overline{T}$/B has an internal pulldown resistor: $\overline{T}$/B = 1: binary output format. $\overline{T}$/B = 0: two's-complement output format.
EP	AGND	Exposed Paddle. Connect EP to the analog ground (AGND) for optimum performance. The exposed paddle is located on the backside of the chip. EP is internally connected to the die substrate.

12-Bit, 125Msps ADC with CMOS Outputs for Wideband Applications

Detailed Description—Theory of Operation

The MAX19541 uses a fully differential, pipelined architecture that allows for high-speed conversion, optimized accuracy and linearity, while minimizing power consumption. Both positive (INP) and negative/complementary analog input terminals (INN) are centered around a 1.365V common-mode voltage, and accept a ±350mV differential analog input voltage swing each, resulting in a typical 1.41V_{P-P} differential full-scale signal swing.

Inputs INP and INN are buffered prior to entering each track-and-hold (T/H) stage and are sampled when the differential sampling clock signal transitions high. The ADC following the first T/H stage then digitizes the signal, and controls a digital-to-analog converter (DAC). Digitized and reference signals are then subtracted, resulting in a fractional residue signal that is amplified before it is passed on to the next stage through another T/H amplifier. This process is repeated until the applied input signal has successfully passed through all stages of the 12-bit quantizer. Finally, the digital outputs of all stages are combined and corrected for in the digital correction logic to generate the final output code. The result is a 12-bit parallel digital output word in user-selectable two's complement or binary output formats with CMOS-compatible output levels. See the functional diagram (Figure 1) for a more detailed view of the MAX19541's architecture.

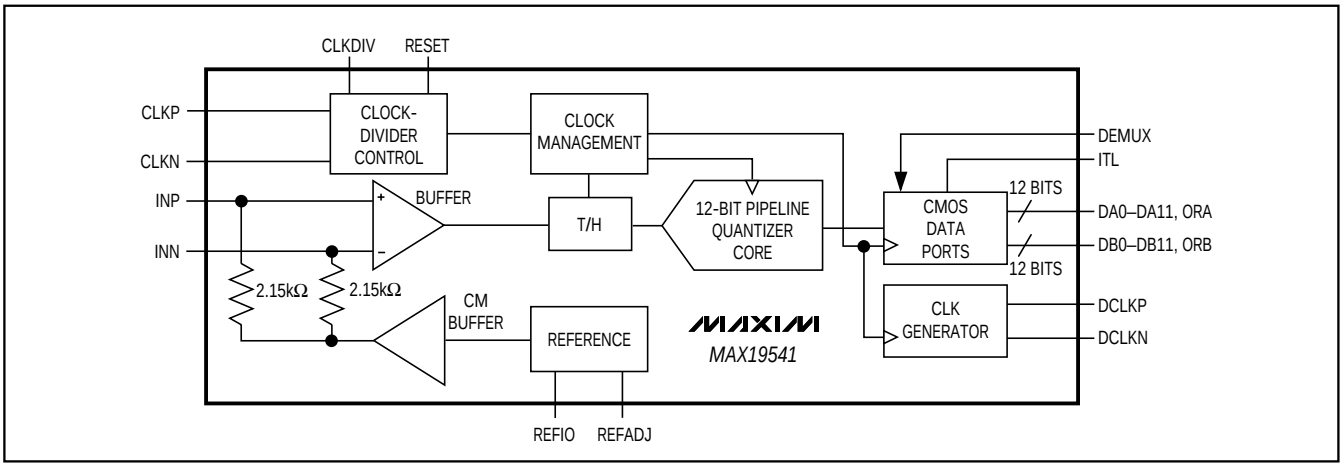


Figure 1. MAX19541 Functional Diagram

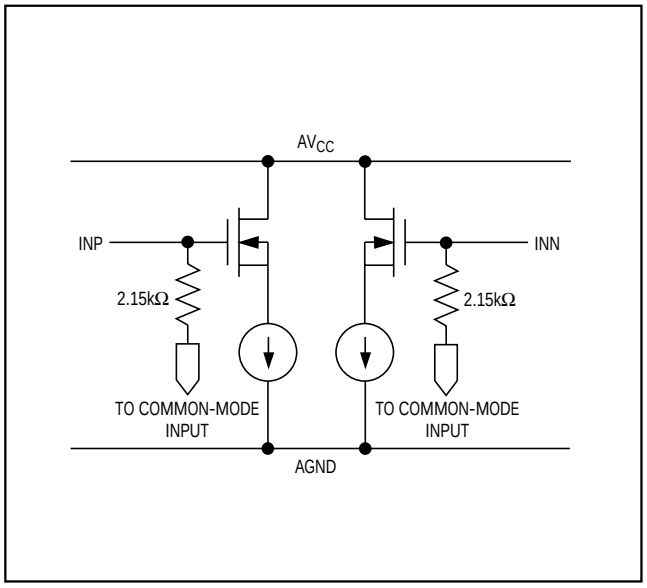


Figure 2. Simplified Analog Input Architecture

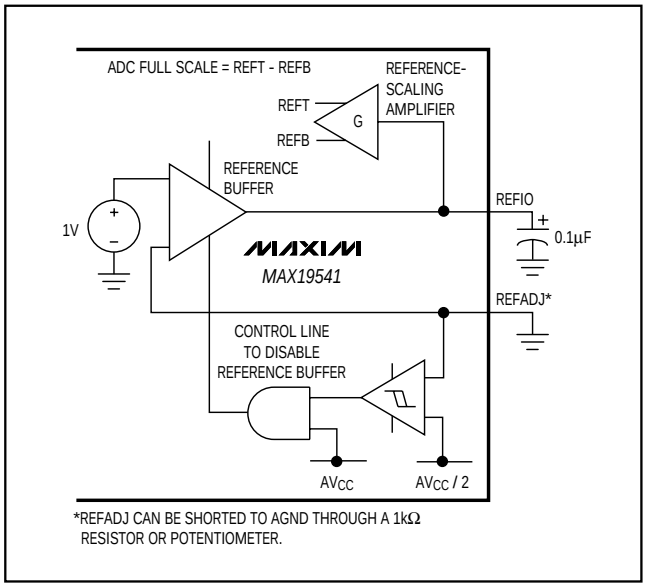


Figure 3. Simplified Reference Architecture

Analog Inputs (INP, INN)

INP and INN are the fully differential inputs of the MAX19541. Differential inputs usually feature good rejection of even-order harmonics, which allows for enhanced AC performance as the signals are progressing through the analog stages. The MAX19541 analog inputs are self-biased at a 1.365V common-mode voltage and allow a $1.41V_{P-P}$ differential input voltage swing. Both inputs are self-biased through 2.15kΩ resistors, resulting in a typical differential input resistance of 4.3kΩ (Figure 2). It is recommended driving the analog inputs of the MAX19541 in an AC-coupled configuration to achieve the best dynamic performance. See the *Transformer-Coupled, Differential Analog Input Drive* section for a detailed discussion of this configuration.

On-Chip Reference Circuit

The MAX19541 features an internal 1.24V bandgap reference circuit (Figure 3), which, in combination with an internal reference-scaling amplifier, determine the full-scale range of the MAX19541. Bypass REFIO with a 0.1µF capacitor to AGND. To compensate for gain errors or increase the ADC's full-scale range, the voltage of this bandgap reference can be indirectly adjusted by adding an external resistor (e.g., 100kΩ trim potentiometer) between REFADJ and AGND or REFADJ and REFIO. See Figure 8 and the *Applications Information* section for a detailed description of this process.

Clock Inputs (CLKP, CLKN)

Drive the clock inputs of the MAX19541 differentially with an LVPECL-compatible clock to achieve the best dynamic performance. The clock signal source must be high-quality, low phase noise to avoid any degradation in the noise performance of the ADC. The clock inputs (CLKP, CLKN) are internally biased to typically 1.15V, accept a typical $0.5V_{P-P}$ differential signal swing, and are usually driven in an AC-coupled configuration. See the *Differential, AC-Coupled Clock Input* section for more circuit details on how to drive CLKP and CLKN appropriately.

The MAX19541 features an internal clock-management circuit (duty-cycle equalizer). The clock-management circuit ensures that the clock signal applied to inputs CLKP and CLKN is processed to provide a near 50% duty-cycle clock signal. This desensitizes the performance of the converter to variations in the duty cycle of the input clock source. Note that the clock duty-cycle equalizer cannot be turned off externally.

Clock Outputs (DCLKP, DCLKN)

The MAX19541 features CMOS-complementary clock outputs (DCLKP, DCLKN) to latch the digital output data with an external latch or receiver. Additionally, the clock outputs can be used to synchronize external devices (e.g., FPGAs) to the ADC. There is a 2.1ns delay time between the rising (falling) edge of CLKP (CLKN) and the rising (falling) edge of DCLKP (DCLKN). See Figure 4 for timing details.

12-Bit, 125Msps ADC with CMOS Outputs for Wideband Applications

Divide-by-Two Clock Control (CLKDIV)

The MAX19541 offers a clock control line (CLKDIV) that allows the reduction of clock jitter and phase noise in a system as higher frequency oscillators usually exhibit better phase noise and jitter characteristics. Connect CLKDIV to OGND to enable the ADC's internal divide-by-2 clock divider, which allows the user to use an oscillator of twice the maximum sampling frequency. The sampling frequency now becomes 1/2 of the input clock frequency. CLKDIV has an internal pulldown resistor and can be left open for applications that require this divide-by-2 mode. Connecting CLKDIV to OV_{CC} disables the divide-by-2 mode.

RESET Operation

The RESET input defines the pipeline latency of the MAX19541. Drive RESET high to place the MAX19541 in reset mode with the CMOS outputs tri-stated. During the time when RESET is high, no sample information is available at the outputs. For pipeline latency, the first sample is defined at the first rising edge of CLKP after RESET goes low. The conversion information is available at the outputs after 11 clock cycles. Synchronize RESET with the input clock of the device by observing the minimum RESET hold (t_{HR}) and RESET setup (t_{SR}) times (Figure 4). RESET is only used to control the latency of the device and, in applications where this is not critical, drive RESET low or leave unconnected. RESET has an internal pulldown resistor.

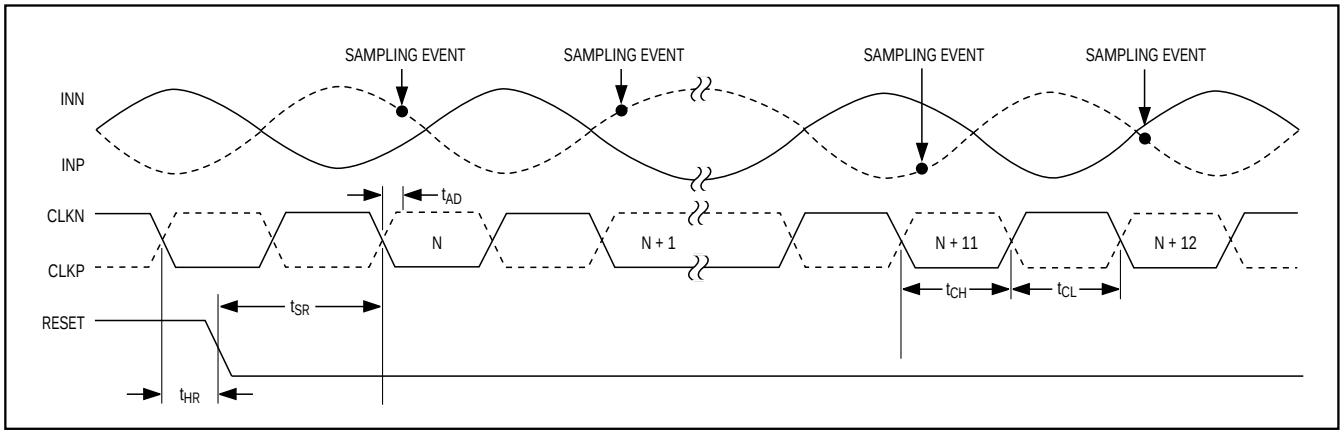


Figure 4. RESET Timing Diagram

System Timing Requirements

Figures 5, 6, and 7 depict the relationship between the clock input and output, analog input, sampling event, and data output. The MAX19541 samples on the rising (falling) edge of CLKP (CLKN). In all these figures, CLKDIV is assumed to be high; otherwise, the sampling events would occur at every other rising edge of CLKP. Output data is latched on the next rising (falling) edge of the DCLKP (DCLKN) clock, but has an internal latency of 11 input clock cycles.

Modes of Operation

The MAX19541 features three modes of operation. In each mode of operation, the conversion data is output in a different format.

Parallel Mode

Drive DEMUX low to place the MAX19541 in the parallel mode. In this mode, the output clock has the same frequency as the sampling frequency and conversion data is output at full rate on parallel ports DA0–DA11. Note that the sampling frequency may not be the same as the input clock frequency. See the *Divide-by-Two Clock Control (CLKDIV)* section. In parallel mode, samples are taken on the rising edge of CLKP. Conversion data appears at the outputs on the rising edge of DCLKP after the latency period of 11 clock cycles and is stable for one clock period (Figure 5). If an overrange condition occurs, it is reflected on the ORA port.

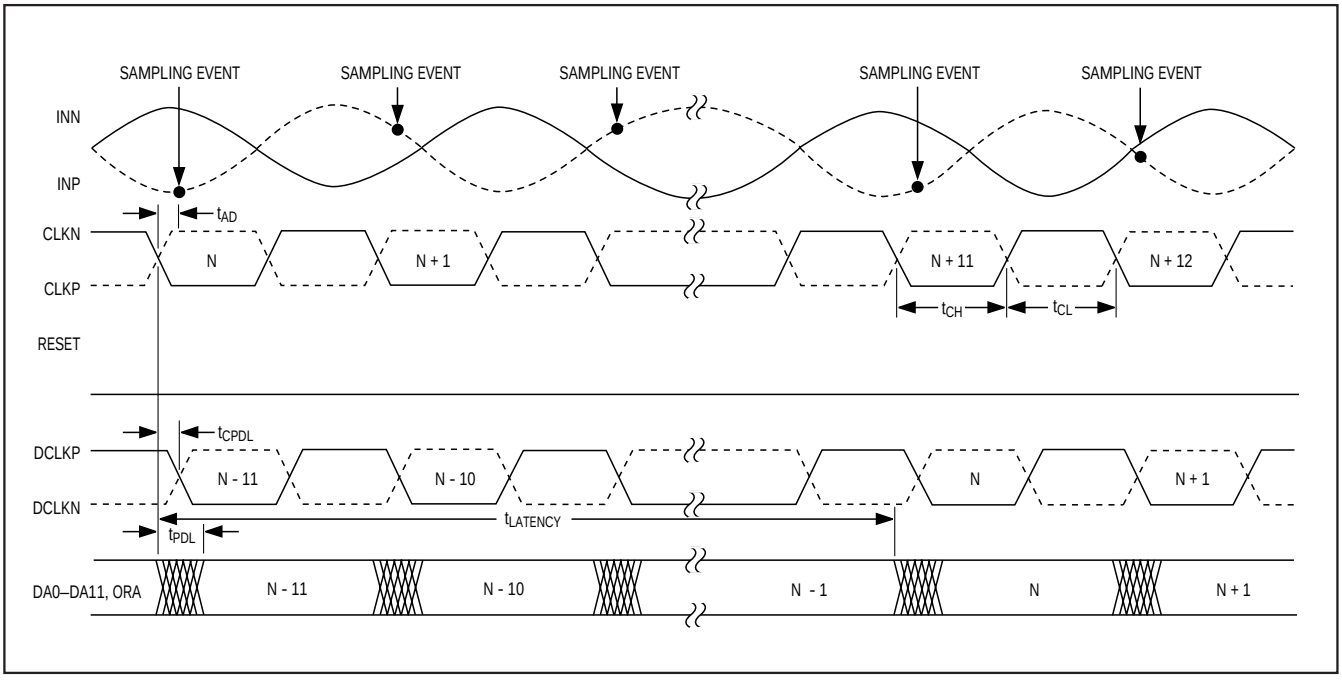


Figure 5. Parallel Mode Timing Diagram

12-Bit, 125Msps ADC with CMOS Outputs for Wideband Applications

Demux Parallel Mode

Drive DEMUX high and ITL low to place the MAX19541 in the demux parallel mode. In this mode, the output clock's frequency is 1/2 the sampling frequency. The sampling frequency may not be the same as the input clock frequency. See the *Divide-by-Two Clock Control (CLKDIV)* section. Each conversion starts with a sampling event on the rising edge of CLKP. Conversion data now appears on both DA0–DA11 and DB0–DB11. The first conversion result is output on the A ports on the rising edge of DCLKP after 12 input clock cycles from the initial sampling event. The second conversion result is output on the B ports on the rising edge of DCLKP after 11 input clock cycles from the initial sampling event. Both conversion results are output simultaneously (Figure 6). The conversion results on ports A and B remain stable for one period of DCLKP after they become valid. Thus, the overall throughput rate is the same as in parallel mode; however, now each data line is allowed to be valid for a longer time (two sampling periods, one digital clock period). Overrange conditions are reflected on the appropriate output port, ORA or ORB, depending on which conversion they occur.

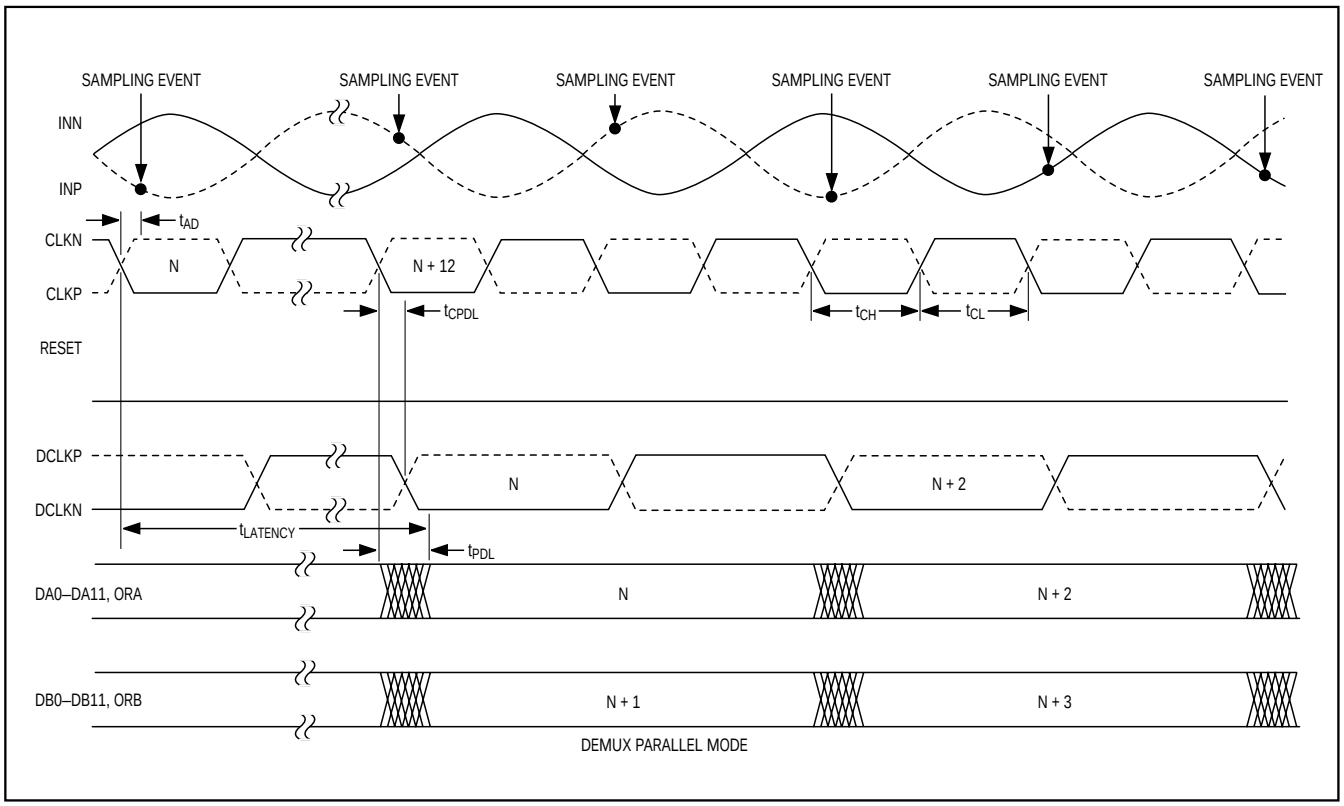


Figure 6. Demux Parallel Mode Timing Diagram

Demux Interleaved Mode

Drive DEMUX high and ITL high to place the MAX19541 in the demux interleaved mode of operation. In this mode, the output clock's frequency is 1/2 the sampling frequency. The sampling frequency may not be the same as the input clock frequency. See the *Divide-by-Two Clock Control (CLKDIV)* section. Each conversion starts with a sampling event on the rising edge of CLKP. Conversion data now appears on both DA0–DA11 and DB0–DB11. The first conversion result is output on the A ports on the rising edge of DCLKP after 12 input clock cycles from the initial sampling event. The second conversion result is output on the B ports on the rising edge of DCLKN after 12 input clock cycles from the initial sampling event. In this way, the two conversion results are interleaved with respect to each other (Figure 7). The conversion results on ports A and B remain stable for one period of DCLKP and DCLKN, respectively, after they become valid. Overrange conditions are reflected on the appropriate output port, ORA or ORB, depending on which conversion they occur. The demux interleaved mode is the recommended demux mode of operation due to the fact that output bus switching is more evenly distributed over sample clock edges.

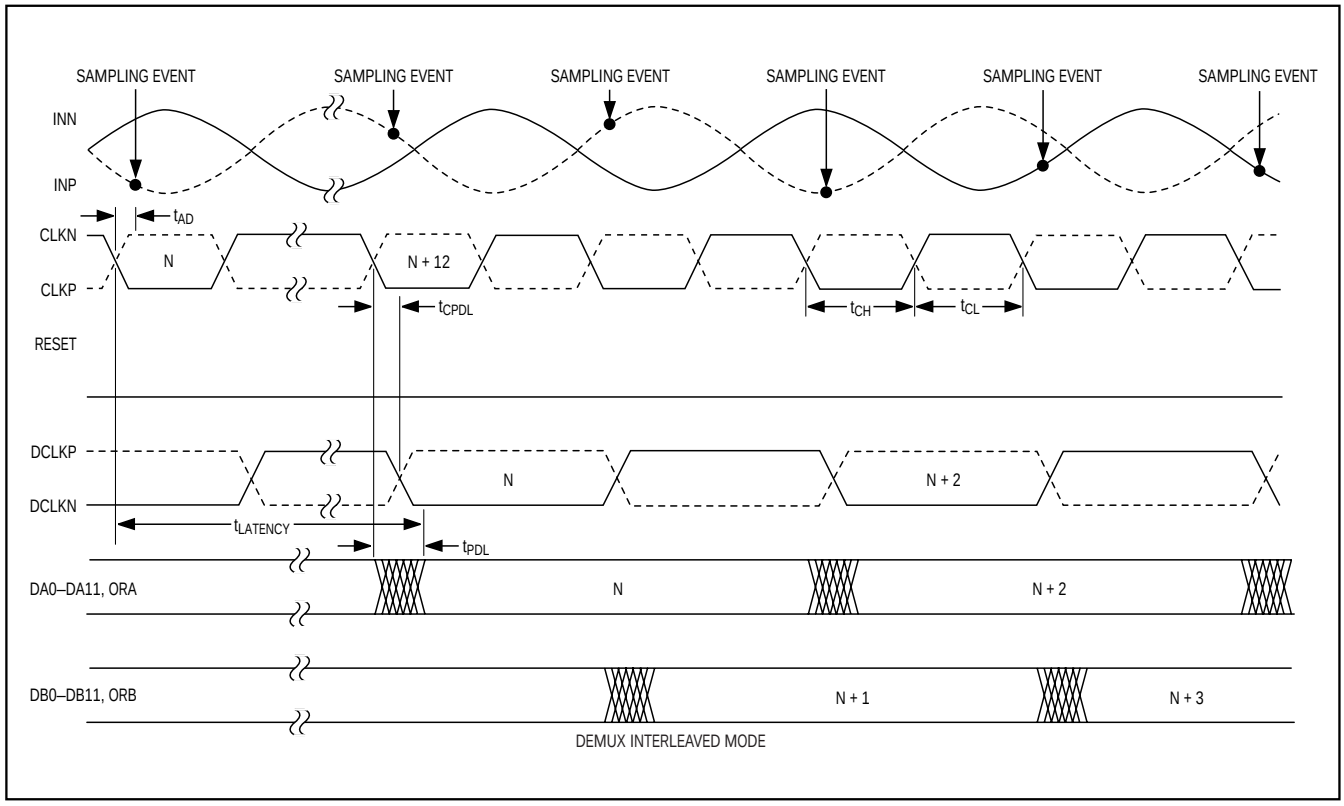


Figure 7. Demux Interleaved Mode Timing Diagram

12-Bit, 125Msps ADC with CMOS Outputs for Wideband Applications

Digital Outputs (DA0–DA11, DCLKP, DCLKN, ORA, DB0–DB11, ORB) and Control Input T/B

Digital outputs DA0/DB0–DA11/DB11, DCLKP, DCLKN, ORA/ORB are CMOS compatible, and data on DA0/DB DA11/DB11 are presented in either binary or two's-complement format (Table 1). The T/B control line is an LVCMOS-compatible input that allows the user to select the desired output format. Drive T/B high to select data to be output in offset binary format and drive it low to select data to be output in two's complement format on the 12-bit parallel bus. T/B has an internal pulldown resistor and can be left unconnected in applications using only two's-complement output format. The CMOS outputs are powered from a separate power supply that can be operated between 1.7V and 1.9V.

The MAX19541 offers an additional differential output pair (ORA, ORB) to flag overrange conditions, where overrange is above positive or below negative full scale. An overrange condition is identified with ORA/ORB transitioning high.

Note: Keep the capacitive load on the digital outputs as low as possible. Use digital buffers on the digital outputs of the ADC when driving larger loads to improve overall performance and reduce system timing constraints. Further improvements in dynamic performance can be achieved by adding small series resistors (100Ω) to the digital output paths, close to the ADC.

Table 1. MAX19541 Digital Output Coding

INP ANALOG INPUT VOLTAGE LEVEL	INN ANALOG INPUT VOLTAGE LEVEL	OVERRANGE ORA/ORB	BINARY DIGITAL OUTPUT CODE (D_11–D_0)	TWO'S-COMPLEMENT DIGITAL OUTPUT CODE (D_11–D_0)
> V_{REF} + 0.35V	< V_{REF} - 0.35V	1	1111 1111 1111 (exceeds +FS, OR set)	0111 1111 1111 (exceeds +FS, OR set)
V_{REF} + 0.35V	V_{REF} - 0.35V	0	1111 1111 1111 (+FS)	0111 1111 1111 (+FS)
V_{REF}	V_{REF}	0	1000 0000 0000 or 0111 1111 1111 (FS/2)	0000 0000 0000 or 1111 1111 1111 (FS/2)
V_{REF} - 0.35V	V_{REF} + 0.35V	0	0000 0000 0000 (-FS)	1000 0000 0000 (-FS)
< V_{REF} + 0.35V	> V_{REF} - 0.35V	1	00 0000 0000 (exceeds -FS, OR set)	10 0000 0000 (exceeds -FS, OR set)

Applications Information

Full-Scale Range Adjustments Using the Internal Bandgap Reference

The MAX19541 supports a full-scale adjustment range of ±10%. To decrease the full-scale range, an external resistor value ranging from 13kΩ to 1MΩ can be added between REFADJ and AGND. A similar approach can be taken to increase the ADCs full-scale range. Add a variable resistor, potentiometer, or predetermined resistor value between REFADJ and REFIO to increase the full-scale range of the data converter. Figure 8 shows the two possible configurations and their impact on the overall full-scale range adjustment of the MAX19541. Do not use resistor values of less than 13kΩ to avoid instability of the internal gain regulation loop for the bandgap reference. Use the following formula to calculate the percentage change of the reference voltage:

$$V_{REF}\ (\%) = 1.25\% \times \frac{100k\Omega}{R_{ADJ}}$$

The percentage change is positive when R_{ADJ} is added between REFADJ and REFIO, and is negative when R_{ADJ} is added between REFADJ and GND.

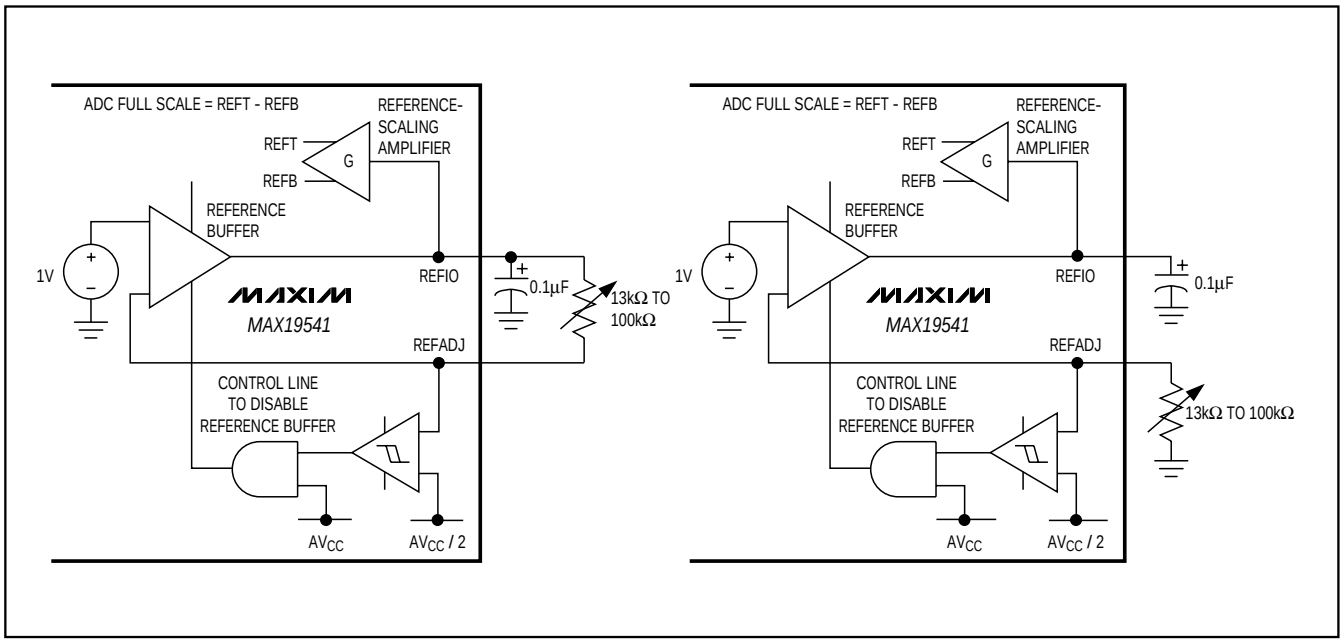


Figure 8. Circuit Suggestions to Adjust the ADC's Full-Scale Range (Simplified Schematic)

12-Bit, 125Msps ADC with CMOS Outputs for Wideband Applications

Differential, AC-Coupled, LVPECL-Compatible Clock Input

The MAX19541 dynamic performance depends on a very clean clock source. The phase noise floor of the clock source has a negative impact on the SNR performance. Spurious signals on the clock signal source also affect the ADC's dynamic range. The preferred method of clocking the MAX19541 is differentially with LVPECL-compatible input levels. The fast data transition rates of these logic families minimize the clock-input circuitry's transition uncertainty, thereby improving the SNR performance. Apply a 50Ω reverse-terminated clock signal source with low phase noise AC-coupled into a fast differential receiver such as the MC100LVEL16 (Figure 9). The receiver produces the necessary LVPECL output levels to drive the clock inputs of the data converter.

Transformer-Coupled, Differential Analog Input Drive

The MAX19541 provides the best SFDR and THD with fully differential input signals and it is not recommended driving the ADC inputs in single-ended configuration. In differential input mode, even-order harmonics are usually lower since INP and INN are balanced, and each of the ADC inputs requires only half the signal swing compared to a single-ended configuration. Wideband RF transformers provide an excellent solution to convert a single-ended source signal to a fully differential signal, required by the MAX19541 for optimum dynamic performance.

A secondary-side termination of a 1:1 transformer (e.g., Mini-Circuit's ADT1-1WT) into two separate 24.9Ω ±0.1% resistors (use tight resistor tolerances to minimize effects of imbalance; 0.1% would be an ideal choice) placed between top/bottom and center tap of the transformer is recommended to maximize the ADC's dynamic range. This configuration optimizes THD and SFDR performance of the ADC by reducing the effects of transformer parasitics. However, the source impedance combined with the shunt capacitance provided by a PC board and the ADC's parasitic capacitance limit the ADC's full-power input bandwidth to approximately 600MHz.

To further enhance THD and SFDR performance at high input frequencies (>100MHz), a second transformer (Figure 10) should be placed in series with the single-ended-to-differential conversion transformer. This transformer reduces the increase of even-order harmonics at high frequencies.

For more detailed information on transformer termination methods, refer to the Application Note: *Secondary-Side Transformer Termination Improves Gain Flatness in High-Speed ADCs* from the Maxim website: www.maxim-ic.com.

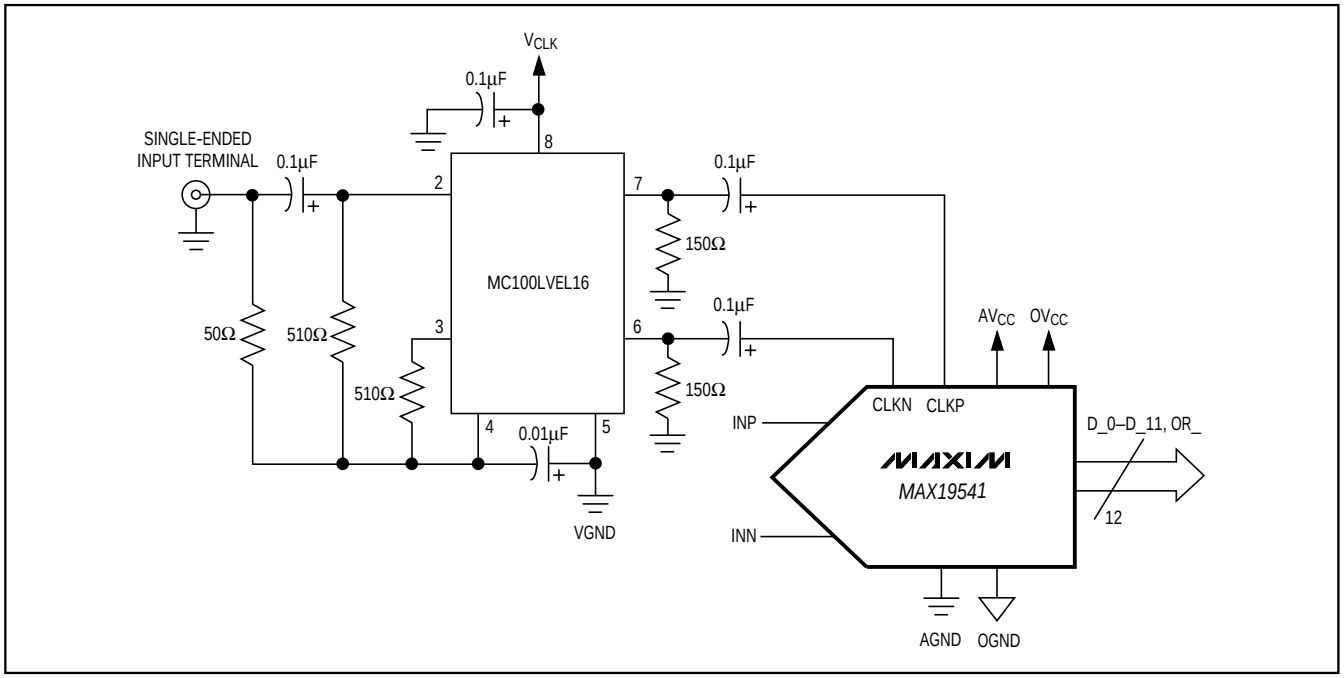


Figure 9. Differential, AC-Coupled, LVPECL-Compatible Clock Input Configuration

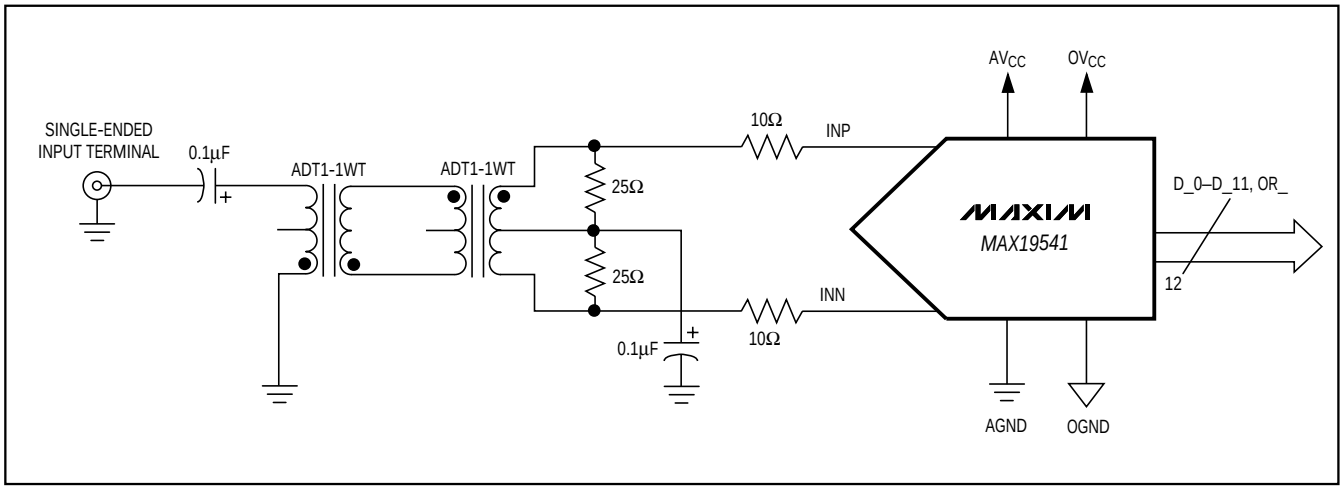


Figure 10. Analog Input Configuration with Back-to-Back Transformers and Secondary-Side Termination

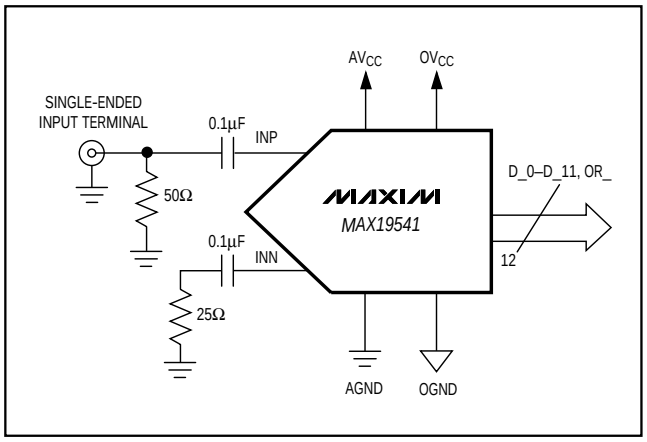


Figure 11. Single-Ended AC-Coupled Analog Input Configuration

Single-Ended, AC-Coupled Analog Input

Although not recommended, the MAX19541 can be used in single-ended mode (Figure 11). Analog signals can be AC-coupled to the positive input INP through a 0.1µF capacitor and terminated with a 49.9Ω resistor to AGND. Terminate the negative input with a 24.9Ω resistor and AC ground it with a 0.1µF capacitor.

Grounding, Bypassing, and Board Layout Considerations

The MAX19541 requires board layout design techniques suitable for high-speed data converters. This ADC provides separate analog and digital power supplies. The analog and digital supply voltage inputs AV_{CC} and OV_{CC} accept 1.7V to 1.9V input voltage ranges. Although both supply types can be combined and supplied from one source, it is recommended using separate sources to cut down on performance degradation caused by digital switching currents that can couple into the analog supply network. Isolate analog and digital supplies (AV_{CC} and OV_{CC}) where they enter the PC board with separate networks of ferrite beads and capacitors to their corresponding grounds (AGND, OGND).

To achieve optimum performance, provide each supply with a separate network of a 47µF tantalum capacitor in parallel with 10µF and 1µF ceramic capacitors. Additionally, the ADC requires each supply pin to be bypassed with separate 0.1µF ceramic capacitors (Figure 12). Locate these capacitors directly at the ADC supply pins or as close as possible to the MAX19541. Choose surface-mount capacitors, whose preferred location should be on the same side as the converter, to save space and minimize the inductance. If close placement on the same side is not possible, these bypassing capacitors may be routed through vias to the bottom side of the PC board.

Multilayer boards with separated ground and power planes produce the highest level of signal integrity. Consider the use of a split ground plane arranged to match the physical location of analog and digital ground on the ADC's package. The two ground planes should be joined at a single point so the noisy digital ground currents do not interfere with the analog ground plane. A major concern with this approach are the dynamic currents that may need to travel long distances before they are recombined at a common source ground, resulting in large and undesirable

ground loops. Ground loops can add to digital noise by coupling back to the analog front end of the converter, resulting in increased spur activity and a decreased noise performance.

Alternatively, all ground pins could share the same ground plane if the ground plane is sufficiently isolated from any noisy, digital systems ground. To minimize the effects of digital noise coupling, ground return vias can be positioned throughout the layout to divert digital switching currents away from the sensitive analog sections of the ADC. This does not require additional ground splitting, but can be accomplished by placing substantial ground connections between the analog front end and the digital outputs.

The MAX19541 is packaged in a 68-pin QFN-EP package (package code: G6800-4), providing greater design flexibility, increased thermal dissipation, and optimized AC performance of the ADC. The EP must be soldered down to AGND.

In this package, the data converter die is attached to an EP lead frame with the back of this frame exposed at the package bottom surface, facing the PC board side of the package. This allows a solid attachment of the package to the board with standard infrared (IR) flow-soldering techniques.

Thermal efficiency is one of the factors for the selection of a package with an exposed pad for the MAX19541. The exposed pad improves thermal dissipation and ensures a solid ground connection between the ADC and the PC board's analog ground layer.

Take considerable care when routing the digital output traces for a high-speed, high-resolution data converter. It is essential to keep trace lengths at a minimum and place minimal capacitive loading—less than 5pF—on any digital trace to prevent coupling to sensitive analog sections of the ADC. Route high-speed digital signal traces away from sensitive analog traces, and remove digital ground and power planes from underneath digital outputs. Keep all signal lines short and free of 90° turns.

Static Parameter Definitions

Integral Nonlinearity (INL)

Integral nonlinearity is the deviation of the values on an actual transfer function from a straight line. This straight line can be either a best straight-line fit or a line drawn between the end points of the transfer function, once offset and gain errors have been nullified. However, the static linearity parameters for the MAX19541 are measured using the histogram method with a 10MHz input frequency.

Differential Nonlinearity (DNL)

Differential nonlinearity is the difference between an actual step width and the ideal value of 1 LSB. A DNL error specification of less than 1 LSB guarantees no missing codes and a monotonic transfer function. The MAX19541's DNL specification is measured with the histogram method based on a 10MHz input tone.

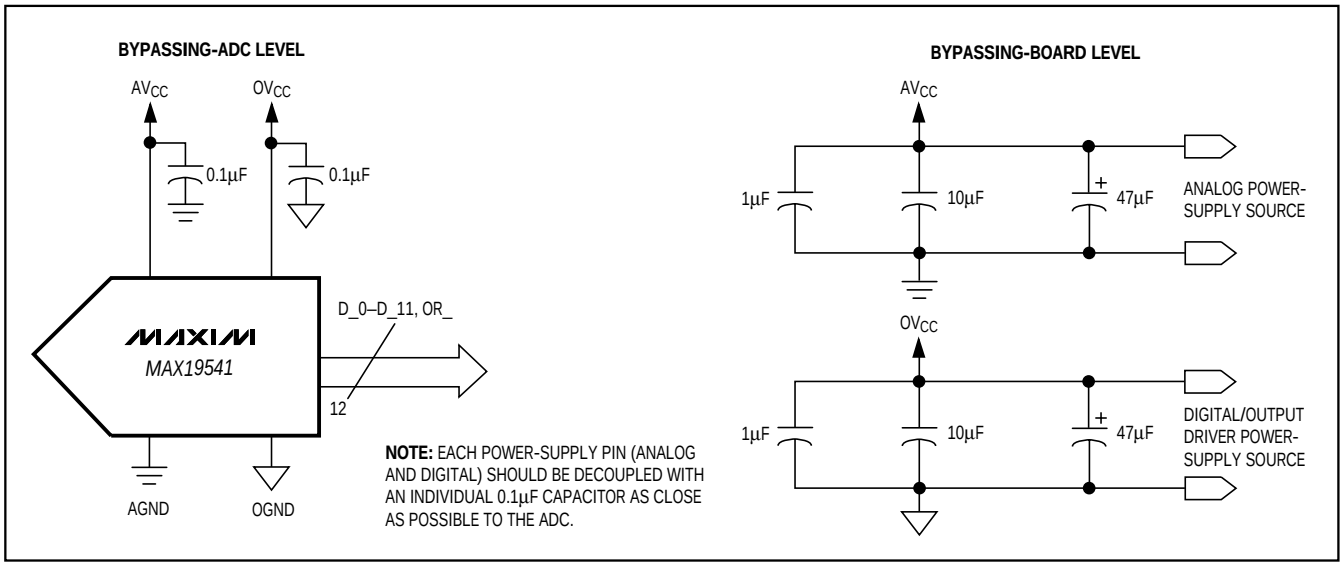


Figure 12. Grounding, Bypassing, and Decoupling Recommendations for the MAX19541

Dynamic Parameter Definitions

Aperture Jitter

Figure 13 depicts the aperture jitter (t_{AJ}), which defines the sample-to-sample variation in the aperture delay. Aperture jitter is measured in ps_{RMS}.

Aperture Delay

Aperture delay (t_{AD}) is the time defined between the 620ps rising edge of the sampling clock and the instant when an actual sample is taken (Figure 13).

Signal-to-Noise Ratio (SNR)

For a waveform perfectly reconstructed from digital samples, the theoretical maximum SNR is the ratio of the full-scale analog input (RMS value) to the RMS quantization error (residual error). The ideal, theoretical minimum analog-to-digital noise is caused by quantization error only and results directly from the ADC's resolution (N bits):

$$SNR_{dB[max]} = 6.02_{dB} \times N + 1.76_{dB}$$

In reality, other noise sources such as thermal noise, clock jitter, signal phase noise, and transfer function nonlinearities are also contributing to the SNR calculation and should be considered when determining the SNR of an ADC.

Signal-to-Noise Plus Distortion (SINAD)

SINAD is computed by taking the ratio of the RMS signal to all spectral components excluding the fundamental and the DC offset. In the case of the MAX19541, SINAD is computed from a curve fit.

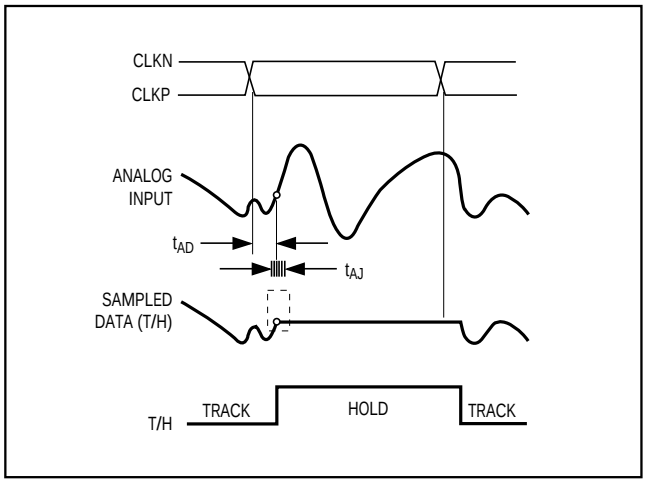


Figure 13. Aperture Jitter/Delay Specifications

Spurious-Free Dynamic Range (SFDR)

SFDR is the ratio of RMS amplitude of the carrier frequency (maximum signal component) to the RMS value of the next-largest noise or harmonic distortion component. SFDR is usually measured in dBc with respect to the carrier frequency amplitude or in dBFS with respect to the ADC's full-scale range.

Two-Tone Intermodulation Distortion (IMD)

The two-tone IMD is the ratio expressed in decibels of either input tone to the worst 2nd-order (or higher) intermodulation products. The individual input tone levels are usually set to 7dB below full scale and intermodulation products IM2 through IM5 are considered for the IMD calculation. The various intermodulation products are defined as follows:

- 2nd-order intermodulation distortion (IM2):
  $f_{IN1} + f_{IN2}$, $f_{IN2} - f_{IN1}$
- 3rd-order intermodulation distortion (IM3):
  $2f_{IN1} + f_{IN2}$, $2f_{IN1} - f_{IN2}$, $2f_{IN2} + f_{IN1}$, $2f_{IN2} - f_{IN1}$
- 4th-order intermodulation distortion (IM4):
  $3f_{IN1} + f_{IN2}$, $3f_{IN1} - f_{IN2}$, $3f_{IN2} + f_{IN1}$, $3f_{IN2} - f_{IN1}$
- 5th-order intermodulation distortion (IM5):
  $4f_{IN1} + f_{IN2}$, $4f_{IN1} - f_{IN2}$, $4f_{IN2} + f_{IN1}$, $4f_{IN2} - f_{IN1}$

Full-Power Bandwidth

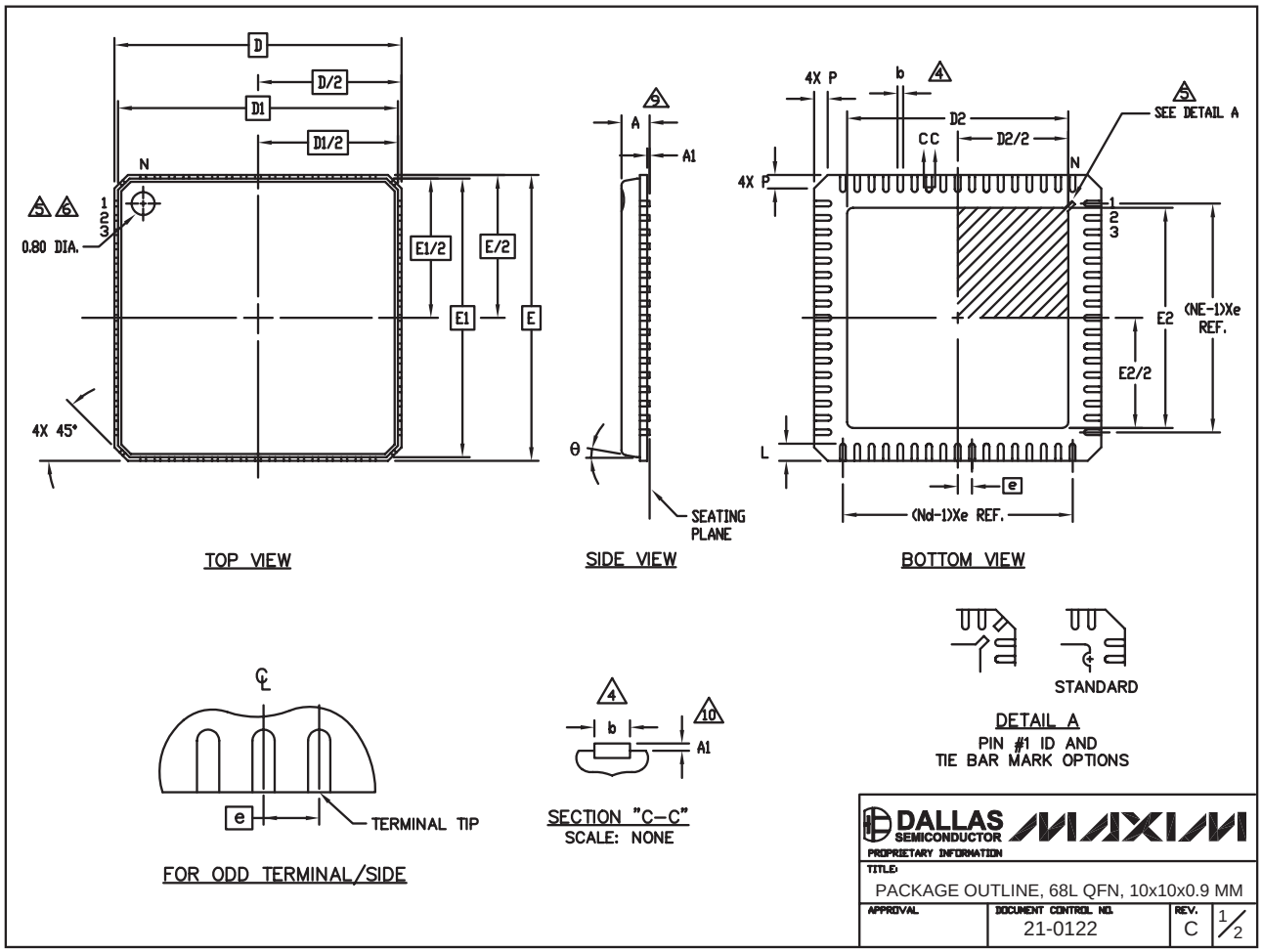
A large -1dBFS analog input signal is applied to an ADC and the input frequency is swept up to the point where the amplitude of the digitized conversion result has decreased by 3dB. The -3dB point is defined as the full-power input bandwidth frequency of the ADC.

12-Bit, 125Msps ADC with CMOS Outputs for Wideband Applications

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)

68L QFN.EPS



Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)

SYMBOL	COMMON DIMENSIONS			NOTE
	MIN.	NOM.	MAX.	
A	–	0.90	1.00	
A1	0.00	0.01	0.05	11
b	0.18	0.23	0.30	4
D	10.00 BSC			
D1	9.75 BSC			
e	0.50 BSC			
E	10.00 BSC			
E1	9.75 BSC			
L	0.50	0.60	0.65	
N	68			3
Nd	17			3
Ne	17			3
θ	0		12°	
P	0	0.42	0.60	

1. DIE THICKNESS ALLOWABLE IS .012 INCHES MAXIMUM.
2. DIMENSIONING & TOLERANCES CONFORM TO ASME Y14.5M. – 1994.
3. N IS THE NUMBER OF TERMINALS.
   Nd IS THE NUMBER OF TERMINALS IN X-DIRECTION &
   Ne IS THE NUMBER OF TERMINALS IN Y-DIRECTION.
4. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.20 AND 0.25mm FROM TERMINAL TIP.
5. THE PIN #1 IDENTIFIER MUST BE LOCATED ON THE TOP SURFACE OF THE PACKAGE BY USING INDENTATION MARK OR OTHER FEATURE OF PACKAGE BODY. DETAILS OF PIN #1 IDENTIFIER IS OPTIONAL, BUT MUST BE LOCATED WITHIN ZONE INDICATED.
6. EXACT SHAPE AND SIZE OF THIS FEATURE IS OPTIONAL.
7. ALL DIMENSIONS ARE IN MILLIMETERS.
8. PACKAGE WARPAGE MAX 0.10mm.
9. APPLIES TO EXPOSED SURFACE OF PADS AND TERMINALS
10. APPLIES ONLY TO TERMINALS.
11. MEETS JEDEC MO-220.

EXPOSED PAD VARIATIONS						
	D2			E2		
PKG CODE	MIN	NOM	MAX	MIN	NOM	MAX
G6800-2	7.55	7.70	7.85	7.55	7.70	7.85
G6800-4	5.65	5.80	5.95	5.65	5.80	5.95

DALLAS SEMICONDUCTOR MAXIM

PROPRIETARY INFORMATION

TITLE: PACKAGE OUTLINE, 68L QFN, 10x10x0.9 MM

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0122	C	1/2