# PTN3300A

## DVI/HDMI level shifter with inverting 1.1 V HPD

Rev. 01 — 30 June 2008 Product data sheet

## 1. General description

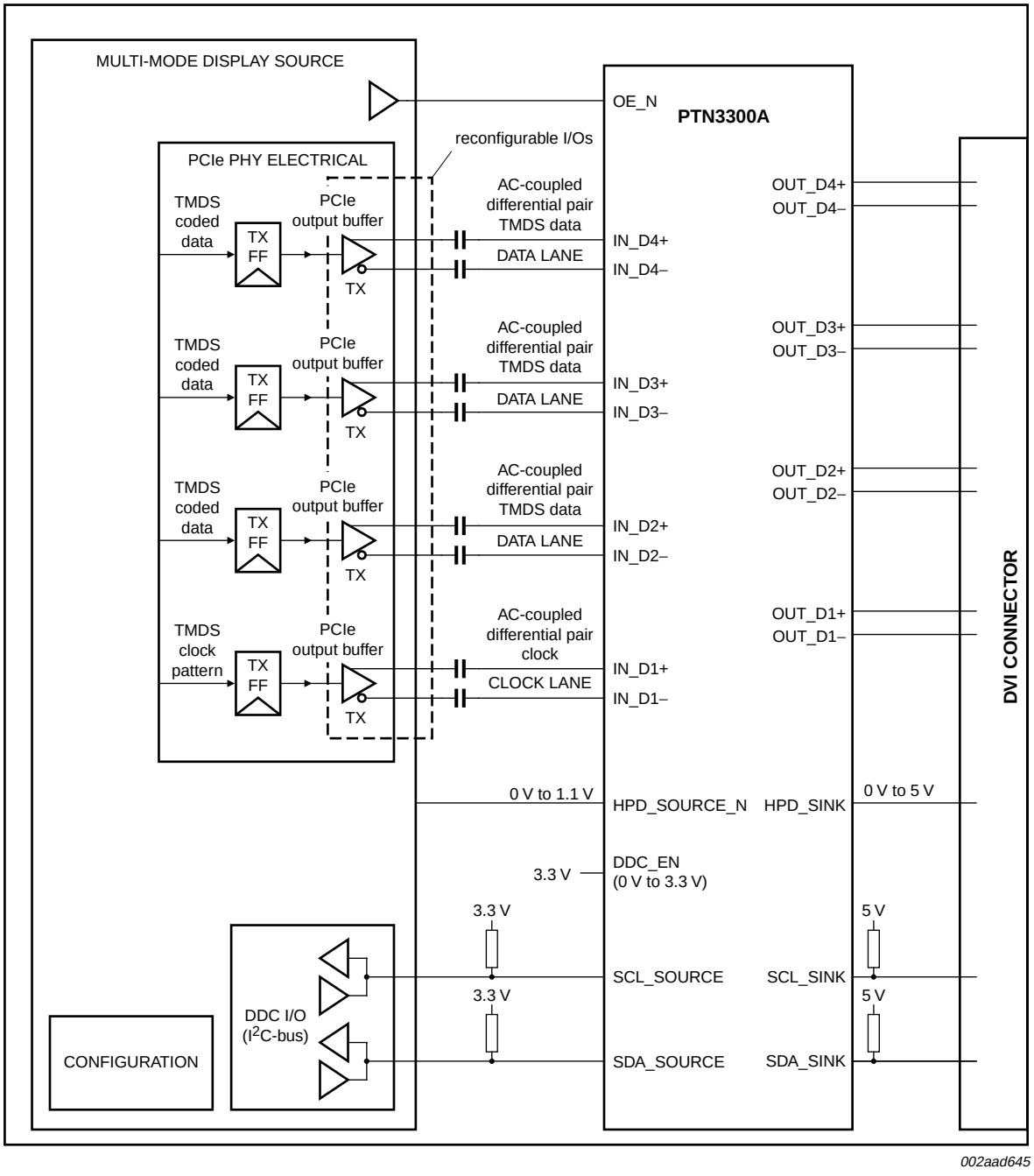
The PTN3300A is a high-speed level shifter device which converts four lanes of low-swing AC-coupled differential input signals to DVI and HDMI compliant open-drain current-steering differential output signals, up to 2.25 Gbit/s per lane. Each of these lanes provides a level-shifting differential buffer to translate from low-swing AC-coupled differential signaling on the source side, to TMDS-type DC-coupled differential current-mode signaling terminated into 50 Ω to 3.3 V on the sink side. Additionally, the PTN3300A provides a single-ended active inverting buffer for voltage translation of the HPD signal from 5 V on the sink side to 1.1 V on the source side and provides a channel for level shifting of the DDC channel (consisting of a clock and a data line) between 3.3 V source-side and 5 V sink-side. The DDC channel is implemented using pass gate technology allowing level shifting as well as disablement (isolation between source and sink) of the clock and data lines.

The low-swing AC-coupled differential input signals to the PTN3300A typically come from a display source with multi-mode I/O, which supports multiple display standards, e.g., DisplayPort, HDMI and DVI. While the input differential signals are configured to carry DVI or HDMI coded data, they do not comply with the electrical requirements of the DVI v1.0 specification or HDMI v1.3a specification. By using PTN3300A, chip set vendors are able to implement such reconfigurable I/Os on multi-mode display source devices, allowing the support of multiple display standards while keeping the number of chip set I/O pins low. See Figure 1.

The PTN3300A main high-speed differential lanes feature low-swing self-biasing differential inputs which are compliant to the electrical specifications of *DisplayPort Standard v1.1* and/or *PCI Express Standard v1.1*, and open-drain current-steering differential outputs compliant to DVI v1.0 and HDMI V1.3a electrical specifications. The PTN3300A also supports power-saving modes in order to minimize current consumption when no display is active or connected.

The PTN3300A supports level translation functions and features supporting DVI and HDMI. It is identical to the PTN3300B except that the HPD_SOURCE_N output is the logic inverse function of input HPD_SINK, level shifted to 1.1 V. For a fully-featured HDMI/DVI level shifter function that supports active buffering of the DDC lines and HDMI dongle detect, the PTN3301 should be used.

PTN3300A is powered from a single 3.3 V power supply consuming a small amount of power (120 mW typ.) and is offered in two different 48-terminal HWQFN packages, one laminate based (no terminals visible from edge of the package), and one leadframe-based (terminals visible from edge of the package).




**Remark:** TMDS clock and data lanes can be assigned arbitrarily and interchangeably to D[4:1].

**Fig 1. Typical application system diagram**

# 2. Features

## 2.1 High-speed TMDS level shifting

- Converts four lanes of low-swing AC-coupled differential input signals to DVI and HDMI compliant open-drain current-steering differential output signals
- TMDS level shifting operation up to 2.25 Gbit/s per lane (225 MHz character clock)
- Integrated 50 Ω termination resistors for self-biasing differential inputs
- Back-current safe outputs to disallow current when device power is off and monitor is on
- Disable feature to turn off TMDS inputs and outputs and to enter low-power state

## 2.2 DDC level shifting

- Integrated DDC level shifting (3.3 V source to 5 V sink side)
- 0 Hz to 400 kHz clock frequency
- Back-power safe to disallow backdrive current when power is off or when DDC is not enabled

## 2.3 HPD level shifting

- HPD **inverting** level shift from 0 V on the sink side to 1.1 V on the source side, or from 5 V on the sink side to 0 V on the source side
- Integrated 200 kΩ pull-down resistor on HPD sink input guarantees ‘input LOW’ when no display is plugged in

## 2.4 General

- Power supply 3.3 V ± 10 %
- ESD resilience to 3.5 kV HBM, 1 kV CDM
- Power-saving modes by source-side disablement (using output enable) as well as sink-side detection (using HPD)
- Back-current-safe design on all sink-side terminals
- Transparent operation: no re-timing or software configuration required

# 3. Ordering information

**Table 1. Ordering information**

| Type number | Package | | |
|---|---|---|---|
| | Name | Description | Version |
| PTN3300AHF | HWQFN48R | plastic thermal enhanced very very thin quad flat package; no leads; 48 terminals; resin based; body 7 × 7 × 0.7 mm | SOT1031-2 |
| PTN3300AHF2 | HWQFN48 | plastic thermal enhanced very very thin quad flat package; no leads; 48 terminals; body 7 × 7 × 0.65 mm | SOT1074-1 |

# 4. Functional diagram

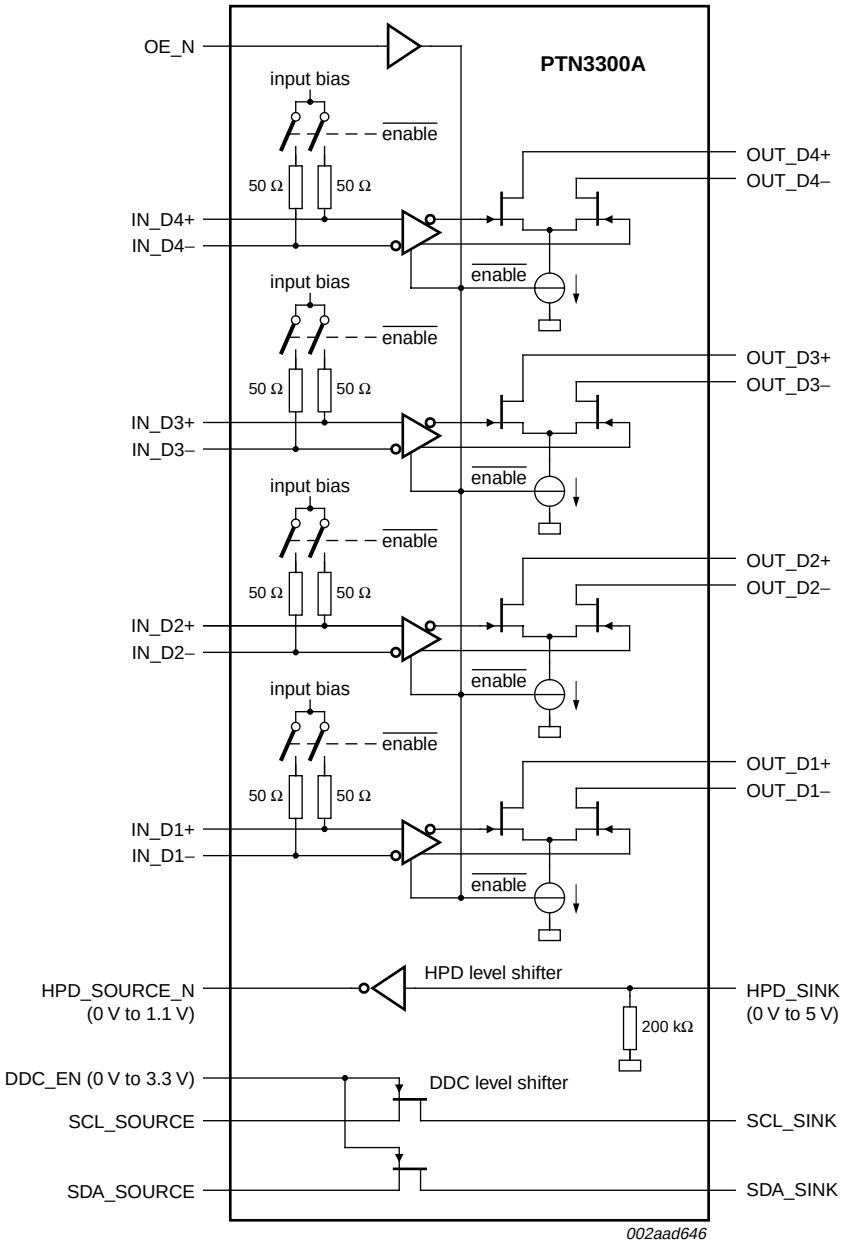
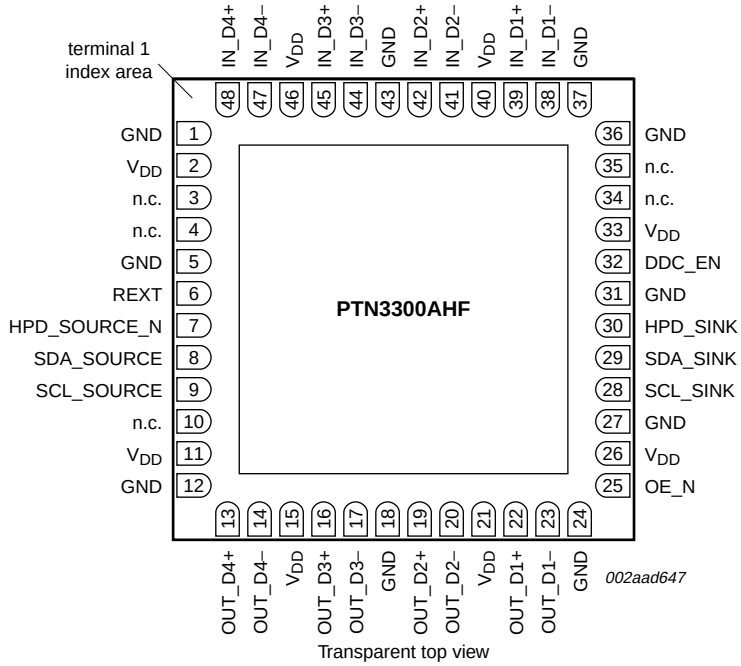



**Fig 2. Functional diagram of PTN3300A**

# 5. Pinning information

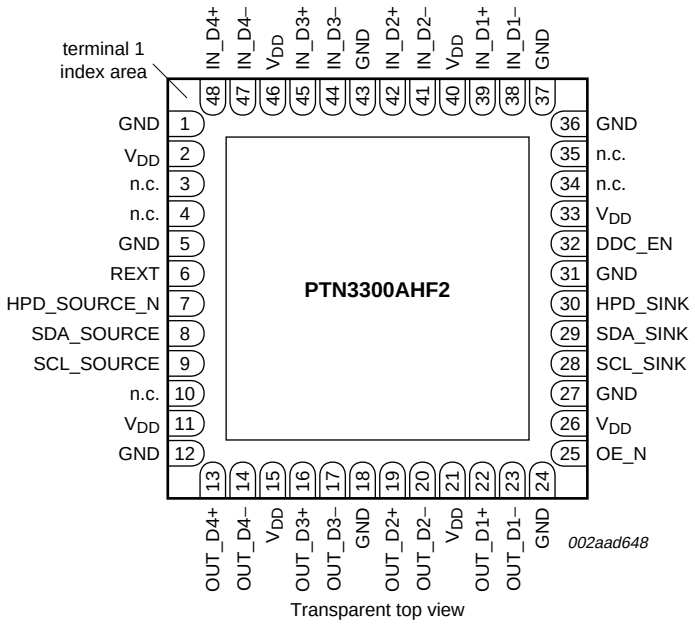
## 5.1 Pinning




Transparent top view

HWQFN48R package supply ground is connected to both GND pins and exposed center pad. GND pins must be connected to supply ground for proper device operation. For enhanced thermal, electrical, and board level performance, the exposed pad needs to be soldered to the board using a corresponding thermal pad on the board and for proper heat conduction through the board, thermal vias need to be incorporated in the PCB in the thermal pad region.

**Fig 3. Pin configuration for HWQFN48R**




Transparent top view

HWQFN48 package supply ground is connected to both GND pins and exposed center pad. GND pins must be connected to supply ground for proper device operation. For enhanced thermal, electrical, and board level performance, the exposed pad needs to be soldered to the board using a corresponding thermal pad on the board and for proper heat conduction through the board, thermal vias need to be incorporated in the PCB in the thermal pad region.

**Fig 4. Pin configuration for HWQFN48**

## 5.2 Pin description

**Table 2. Pin description**

| Symbol | Pin | Type | Description |
|---|---|---|---|
| **OE_N, IN_Dx and OUT_Dx signals** | | | |
| OE_N | 25 | 3.3 V low-voltage CMOS single-ended input | Output Enable and power saving function for high-speed differential level shifter path.<br>When OE_N = HIGH:<br>IN_Dx termination = high-impedance<br>OUT_Dx outputs = high-impedance; zero output current<br>When OE_N = LOW:<br>IN_Dx termination = 50 Ω<br>OUT_Dx outputs = active |
| IN_D4+ | 48 | Self-biasing differential input | Low-swing differential input from display source with PCI Express electrical signalling. IN_D4+ makes a differential pair with IN_D4–. The input to this pin must be AC coupled externally. |
| IN_D4– | 47 | Self-biasing differential input | Low-swing differential input from display source with PCI Express electrical signalling. IN_D4– makes a differential pair with IN_D4+. The input to this pin must be AC coupled externally. |
| IN_D3+ | 45 | Self-biasing differential input | Low-swing differential input from display source with PCI Express electrical signalling. IN_D3+ makes a differential pair with IN_D3–. The input to this pin must be AC coupled externally. |
| IN_D3– | 44 | Self-biasing differential input | Low-swing differential input from display source with PCI Express electrical signalling. IN_D3– makes a differential pair with IN_D3+. The input to this pin must be AC coupled externally. |
| IN_D2+ | 42 | Self-biasing differential input | Low-swing differential input from display source with PCI Express electrical signalling. IN_D2+ makes a differential pair with IN_D2–. The input to this pin must be AC coupled externally. |
| IN_D2– | 41 | Self-biasing differential input | Low-swing differential input from display source with PCI Express electrical signalling. IN_D2– makes a differential pair with IN_D2+. The input to this pin must be AC coupled externally. |
| IN_D1+ | 39 | Self-biasing differential input | Low-swing differential input from display source with PCI Express electrical signalling. IN_D1+ makes a differential pair with IN_D1–. The input to this pin must be AC coupled externally. |
| IN_D1– | 38 | Self-biasing differential input | Low-swing differential input from display source with PCI Express electrical signalling. IN_D1– makes a differential pair with IN_D1+. The input to this pin must be AC coupled externally. |
| OUT_D4+ | 13 | TMDS differential output | DVI and HDMI compliant TMDS output. OUT_D4+ makes a differential pair with OUT_D4–. OUT_D4+ is in phase with IN_D4+. |
| OUT_D4– | 14 | TMDS differential output | DVI and HDMI compliant TMDS output. OUT_D4– makes a differential pair with OUT_D4+. OUT_D4– is in phase with IN_D4–. |
| OUT_D3+ | 16 | TMDS differential output | DVI and HDMI compliant TMDS output. OUT_D3+ makes a differential pair with OUT_D3–. OUT_D3+ is in phase with IN_D3+. |
| OUT_D3– | 17 | TMDS differential output | DVI and HDMI compliant TMDS output. OUT_D3– makes a differential pair with OUT_D3+. OUT_D3– is in phase with IN_D3–. |
| OUT_D2+ | 19 | TMDS differential output | DVI and HDMI compliant TMDS output. OUT_D2+ makes a differential pair with OUT_D2–. OUT_D2+ is in phase with IN_D2+. |
| OUT_D2– | 20 | TMDS differential output | DVI and HDMI compliant TMDS output. OUT_D2– makes a differential pair with OUT_D2+. OUT_D2– is in phase with IN_D2–. |

**Table 2. Pin description** *...continued*

| Symbol | Pin | Type | Description |
|---|---|---|---|
| OUT_D1+ | 22 | TMDS differential output | DVI and HDMI compliant TMDS output. OUT_D1+ makes a differential pair with OUT_D1–. OUT_D1+ is in phase with IN_D1+. |
| OUT_D1– | 23 | TMDS differential output | DVI and HDMI compliant TMDS output. OUT_D1– makes a differential pair with OUT_D1+. OUT_D1– is in phase with IN_D1–. |
| **HPD and DDC signals** | | | |
| HPD_SINK | 30 | 5 V CMOS single-ended input | 0 V to 5 V (nominal) input signal. This signal comes from the DVI or HDMI sink. A HIGH value indicates that the DVI or HDMI sink is connected; a LOW value indicates that the sink is disconnected. HPD_SINK is pulled down by an integrated 200 kΩ pull-down resistor. A LOW input level on this pin will automatically put the PTN3300A in Standby mode for lowest power consumption. |
| HPD_SOURCE_N | 7 | 1.1 V CMOS single-ended output | 0 V to 1.1 V (nominal) output signal. This is the level-shifted **logic-inverted** version of the HPD_SINK signal. |
| SCL_SOURCE | 9 | single-ended 3.3 V DDC I/O pass gate | 3.3 V source-side DDC clock I/O. Pulled up by external termination to 3.3 V. |
| SDA_SOURCE | 8 | single-ended 3.3 V DDC I/O pass gate | 3.3 V source-side DDC data I/O. Pulled up by external termination to 3.3 V. |
| SCL_SINK | 28 | single-ended 5 V DDC I/O pass gate | 5 V sink-side DDC clock I/O. Pulled up by external termination to 5 V. |
| SDA_SINK | 29 | single-ended 5 V DDC I/O pass gate | 5 V sink-side DDC data I/O. Pulled up by external termination to 5 V. |
| DDC_EN | 32 | 3.3 V CMOS input | Enables the DDC level shifter path.<br>When DDC_EN = LOW, DDC level shifter is disabled.<br>When DDC_EN = HIGH, DDC level shifter are enabled.<br>Note that HPD_SINK needs to be HIGH for the DDC channel to be enabled. |
| **Supply and ground** | | | |
| $V_{DD}$ | 2, 11, 15, 21, 26, 33, 40, 46 | 3.3 V DC supply | Supply voltage; 3.3 V ± 10 %. |
| GND[1] | 1, 5, 12, 18, 24, 27, 31, 36, 37, 43 | ground | Supply ground. All ground pins must be connected to ground for proper operation. |
| **Feature control signals** | | | |
| REXT | 6 | analog I/O | Current sense port used to provide an accurate current reference for the differential outputs OUT_Dx. For best output voltage swing accuracy, use of a 10 kΩ resistor (1 % tolerance) from this terminal to GND is recommended. May also be left open-circuit or tied to either $V_{DD}$ or GND. |
| **Miscellaneous** | | | |
| n.c. | 3, 4, 10, 34, 35 | no connection to the die | Not connected. May be left open-circuit or tied to GND or $V_{DD}$ either directly or via a resistor. |

[1] HWQFN48R and HWQFN48 package supply ground is connected to both GND pins and exposed center pad. GND pins must be connected to supply ground for proper device operation. For enhanced thermal, electrical, and board level performance, the exposed pad needs to be soldered to the board using a corresponding thermal pad on the board and for proper heat conduction through the board, thermal vias need to be incorporated in the PCB in the thermal pad region.

# 6. Functional description

Refer to Figure 2 “Functional diagram of PTN3300A”.

The PTN3300A level shifts four lanes of low-swing AC-coupled differential input signals to DVI or HDMI compliant open-drain current-steering differential output signals, up to 2.25 Gbit/s per lane. It has integrated 50 Ω termination resistors for AC-coupled differential input signals. An enable signal OE_N can be used to turn off the TMDS inputs and outputs, thereby minimizing power consumption. The TMDS outputs are back-power safe to disallow current flow from a powered sink while the PTN3300A is unpowered.

The PTN3300A's DDC level-shifter allows 3.3 V source-side termination and 5 V sink-side termination. The PTN3300A offers the back-power safe feature to disallow backdrive current from the DDC clock and data lines when power is off or when DDC is not enabled. An enable signal DCC_EN enables the level shifter block.

The PTN3300A also provides voltage translation for the Hot Plug Detect (HPD) signal from 0 V/5 V on the sink side, inverting and level-shifting to 1.1 V/0 V on the source side. PTN3300A also automatically goes into low power mode when the sink is not connected (HPD_SINK is LOW).

The PTN3300A does not re-time any data. It contains no state machines. No inputs or outputs of the device are latched or clocked. Because the PTN3300A acts as a transparent level shifter, no reset is required.

## 6.1 Flexible and power-efficient enable and disable features

PTN3300A offers different ways to enable or disable functionality, using the Output Enable (OE_N), Hot Plug Detect (HPD_SINK) and DDC Enable (DDC_EN) inputs. Whenever the PTN3300A is disabled using HPD_SINK or OE_N, the device will be in Standby mode and power consumption will be minimal; otherwise the PTN3300A will be in Active mode and power consumption will be nominal. These three inputs each affect the operation of PTN3300A differently: OE_N affects only the TMDS channels, DDC_EN affects only the DDC channel, and HPD_SINK affects both TMDS and DDC channels. The following sections and truth table describe their detailed operation.

### 6.1.1 Hot plug detect with power-saving feature

The HPD channel of PTN3300A in fact has a dual function: as a level-shifting inverting buffer to pass the HPD logic signal from the display sink device (via input HPD_SINK) on to the display source device (via output HPD_SOURCE_N), as well as a detection input for determining when the PTN3300A will go into Standby mode to save power consumption.

The PTN3300A will automatically disable both the TMDS and DDC channels when the HPD input indicates that no display is connected (indicated by HPD_SINK = LOW), upon which power consumption is minimized. The power-down behavior in HPD power-saving mode is identical to the active disablement using both the OE_N input and the DDC_EN input.

The logic state of the HPD_SOURCE_N output always follows the inverse logic state of the HPD_SINK input, regardless of whether the device is in Active or Standby mode.

### 6.1.2 Output Enable function (OE_N)

When input OE_N is asserted (active LOW), the IN_Dx and OUT_Dx signals are fully functional provided that HPD_SINK input is HIGH. Input termination resistors are enabled and the internal bias circuits are turned on.

When OE_N is de-asserted (inactive HIGH), the OUT_Dx outputs are in a high-impedance state and drive zero output current. The IN_Dx input buffers are disabled and IN_Dx termination is disabled. Internal bias circuits for the differential inputs and outputs are turned off. Power consumption is minimized.

**Remark:** Note that OE_N has no influence on the HPD_SINK input, HPD_SOURCE_N output, or the SCL and SDA level shifters. OE_N only affects the high-speed TMDS channel.

### 6.1.3 DDC channel enable function (DDC_EN)

The DDC_EN pin is active HIGH and can be used to isolate a badly behaved slave. When DDC_EN is LOW, the DDC channel is turned off. The DDC_EN input should never change state during an $I^2C$-bus operation. Note that disabling DDC_EN during a bus operation will hang the bus, while enabling DDC_EN during bus traffic would corrupt the $I^2C$-bus operation. Hence, DDC_EN should only be toggled while the bus is idle. (See $I^2C$-bus specification).

### 6.1.4 Enable/disable truth table

**Table 3. HPD_SINK, OE_N and DDC_EN enabling and power saving functions truth table**

| Inputs | | | Channels | | | | Mode |
|---|---|---|---|---|---|---|---|
| HPD_SINK [1] | OE_N [2] | DDC_EN [3] | IN_Dx | OUT_Dx[4] | DDC[5] | HPD_SOURCE_N [6] | |
| LOW | X | X | high-impedance | high-impedance; zero output current | high-impedance | HIGH | Standby |
| HIGH | LOW | LOW | 50 Ω termination to $V_{RX(bias)}$ | enabled | high-impedance | LOW | Active |
| HIGH | LOW | HIGH | 50 Ω termination to $V_{RX(bias)}$ | enabled | enabled | LOW | Active |
| HIGH | HIGH | LOW | high-impedance | high-impedance; zero output current | high-impedance | LOW | Standby |
| HIGH | HIGH | HIGH | high-impedance | high-impedance; zero output current | enabled | LOW | Standby with DDC channel enabled |

[1] A LOW level on input HPD_SINK disables both the TMDS and DDC channels.

[2] A HIGH level on input OE_N disables only the TMDS channels.

[3] A LOW level on input DDC_EN disables only the DDC channel.

[4] OUT_Dx channels ‘enabled’ means outputs OUT_Dx toggling in accordance with IN_Dx differential input voltage switching.

[5] DDC channel ‘enabled’ means SDA_SINK is connected to SDA_SOURCE and SCL_SINK is connected to SCL_SOURCE.

[6] The HPD_SOURCE_N output logic state follows the inverse of the HPD_SINK input logic state regardless of Active or Standby mode.

## 6.2 Analog current reference

The REXT pin (pin 6) is an analog current sense port used to provide an accurate current reference for the differential outputs OUT_Dx. For best output voltage swing accuracy, use of a 10 kΩ resistor (1 % tolerance) connected between this terminal and GND is recommended.

If an external 10 kΩ ± 1 % resistor is not used, this pin can be left open-circuit, or connected to GND or $V_{DD}$, either directly (0 Ω) or using pull-up or pull-down resistors of value less than 10 kΩ. In any of these cases, the output will function normally but at reduced accuracy over voltage and temperature of the following parameters: output levels ($V_{OL}$), differential output voltage swing, and rise and fall time accuracy.

## 6.3 Backdrive current protection

The PTN3300A is designed for backdrive prevention on all sink-side terminals. This supports user scenarios where the display is connected and powered, but the PTN3300A is unpowered. In these cases, the PTN3300A will sink no more than a negligible amount of leakage current, and will block the display (sink) termination network from driving the power supply of the PTN3300A or that of the inactive DVI or HDMI source.

# 7. Limiting values

**Table 4. Limiting values**

*In accordance with the Absolute Maximum Rating System (IEC 60134).*

| Symbol | Parameter | Conditions | | Min | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{DD}$ | supply voltage | | | –0.3 | +4.6 | V |
| $V_I$ | input voltage | 3.3 V CMOS inputs | | –0.3 | $V_{DD}$ + 0.5 | V |
| | | 5.0 V CMOS inputs | | –0.3 | 6.0 | V |
| $T_{stg}$ | storage temperature | | | –65 | +150 | °C |
| $V_{esd}$ | electrostatic discharge voltage | HBM | [1] | - | 3500 | V |
| | | CDM | [2] | - | 1000 | V |

[1] Human Body Model: ANSI/EOS/ESD-S5.1-1994, standard for ESD sensitivity testing, Human Body Model - Component level; Electrostatic Discharge Association, Rome, NY, USA.

[2] Charged Device Model: ANSI/EOS/ESD-S5.3-1-1999, standard for ESD sensitivity testing, Charged Device Model - Component level; Electrostatic Discharge Association, Rome, NY, USA.

# 8. Recommended operating conditions

**Table 5. Recommended operating conditions**

| Symbol | Parameter | Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| $V_{DD}$ | supply voltage | | | 3.0 | 3.3 | 3.6 | V |
| $V_I$ | input voltage | 3.3 V CMOS inputs | | 0 | - | 3.6 | V |
| | | 5.0 V CMOS inputs | | 0 | - | 5.5 | V |
| $V_{I(AV)}$ | average input voltage | DC value at IN_Dn+, IN_Dn– inputs | [1] | - | 0 | - | V |
| $R_{ref(ext)}$ | external reference resistance[2] | connected between REXT pin (pin 6) and GND; ± 1 % | | - | 10 | - | kΩ |
| $T_{amb}$ | ambient temperature | operating in free air | | –40 | - | +85 | °C |

[1] Input signals to these pins must be AC-coupled.

[2] Operation without external reference resistor is possible but will result in reduced output voltage swing accuracy. For details, see Section 6.2.

## 8.1 Current consumption

**Table 6. Current consumption**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $I_{DD}$ | supply current | OE_N = 0 **and** HPD_SINK = 1; Active mode | 10 | 35 | 50 | mA |
| | | OE_N = 1 **or** HPD_SINK = 0; Standby mode | - | 5 | 50 | µA |

# 9. Characteristics

## 9.1 Differential inputs

**Table 7. Differential input characteristics for IN_Dx signals**

| Symbol | Parameter | Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| UI | unit interval[1] | | [2] | 400 | - | 4000 | ps |
| $V_{RX\_DIFFp\text{-}p}$ | differential input peak-to-peak voltage | | [3] | 0.175 | - | 1.200 | V |
| $T_{RX\_EYE}$ | receiver eye time | minimum eye width at IN_Dx input pair | | 0.8 | - | - | UI |
| $V_{i(cm)M(AC)}$ | peak common-mode input voltage (AC) | includes all frequencies above 30 kHz | [4] | - | - | 100 | mV |
| $Z_{RX\_DC}$ | DC input impedance | | | 40 | 50 | 60 | Ω |
| $V_{RX(bias)}$ | bias receiver voltage | voltage at IN_Dx when IN_Dx = open circuit | [5] | 1.0 | 1.2 | 1.4 | V |
| $Z_{I(se)}$ | single-ended input impedance | inputs in high-impedance state | [6] | 100 | - | - | kΩ |

[1] UI (unit interval) = $t_{bit}$ (bit time).

[2] UI is determined by the display mode. Nominal bit rate ranges from 250 Mbit/s to 2.25 Gbit/s per lane. Nominal UI at 2.25 Gbit/s = 444 ps. 400 ps = 444 ps – 10 %.

[3] $V_{RX\_DIFFp\text{-}p} = 2 \times |V_{RX\_D+} - V_{RX\_D-}|$. Applies to IN_Dx signals.

[4] $V_{i(cm)M(AC)} = |V_{RX\_D+} + V_{RX\_D-}| / 2 - V_{RX(cm)}$.
$V_{RX(cm)}$ = DC (avg) of $|V_{RX\_D+} + V_{RX\_D-}| / 2$.

[5] Intended to limit power-up stress on source side PCIe output buffers.

[6] Differential inputs will switch to a high-impedance state when OE_N is LOW.

## 9.2 Differential outputs

The level shifter's differential outputs are designed to meet DVI version 1.0 and HDMI v1.3a specifications.

**Table 8. Differential output characteristics for OUT_Dx signals**

| Symbol | Parameter | Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| $V_{OH(se)}$ | single-ended HIGH-level output voltage | | [1] | $V_{TT}$ – 0.01 | $V_{TT}$ | $V_{TT}$ + 0.01 | V |
| $V_{OL(se)}$ | single-ended LOW-level output voltage | | [2] | $V_{TT}$ – 0.60 | $V_{TT}$ – 0.50 | $V_{TT}$ – 0.40 | V |
| $\Delta V_{O(se)}$ | single-ended output voltage variation | logic 1 and logic 0 state applied respectively to differential inputs IN_Dn; $R_{ref(ext)}$ connected. See Table 5 | [3] | 450 | 500 | 600 | mV |
| $I_{OZ}$ | off-state output current | single-ended | | - | - | 10 | µA |
| $t_r$ | rise time | 20 % to 80 % | [4] | 75 | - | 180 | ps |
| $t_f$ | fall time | 80 % to 20 % | [4] | 75 | - | 180 | ps |
| $t_{sk}$ | skew time | intra-pair | [5] | - | - | 10 | ps |
| | | inter-pair | [6] | - | - | 250 | ps |
| $t_{jit}$ | jitter time | jitter contribution | [7] | - | - | 7.4 | ps |

[1] $V_{TT}$ is the DC termination voltage in the DVI or HDMI sink. $V_{TT}$ is nominally 3.3 V. Termination resistance is nominally 50 Ω.

[2] The open-drain output pulls down from $V_{TT}$.

[3] Swing down from TMDS termination voltage (3.3 V ± 10 %).

[4] Maximum rise/fall time at 2.25 Gbit/s = 444 ps. 400 ps = 444 ps – 15 %.

[5] This differential skew budget is in addition to the skew presented between IN_D+ and IN_D– paired input pins.

[6] This lane-to-lane skew budget is in addition to skew between differential input pairs.

[7] Jitter budget for differential signals as they pass through the level shifter. 7.4 ps = 0.02 UI at 1.65 Gbit/s.

## 9.3 HPD_SINK input, HPD_SOURCE_N output

**Table 9. HPD characteristics**

| Symbol | Parameter | Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| $V_{IH}$ | HIGH-level input voltage | HPD_SINK | [1] | 2.0 | 5.0 | 5.3 | V |
| $V_{IL}$ | LOW-level input voltage | HPD_SINK | | 0 | - | 0.8 | V |
| $I_{LI}$ | input leakage current | HPD_SINK | [2] | - | - | 10 | µA |
| $V_{OH}$ | HIGH-level output voltage | HPD_SOURCE_N; $I_{OH}$ = 100 µA; HPD_SINK = LOW | | 0.7 | - | 1.1 | V |
| $V_{OL}$ | LOW-level output voltage | HPD_SOURCE_N; $I_{OL}$ = 100 µA; HPD_SINK = HIGH | | 0 | - | 0.2 | V |
| $t_{PD}$ | propagation delay | from HPD_SINK to HPD_SOURCE_N; 50 % to 50 %; $C_L$ = 10 pF | [3] | - | - | 200 | ns |
| $t_t$ | transition time | HPD_SOURCE_N rise/fall; 10 % to 90 %; $C_L$ = 10 pF | [4] | 1 | - | 20 | ns |
| $R_{pd}$ | pull-down resistance | HPD_SINK input pull-down resistor | [5] | 100 | 200 | 300 | kΩ |

[1] Low-speed input changes state on cable plug/unplug.

[2] Measured with HPD_SINK at $V_{IH}$ maximum and $V_{IL}$ minimum.

[3] Time from HPD_SINK changing state to HPD_SOURCE_N changing state. Includes HPD_SOURCE_N rise/fall time.

[4] Time required to transition from $V_{OH}$ to $V_{OL}$ or from $V_{OL}$ to $V_{OH}$.

[5] Guarantees HPD_SINK is LOW when no display is plugged in.

## 9.4 OE_N and DDC_EN inputs

**Table 10. OE_N and DDC_EN input characteristics**

| Symbol | Parameter | Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| $V_{IH}$ | HIGH-level input voltage | | | 2.0 | - | - | V |
| $V_{IL}$ | LOW-level input voltage | | | - | - | 0.8 | V |
| $I_{LI}$ | input leakage current | OE_N pin | [1] | - | - | 10 | µA |

[1] Measured with input at $V_{IH}$ maximum and $V_{IL}$ minimum.

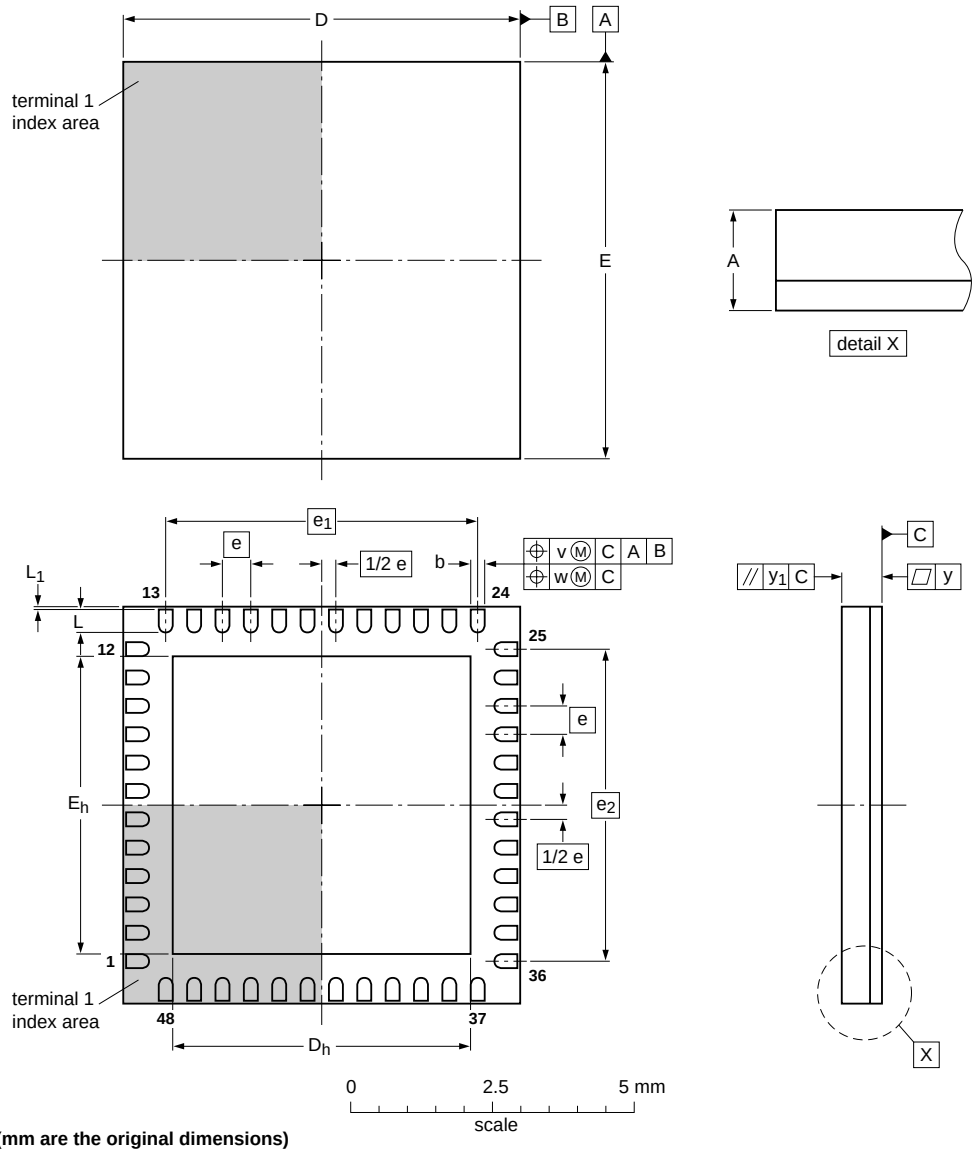
## 9.5 DDC characteristics

**Table 11. DDC characteristics**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $f_{clk}$ | clock frequency | SCL_SOURCE, SDA_SOURCE, SCL_SINK, SDA_SINK | - | - | 400 | kHz |
| **ON state (DDC_EN = HIGH and HPD_SINK = HIGH)** | | | | | | |
| $R_{ON}$ | ON resistance | pass gate in ON state; $I_O$ = 15 mA; $V_O$ = 0.4 V | - | 7 | 30 | Ω |
| $V_{O(sw)}$ | switch output voltage | SOURCE side; $V_I$ = 3.3 V; $I_O$ = –100 µA | 1.8 | 2.1 | 2.4 | V |
| | | SINK side; $V_I$ = 5.0 V; $I_O$ = –100 µA | 1.8 | 2.1 | 2.4 | V |
| $C_{io}$ | input/output capacitance | $V_I$ = 3.3 V; $I_O$ = –100 µA | - | 5 | 10 | pF |
| **OFF state (DDC_EN = LOW)** | | | | | | |
| $I_{LI}$ | input leakage current | SOURCE side; 0 V < $V_I$ < 3.3 V | –1 | - | +1 | µA |
| | | SINK side; 0 V < $V_I$ < 5.0 V | –1 | - | +1 | µA |
| $C_{io}$ | input/output capacitance | $V_I$ = 3.3 V; $I_O$ = –100 µA | - | 1 | 5 | pF |

# 10. Package outline

**HWQFN48R: plastic thermal enhanced very very thin quad flat package; no leads 48 terminals; resin based; body 7 x 7 x 0.7 mm** **SOT1031-2**



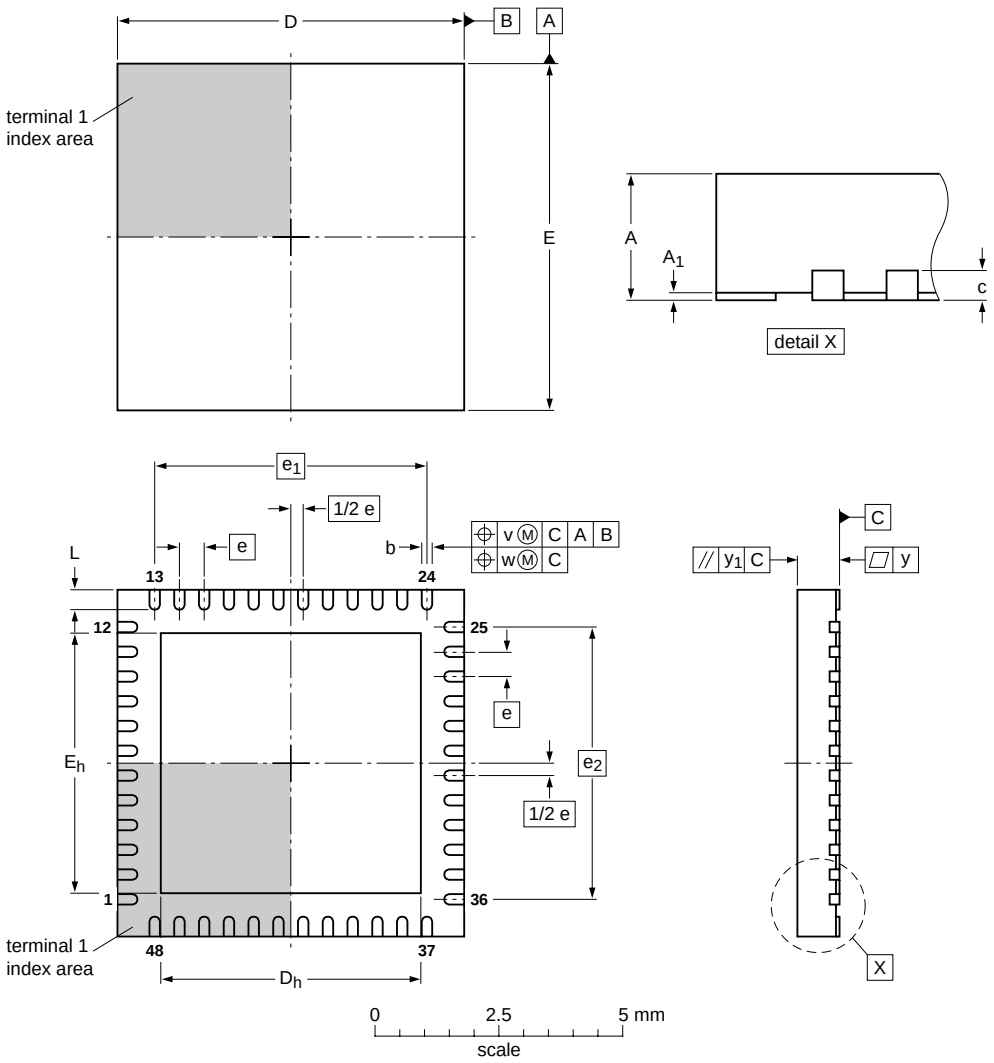

**DIMENSIONS (mm are the original dimensions)**

| UNIT | | A | b | D | $D_h$ | E | $E_h$ | e | $e_1$ | $e_2$ | L | $L_1$ | v | w | y | $y_1$ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | max | 0.80 | 0.27 | 7.1 | 5.35 | 7.1 | 5.35 | | | | 0.42 | 0.10 | | | | |
| | nom | 0.70 | 0.25 | 7.0 | 5.25 | 7.0 | 5.25 | 0.5 | 5.5 | 5.5 | 0.40 | 0.05 | 0.1 | 0.05 | 0.05 | 0.1 |
| | min | 0.65 | 0.23 | 6.9 | 5.15 | 6.9 | 5.15 | | | | 0.38 | 0.00 | | | | |

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | JEITA | | | |
| SOT1031-2 | - - - | - - - | - - - | | | ~~08-03-06~~ 08-03-26 |

**Fig 5. Package outline SOT1031-2 (HWQFN48R)**

**HWQFN48: plastic thermal enhanced very very thin quad flat package; no leads; 48 terminals; body 7 x 7 x 0.65 mm** **SOT1074-1**




**DIMENSIONS (mm are the original dimensions)**

| UNIT | | A(1) | $A_1$ | b | c | D(1) | $D_h$ | E(1) | $E_h$ | e | $e_1$ | $e_2$ | L | v | w | y | $y_1$ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | max | 0.80 | 0.05 | 0.30 | | 7.1 | 5.40 | 7.1 | 5.40 | | | | 0.5 | | | | |
| | nom | 0.65 | 0.02 | 0.21 | 0.2 | 7.0 | 5.25 | 7.0 | 5.25 | 0.5 | 5.5 | 5.5 | 0.4 | 0.1 | 0.05 | 0.05 | 0.1 |
| | min | 0.60 | 0.00 | 0.18 | | 6.9 | 5.10 | 6.9 | 5.10 | | | | 0.3 | | | | |

**Note**

1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | JEITA | | | |
| SOT1074-1 | - - - | - - - | - - - | | | ~~08-03-06~~ 08-03-14 |

**Fig 6. Package outline SOT1074-1 (HWQFN48)**

# 11. Soldering of SMD packages

This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note *AN10365 "Surface mount reflow soldering description"*.

## 11.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

## 11.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

- Through-hole components
- Leaded or leadless SMDs, which are glued to the surface of the printed circuit board

Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leaded SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leaded packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

- Board specifications, including the board finish, solder masks and vias
- Package footprints, including solder thieves and orientation
- The moisture sensitivity level of the packages
- Package placement
- Inspection and repair
- Lead-free soldering versus SnPb soldering

## 11.3 Wave soldering

Key characteristics in wave soldering are:

- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- Solder bath specifications, including temperature and impurities

## 11.4 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see Figure 7) than a SnPb process, thus reducing the process window
- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with Table 12 and 13

**Table 12. SnPb eutectic process (from J-STD-020C)**

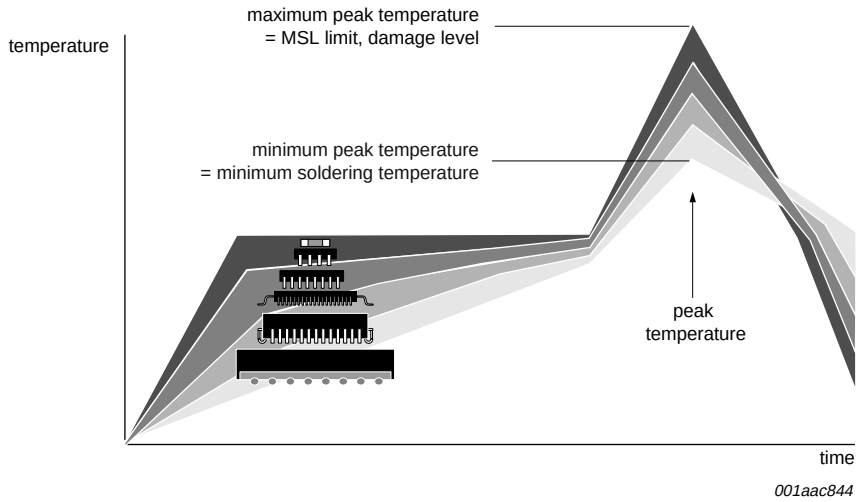
| Package thickness (mm) | Package reflow temperature (°C) | |
|---|---|---|
| | Volume ($mm^3$) | |
| | < 350 | ≥ 350 |
| < 2.5 | 235 | 220 |
| ≥ 2.5 | 220 | 220 |

**Table 13. Lead-free process (from J-STD-020C)**

| Package thickness (mm) | Package reflow temperature (°C) | | |
|---|---|---|---|
| | Volume ($mm^3$) | | |
| | < 350 | 350 to 2000 | > 2000 |
| < 1.6 | 260 | 260 | 260 |
| 1.6 to 2.5 | 260 | 250 | 245 |
| > 2.5 | 250 | 245 | 245 |

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see Figure 7.




MSL: Moisture Sensitivity Level

**Fig 7. Temperature profiles for large and small components**

For further information on temperature profiles, refer to Application Note *AN10365 "Surface mount reflow soldering description"*.

## 12. Abbreviations

**Table 14. Abbreviations**

| Acronym | Description |
|---|---|
| CDM | Charged-Device Model |
| CEC | Consumer Electronics Control |
| DDC | Data Display Channel |
| DVI | Digital Visual Interface |
| EMI | ElectroMagnetic Interference |
| ESD | ElectroStatic Discharge |
| HBM | Human Body Model |
| HDMI | High-Definition Multimedia Interface |
| HPD | Hot Plug Detect |
| $I^2C$-bus | Inter-Integrated Circuit bus |
| I/O | Input/Output |
| NMOS | Negative-channel Metal-Oxide Semiconductor |
| TMDS | Transition Minimized Differential Signaling |
| VESA | Video Electronics Standards Association |

## 13. Revision history

**Table 15. Revision history**

| Document ID | Release date | Data sheet status | Change notice | Supersedes |
|---|---|---|---|---|
| PTN3300A_1 | 20080630 | Product data sheet | - | - |

# 14. Legal information

## 14.1 Data sheet status

| Document status[1][2] | Product status[3] | Definition |
|---|---|---|
| Objective [short] data sheet | Development | This document contains data from the objective specification for product development. |
| Preliminary [short] data sheet | Qualification | This document contains data from the preliminary specification. |
| Product [short] data sheet | Production | This document contains the product specification. |

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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