Dual P-channel MOSFET

ELM54801AA-N

■General description

ELM54801AA-N uses advanced trench technology to provide excellent Rds(on) and low gate charge.

■Features

- Vds=-30V
- Id=-5A (Vgs=-10V)
- Rds(on) < 48mΩ (Vgs=-10V)
- Rds(on) < 57mΩ (Vgs=-4.5V)
- Rds(on) < 80mΩ (Vgs=-2.5V)

■Maximum absolute ratings

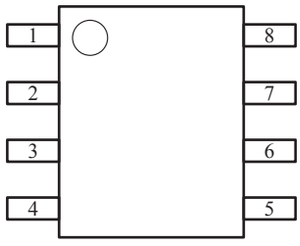
Parameter		Symbol	Limit	Unit	Note
Drain-source voltage		Vds	-30	V	
Gate-source voltage		Vgs	±12	V	
Continuous drain current	Ta=25°C	Id	-5	A	
	Ta=70°C		-4		
Pulsed drain current		Idm	-28	A	3
Avalanche current		Ias, Iar	17	A	3
Avalanche energy	L=0.1mH	Eas, Ear	14	mJ	3
Power dissipation	Ta=25°C	Pd	2.0	W	2
	Ta=70°C		1.3		
Junction and storage temperature range		Tj, Tstg	-55 to 150	°C	

■Thermal characteristics

Parameter		Symbol	Typ.	Max.	Unit	Note
Maximum junction-to-ambient	t≤10s	Rθja	48.0	62.5	°C/W	1
Maximum junction-to-ambient	Steady-state		74.0	90.0	°C/W	1, 4
Maximum junction-to-lead	Steady-state	Rθjl	32.0	40.0	°C/W	

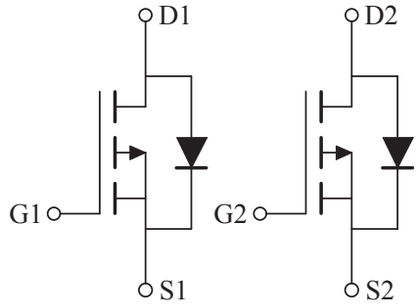
■Pin configuration

SOP-8(TOP VIEW)



Pin No.	Pin name
1	SOURCE2
2	GATE2
3	SOURCE1
4	GATE1
5	DRAIN1
6	DRAIN1
7	DRAIN2
8	DRAIN2

■Circuit



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■Electrical characteristics

Ta=25°C

Parameter	Symbol	Condition		Min.	Typ.	Max.	Unit
STATIC PARAMETERS							
Drain-source breakdown voltage	BVdss	Id=-250μA, Vgs=0V		-30			V
Zero gate voltage drain current	Idss	Vds=-30V, Vgs=0V				-1	μA
			Tj=55°C			-5	
Gate-body leakage current	Igss	Vds=0V, Vgs=±12V				±100	nA
Gate threshold voltage	Vgs(th)	Vds=Vgs, Id=-250μA		-0.5	-0.9	-1.3	V
On state drain current	Id(on)	Vgs=-4.5V, Vds=-5V		-28			A
Static drain-source on-resistance	Rds(on)	Vgs=-10V, Id=-5A			40	48	mΩ
			Tj=125°C		60	72	
		Vgs=-4.5V, Id=-3.5A			45	57	
		Vgs=-2.5V, Id=-2.5A			60	80	
Forward transconductance	Gfs	Vds=-5V, Id=-5A			18		S
Diode forward voltage	Vsd	Is=-1A, Vgs=0V			-0.7	-1.0	V
Max. body-diode continuous current	Is					-2.5	A
DYNAMIC PARAMETERS							
Input capacitance	Ciss	Vgs=0V, Vds=-15V, f=1MHz		515	645	780	pF
Output capacitance	Coss			55	80	105	pF
Reverse transfer capacitance	Crss			30	55	80	pF
Gate resistance	Rg	Vgs=0V, Vds=0V, f=1MHz		4.0	7.8	12.0	Ω
SWITCHING PARAMETERS							
Total gate charge	Qg	Vgs=-4.5V, Vds=-15V Id=-5A		5.0	7.0	9.0	nC
Gate-source charge	Qgs				1.5		nC
Gate-drain charge	Qgd				2.5		nC
Turn-on delay time	td(on)	Vgs=-10V, Vds=-15V Rl=3Ω, Rgen=6Ω			6.5		ns
Turn-on rise time	tr				3.5		ns
Turn-off delay time	td(off)				41.0		ns
Turn-off fall time	tf				9.0		ns
Body diode reverse recovery time	trr	If=-5A, dl/dt=100A/μs			11	15	ns
Body diode reverse recovery charge	Qrr	If=-5A, dl/dt=100A/μs			3.5	5.0	nC

NOTE :

1. The value of Rθja is measured with the device mounted on 1in2 FR-4 board of 2oz. Copper, in still air environment with Ta =25°C. The value in any given application depends on the user's specific board design.
2. The power dissipation Pd is based on Tj(Max)=150°C, using 10s junction-to-ambient thermal resistance.
3. Repetitive rating, pulse width limited by junction temperature Tj(Max)=150°C. Ratings are based on low frequency and duty cycles to keep initial Tj=25°C.
4. The Rθja is the sum of the thermal impedence from junction to lead Rθjl and lead to ambient.
5. The static characteristics in Figures 1 to 6 are obtained using <300μs pulses, duty cycle 0.5% max.
6. These curves are based on the junction-to-ambient thermal impedence which is measured with the device mounted on 1in2 FR-4 board with 2oz.Copper, assuming a maximum junction temperature of Tj(Max)=150°C. The SOA curve provides a single pulse rating.

■Typical electrical and thermal characteristics

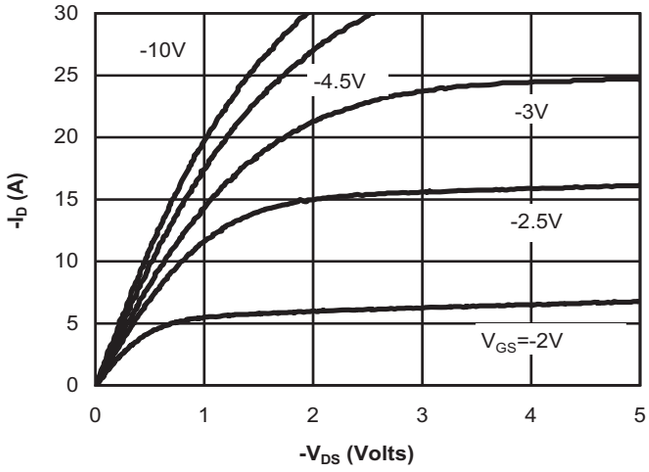


Fig 1: On-Region Characteristics (Note E)

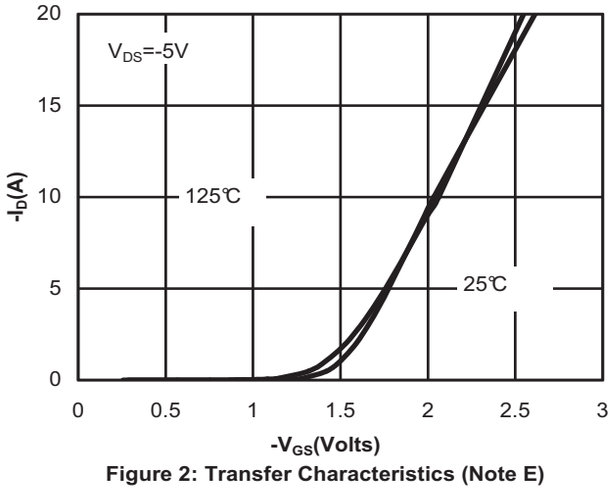


Figure 2: Transfer Characteristics (Note E)

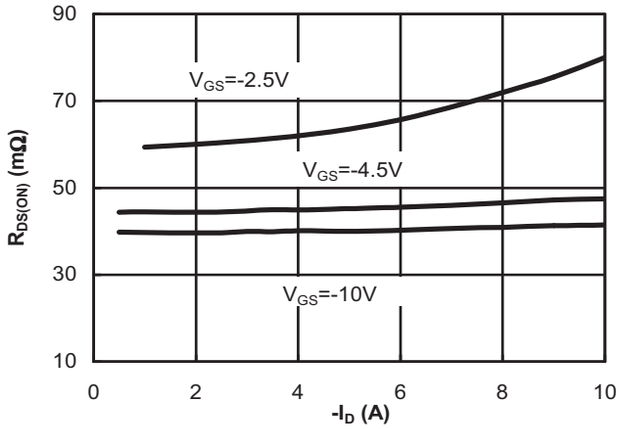


Figure 3: On-Resistance vs. Drain Current and Gate Voltage (Note E)

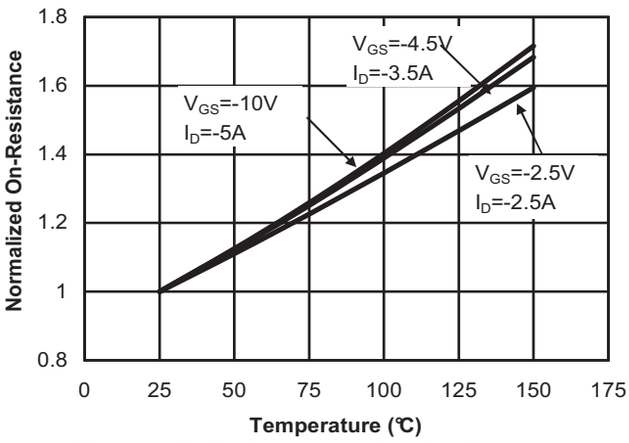


Figure 4: On-Resistance vs. Junction Temperature (Note E)

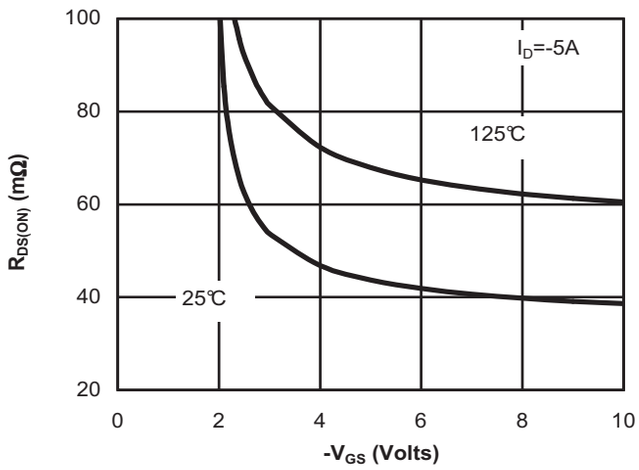


Figure 5: On-Resistance vs. Gate-Source Voltage (Note E)

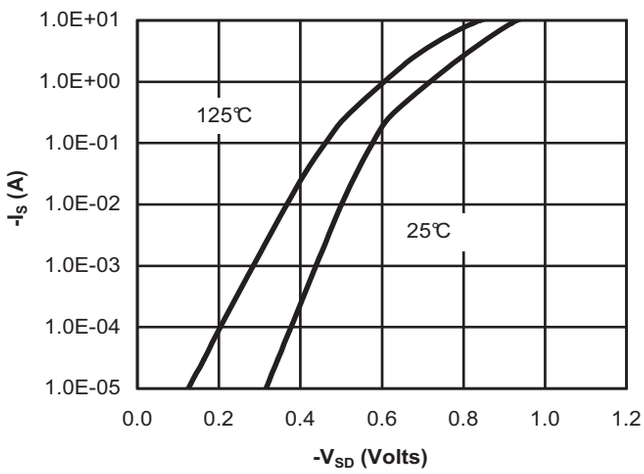


Figure 6: Body-Diode Characteristics (Note E)

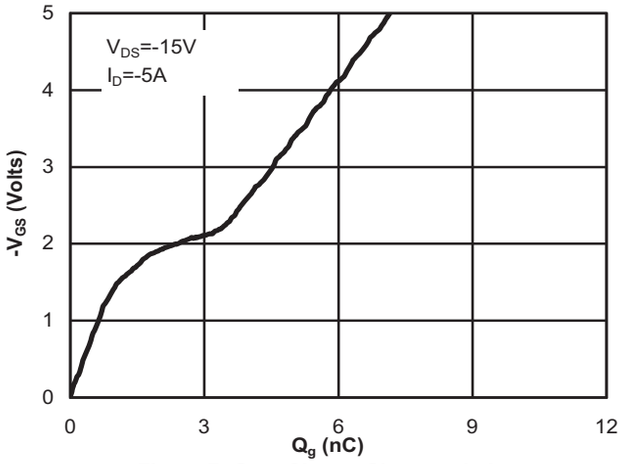


Figure 7: Gate-Charge Characteristics

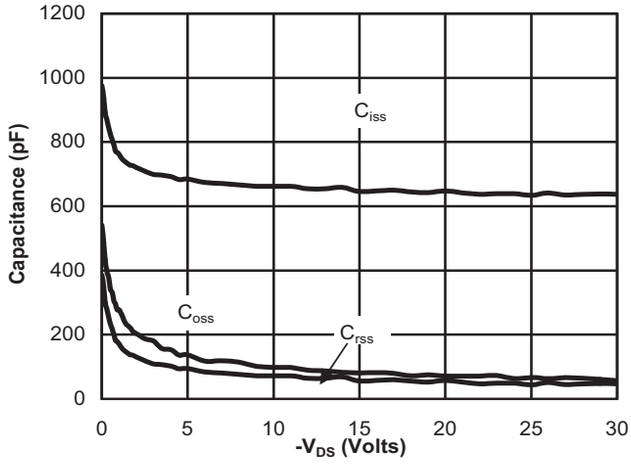


Figure 8: Capacitance Characteristics

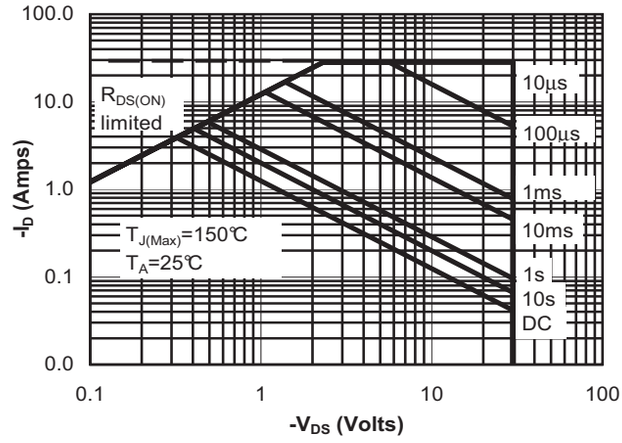


Figure 9: Maximum Forward Biased Safe Operating Area (Note F)

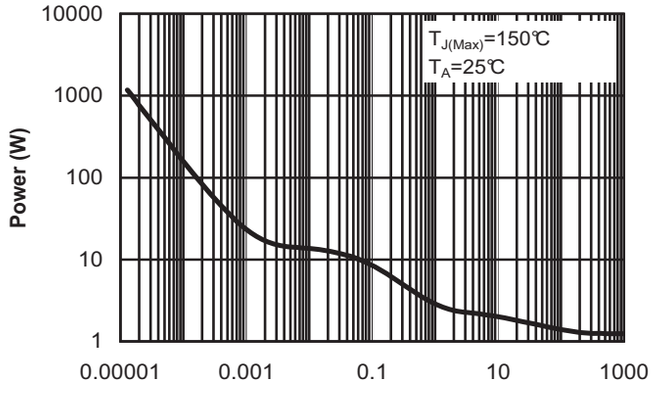


Figure 10: Single Pulse Power Rating Junction-to-Ambient (Note F)

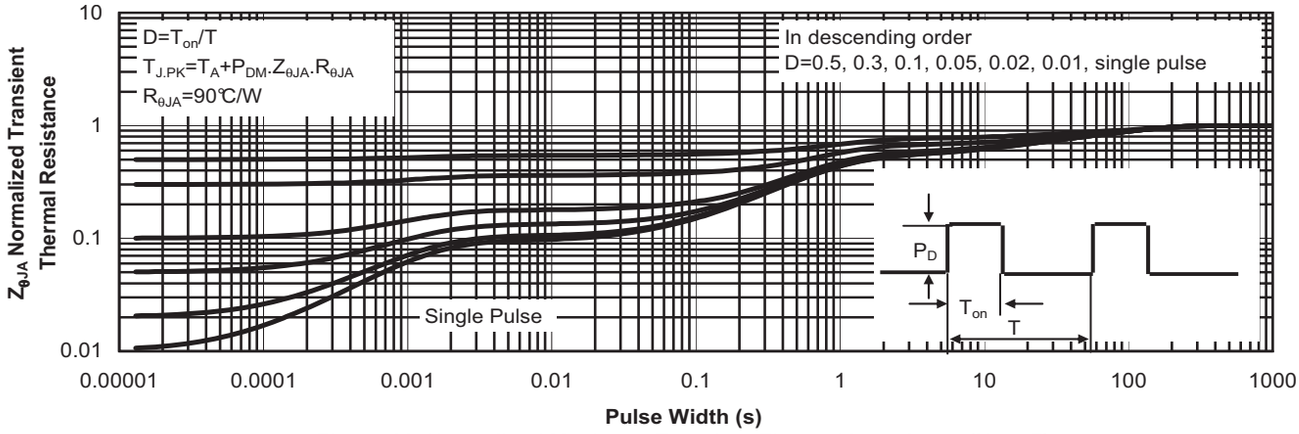
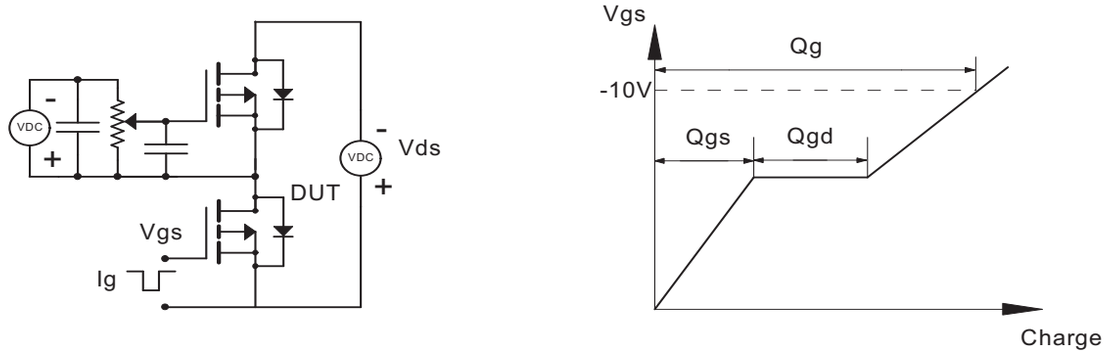


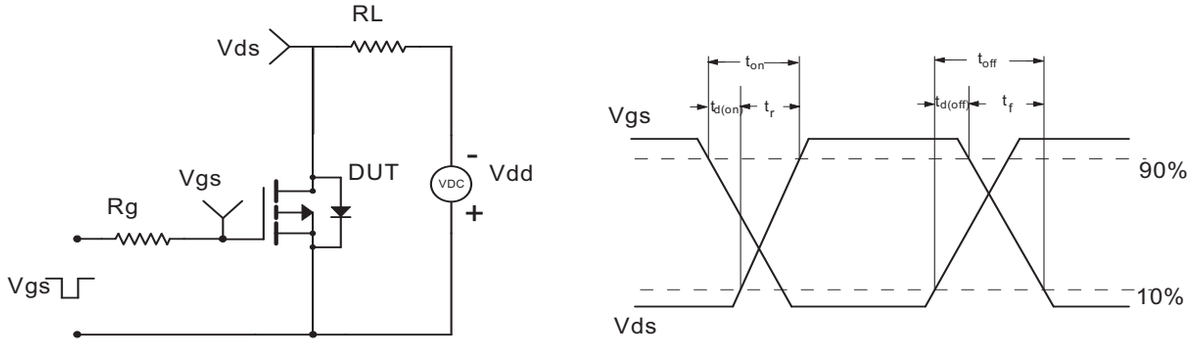
Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)

■Test circuit & waveform

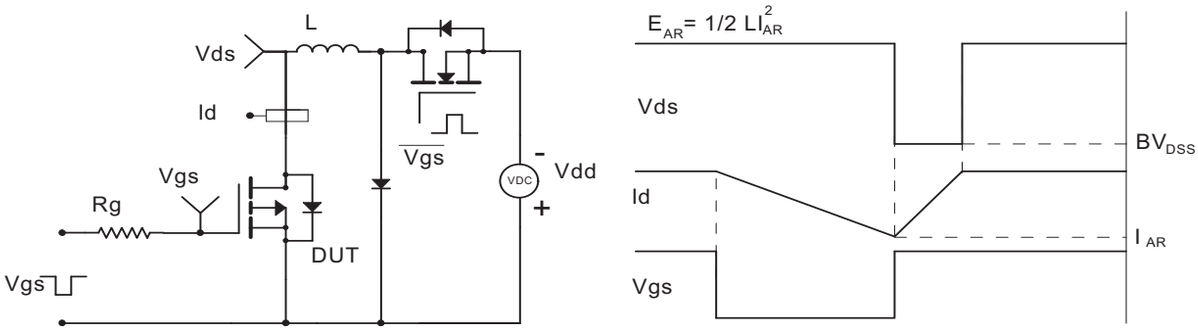
Gate Charge Test Circuit & Waveform



Resistive Switching Test Circuit & Waveforms



Unclamped Inductive Switching (UIS) Test Circuit & Waveforms



Diode Recovery Test Circuit & Waveforms