MYSON TECHNOLOGY

MTD516 (Preliminary)

16 Port 10M/100M Ethernet Switch

FEATURES

- IEEE802.3 and IEEE802.3u compliant.
- Provide 16 RMII (Reduced Media Independent Interface) ports.
- Programmable 1K/8K MAC addresses filtering database.
- Store and forward switching function and bad packet filtering function.
- Optional back_pressure/802.3x flow control/ flooding control/broadcast control.
- Optional EEPROM Interface for advanced switch configurations.
- 4MB/2MB packet buffer with SGRAM/SDRAM flexible memory interface.
- Port VLAN/trunking.
- Link/Rx activity, packet buffer utilization LED display.
- 83MHz for non-blocking 16 port switch.
- Build in internal/external memory test function.
- 208 pin PQFP package, 3.3V operation voltage.

GENERAL DESCRIPTION

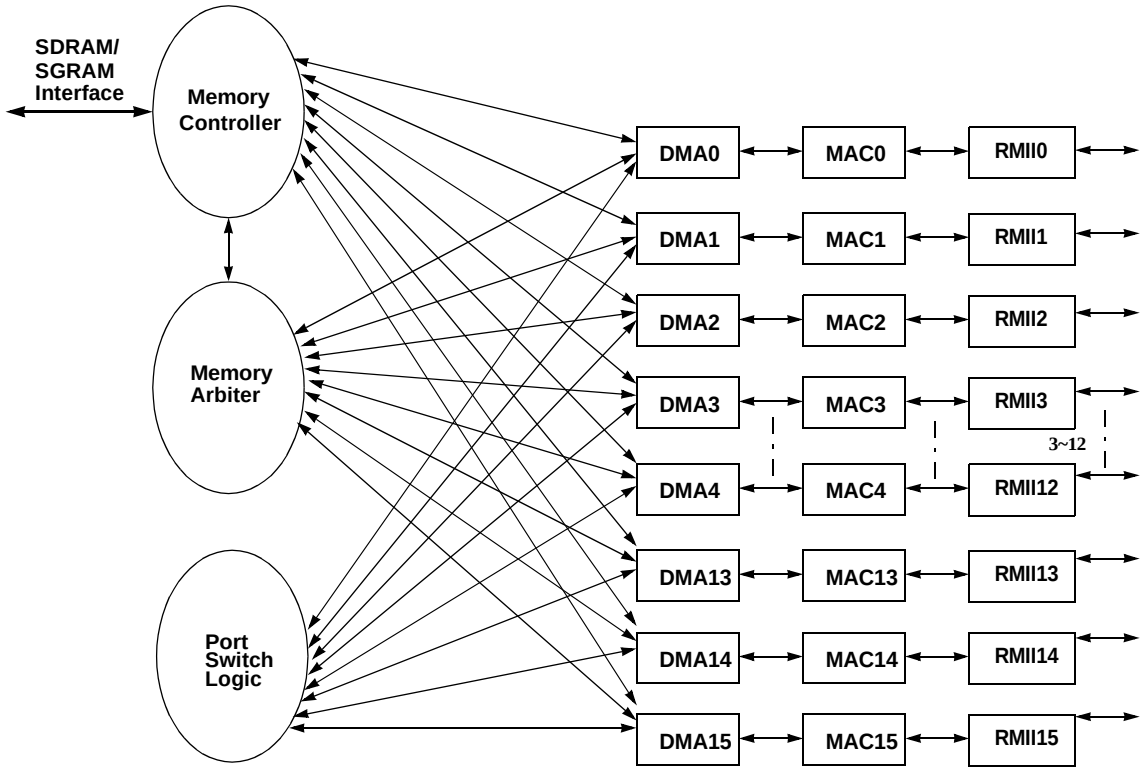
The MTD516 complies fully with the IEEE802.3, 802.3u and 802.3x specifications and is a non-blocking 16 port 10M/100M Ethernet switch device.

Support 16 RMII ports for 10M/100M operation. 4MB memory interface provides maximum 2730 packet buffers for Ethernet packet buffering. Up to 8192 address entrys are provided by the MTD516, and the MTD516 use full Ethernet address compare algorithm to minimize hashing collision events.

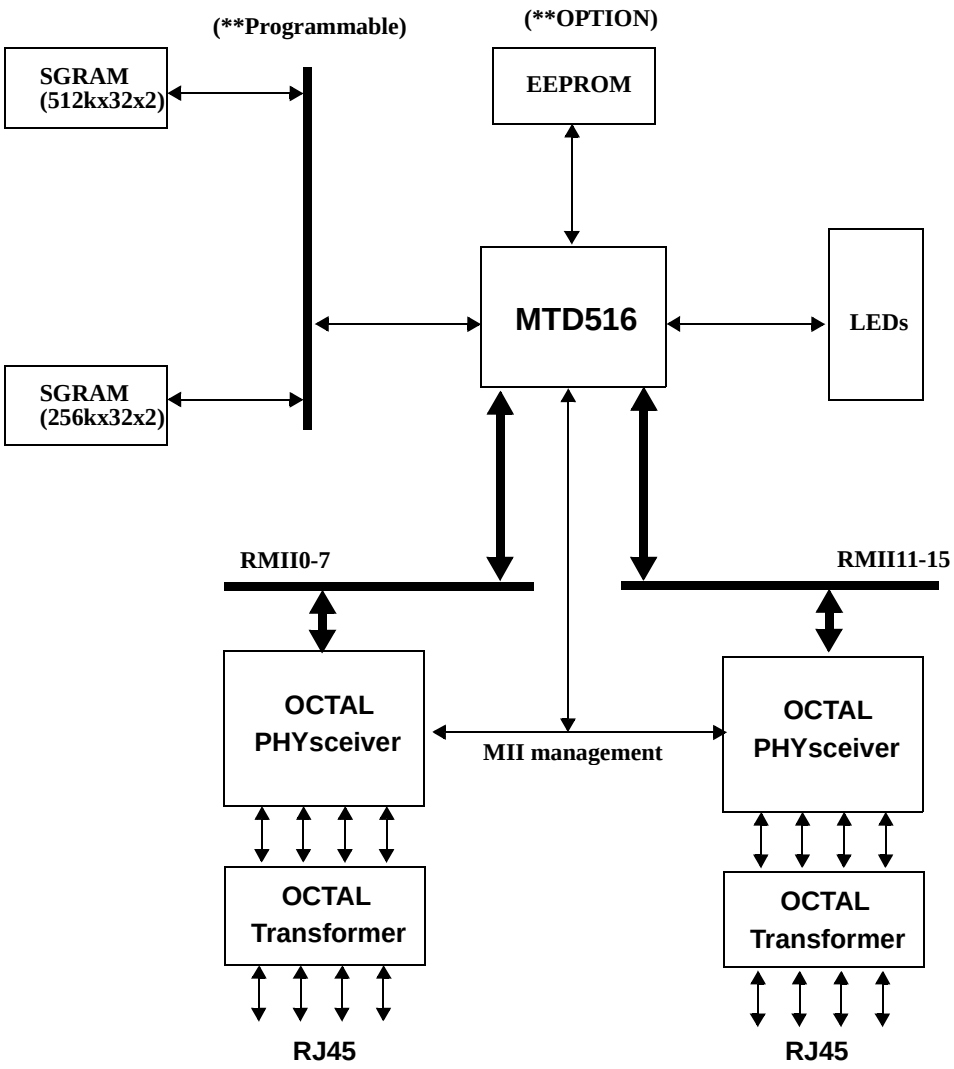
The MTD516 provides EEPROM interface to config port trunking, port VLAN, static entry, 802.3x flow control threshold, flooding port, broadcast control threshold. Each MTD516 ports support 10M/100M auto-negotiation by MII management interface.

The MTD516 also provides 2 pins for Link/ RX activity, packet buffer utilization LED display function.

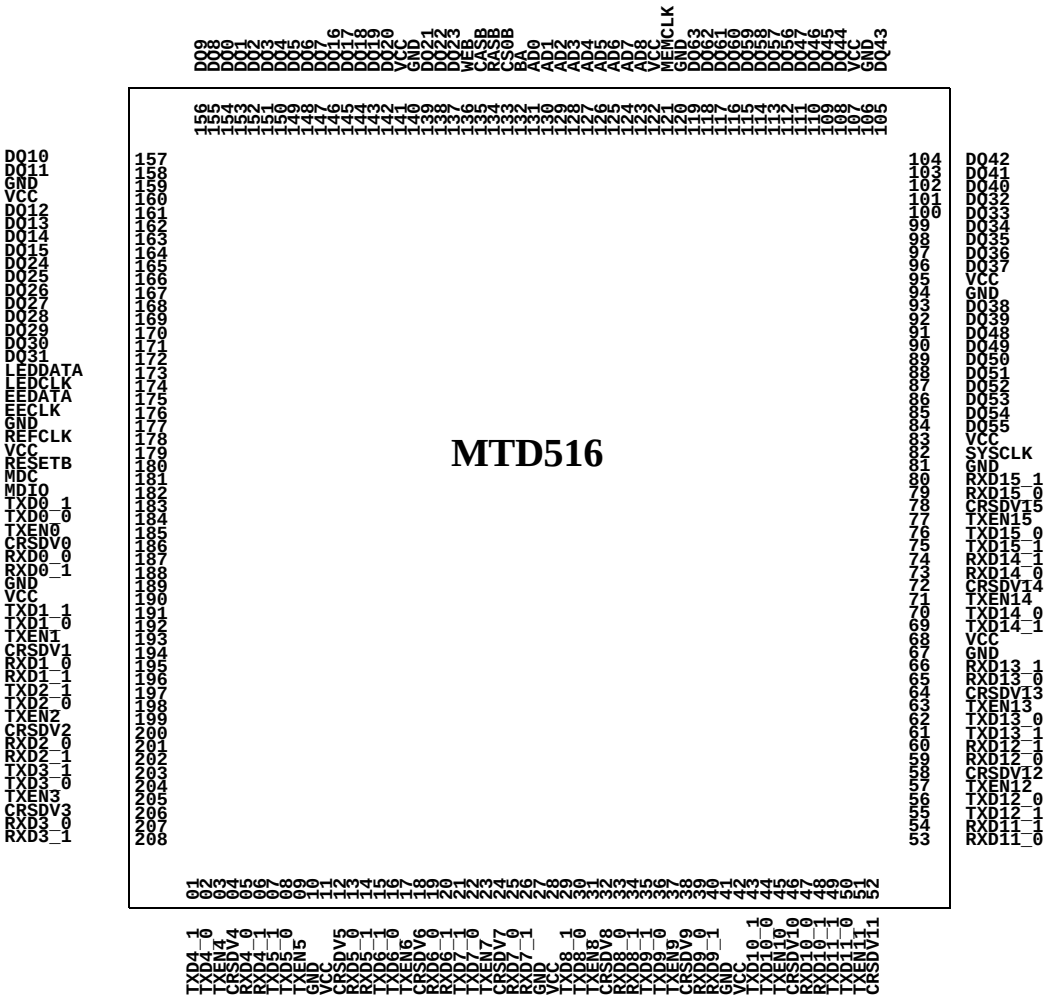
BLOCK DIAGRAM



SYSTEM DIAGRAM



1.0 PIN CONNECTION



2.0 PIN DESCRIPTIONS

RMII Port Interface Pins			
Name	**Pin Number**	**I/O**	**Descriptions**
CRSDV0	186	I	Port0 RMII receive interface signal, CRSDV0 is asserted high when port0 media is non_idle.
RXD0_0	187	I	Port0 RMII receive data bit_0.
RXD0_1	188	I	Port0 RMII receive data bit_1.
TXEN0	185	O	Port0 RMII transmit enable signal.
TXD0_0	184	O	Port0 RMII transmit data bit_0.
TXD0_1	183	O	Port0 RMII transmit data bit_1.
CRSDV1	194	I	Port1 RMII receive interface signal, CRSDV1 is asserted high when port1 media is non_idle.
RXD1_0	195	I	Port1 RMII receive data bit_0.
RXD1_1	196	I	Port1 RMII receive data bit_1.
TXEN1	193	O	Port1 RMII transmit enable signal.
TXD1_0	192	O	Port1 RMII transmit data bit_0.
TXD1_1	191	O	Port1 RMII transmit data bit_1.
CRSDV2	200	I	Port2 RMII receive interface signal, CRSDV2 is asserted high when port2 media is non_idle.
RXD2_0	201	I	Port2 RMII receive data bit_0.
RXD2_1	202	I	Port2 RMII receive data bit_1.
TXEN2	199	O	Port2 RMII transmit enable signal.
TXD2_0	198	O	Port2 RMII transmit data bit_0.
TXD2_1	197	O	Port2 RMII transmit data bit_1.
CRSDV3	206	I	Port3 RMII receive interface signal, CRSDV0 is asserted high when port3 media is non_idle.
RXD3_0	207	I	Port3 RMII receive data bit_0.
RXD3_1	208	I	Port3 RMII receive data bit_1.
TXEN3	205	O	Port3 RMII transmit enable signal.
TXD3_0	204	O	Port3 RMII transmit data bit_0.
TXD3_1	203	O	Port3 RMII transmit data bit_1.
CRSDV4	4	I	Port4 RMII/MII receive interface signal, CRSDV4 is asserted high when port4 media is non_idle.
RXD4_0	5	I	Port4 RMII/MII receive data bit_0.
RXD4_1	6	I	Port4 RMII/MII receive data bit_1.
TXEN4	3	O	Port4 RMII transmit enable signal
TXD4_0	2	O	Port4 RMII/MII transmit data bit_0.
TXD4_1	1	O	Port4 RMII/MII transmit data bit_1.
CRSDV5	12	I	Port5 RMII receive interface signal, CRSDV5 is asserted high when port5 media is non_idle.
RXD5_0	13	I	Port5 RMII receive data bit_0.
RXD5_1	14	I	Port5 RMII receive data bit_1.
TXEN5	9	O	Port5 RMII transmit enable signal.
TXD5_0	8	O	Port5 RMII transmit data bit_0.
TXD5_1	7	O	Port5 RMII transmit data bit_1.

RMII Port Interface Pins			
Name	**Pin Number**	**I/O**	**Descriptions**
CRSDV6	18	I	Port6 RMII receive interface signal, CRSDV6 is asserted high when port6 media is non_idle.
RXD6_0	19	I	Port6 RMII receive data bit_0.
RXD6_1	20	I	Port6 RMII receive data bit_1.
TXEN6	17	O	Port6 RMII transmit enable signal.
TXD6_0	16	O	Port6 RMII transmit data bit_0.
TXD6_1	15	O	Port6 RMII transmit data bit_1.
CRSDV7	24	I	Port7 RMII receive interface signal, CRSDV7 is asserted high when port7 media is non_idle.
RXD7_0	25	I	Port7 RMII receive data bit_0.
RXD7_1	26	I	Port7 RMII receive data bit_1.
TXEN7	23	O	Port7 RMII transmit enable signal.
TXD7_0	22	O	Port7 RMII transmit data bit_0.
TXD7_1	21	O	Port7 RMII transmit data bit_1.
CRSDV8	32	I	Port8 RMII receive interface signal, CRSDV8 is asserted high when port8 media is non_idle.
RXD8_0	33	I	Port8 RMII receive data bit_0.
RXD8_1	34	I	Port8 RMII receive data bit_1.
TXEN8	31	O	Port8 RMII transmit enable signal.
TXD8_0	30	O	Port8 RMII transmit data bit_0.
TXD8_1	29	O	Port8 RMII transmit data bit_1.
CRSDV9	38	I	Port9 RMII receive interface signal, CRSDV9 is asserted high when port9 media is non_idle.
RXD9_0	39	I	Port9 RMII receive data bit_0.
RXD9_1	40	I	Port9 RMII receive data bit_1.
TXEN9	37	O	Port9 RMII transmit enable signal.
TXD9_0	36	O	Port9 RMII transmit data bit_0.
TXD9_1	35	O	Port9 RMII transmit data bit_1.
CRSDV10	46	I	Port10 RMII receive interface signal, CRSDV10 is asserted high when port10 media is non_idle.
RXD10_0	47	I	Port10 RMII receive data bit_0.
RXD10_1	48	I	Port10 RMII receive data bit_1.
TXEN10	45	O	Port10 RMII transmit enable signal.
TXD10_0	44	O	Port10 RMII transmit data bit_0.
TXD10_1	43	O	Port10 RMII transmit data bit_1.
CRSDV11	52	I	Port11 RMII receive interface signal, CRSDV11 is asserted high when port11 media is non_idle.
RXD11_0	53	I	Port11 RMII receive data bit_0.
RXD11_1	54	I	Port11 RMII receive data bit_1.
TXEN11	51	O	Port11 RMII transmit enable signal.
TXD11_0	50	O	Port11 RMII transmit data bit_0.
TXD11_1	49	O	Port11 RMII transmit data bit_1.

RMII Port Interface Pins			
Name	**Pin Number**	**I/O**	**Descriptions**
CRSDV12	58	I	Port12 RMII receive interface signal, CRSDV12 is asserted high when port12 media is non_idle.
RXD12_0	59	I	Port12 RMII receive data bit_0.
RXD12_1	60	I	Port12 RMII receive data bit_1.
TXEN12	57	O	Port12 RMII transmit enable signal.
TXD12_0	56	O	Port12 RMII transmit data bit_0.
TXD12_1	55	O	Port12 RMII transmit data bit_1.
CRSDV13	64	I	Port13 RMII receive interface signal, CRSDV13 is asserted high when port13 media is non_idle.
RXD13_0	65	I	Port13 RMII receive data bit_0.
RXD13_1	66	I	Port13 RMII receive data bit_1.
TXEN13	63	O	Port13 RMII transmit enable signal.
TXD13_0	62	O	Port13 RMII transmit data bit_0.
TXD13_1	61	O	Port13 RMII transmit data bit_1.
CRSDV14	72	I	Port14 RMII receive interface signal, CRSDV14 is asserted high when port14 media is non_idle.
RXD14_0	73	I	Port14 RMII receive data bit_0.
RXD14_1	74	I	Port14 RMII receive data bit_1.
TXEN14	71	O	Port14 RMII transmit enable signal.
TXD14_0	70	O	Port14 RMII transmit data bit_0.
TXD14_1	69	O	Port14 RMII transmit data bit_1.
CRSDV15	78	I	Port15 RMII receive interface signal, CRSDV15 is asserted high when port15 media is non_idle.
RXD15_0	79	I	Port15 RMII receive data bit_0.
RXD15_1	80	I	Port15 RMII receive data bit_1.
TXEN15	77	O	Port15 RMII transmit enable signal.
TXD15_0	76	O	Port15 RMII transmit data bit_0.
TXD15_1	75	O	Port15 RMII transmit data bit_1.

Synchronous DRAM/GRAM Interface Pins			
Name	**Pin Number**	**I/O**	**Descriptions**
AD[8:0]	123~131	O	Memory row/column address bus outputs AD[7:0] are row/column address [7:0]. AD[8] : This pin should connect to SGRAM/SDRAM MSB address bit.
DQ[63:0]	119~112, 84~91, 111~108, 105~102, 92~93, 96~101, 172~165, 137~139, 142~146, 164~161, 158~155, 147~154	I/O	Memory data bus DQ[63:56] : 119~112 DQ[55:48] : 84~91 DQ[47:44] : 111~108 DQ[43:40] : 105~102 DQ[39:38] : 92~93 DQ[37:32] : 96~101 DQ[31:24] : 172~165 DQ[23:21] : 137~139 DQ[20:16] : 142~146 DQ[15:12] : 164~161 DQ[11:8] : 158~155 DQ[7:0] : 147~154
RASB	134	O	SGRAM/SDRAM row address select
CASB	135	O	SGRAM/SDRAM column address select
WEB	136	O	SGRAM/SDRAM write enable
BA	132	O	SGRAM/SDRAM bank select
CS0B	133	O	Memory chip select 0
MEMCLK	121	O	Memory clock output.

Note: SGRAM/SDRAM access time: 10 ns (max)

Miscellaneous Pins			
Name	**Pin Number**	**I/O**	**Descriptions**
RESETB	180	I	System reset input, low active.
SYSCLK	82	I	Switch core system clock input
REFCLK	178	I	RMII reference clock input
MDC	181	I/O	MII management clock inout.
MDIO	182	I/O	MII management data inout
EECLK/ SDC	176	I/O	After ResetB deassert to ? ms , this pin indicate EECLK, After 150 ms, it indicate SDC.
EEDATA/ SDIO	175	I/O	After ResetB deassert to ? ms , this pin be indicated EEDATA, After 150 ms, it indicate SDIO.
LEDCLK	174	I/O	LED Clock. Using bursted clock for latching 32 display informations (one clock latch one information) , per burst have 32 continuous clocks (clock period = 320 ns); and the time between burst to burst is 655 us.

<table>
<tr><th colspan="6">Miscellaneous Pins</th></tr>
<tr><th>Name</th><th>Pin Number</th><th>I/O</th><th colspan="3">Descriptions</th></tr>
<tr><td>LEDDATA</td><td rowspan="17">173</td><td>I/O</td><td colspan="3">LED Data (high_active).
The serial output display informations using bursted styling ,per burst have 32 informations, as following:</td></tr>
<tr><td>LEDCLK</td><td>LEDDATA</td><td>LEDCLK</td><td>LEDDATA</td></tr>
<tr><td>01</td><td>P0_RxAct</td><td>17</td><td>Uti_1%</td></tr>
<tr><td>02</td><td>P1_RxAct</td><td>18</td><td>Uti_3%</td></tr>
<tr><td>03</td><td>P2_RxAct</td><td>19</td><td>Uti_5%</td></tr>
<tr><td>04</td><td>P3_RxAct</td><td>20</td><td>Uti_10%</td></tr>
<tr><td>05</td><td>P4_RxAct</td><td>21</td><td>Uti_15%</td></tr>
<tr><td>06</td><td>P5_RxAct</td><td>22</td><td>Uti_20%</td></tr>
<tr><td>07</td><td>P6_RxAct</td><td>23</td><td>Uti_30%</td></tr>
<tr><td>08</td><td>P7_RxAct</td><td>24</td><td>Uti_35%</td></tr>
<tr><td>09</td><td>P8_RxAct</td><td>25</td><td>Uti_40%</td></tr>
<tr><td>10</td><td>P9_RxAct</td><td>26</td><td>Uti_50%</td></tr>
<tr><td>11</td><td>P10_RxAct</td><td>27</td><td>Uti_60%</td></tr>
<tr><td>12</td><td>P11_RxAct</td><td>28</td><td>Uti_70%</td></tr>
<tr><td>13</td><td>P12_RxAct</td><td>29</td><td>Uti_80%</td></tr>
<tr><td>14</td><td>P13_RxAct</td><td>30</td><td>Uti_90%</td></tr>
<tr><td>15</td><td>P14_RxAct</td><td>31</td><td>BufferAlarm</td></tr>
<tr><td>16</td><td>P15_RxAct</td><td>32</td><td>MemTestFail</td></tr>
<tr><td>VCC</td><td>11,28,42,68,
83,95,107,
122,141,160,
179,190,</td><td>PWR</td><td colspan="3">Power pins</td></tr>
<tr><td>GND</td><td>10,27,41,67,
81,94,106,
120,140,159,
177,189,</td><td>GND</td><td colspan="3">Ground pins</td></tr>
</table>

3.0 Power on Setting Configuration

Jumper Configuration After Power On Reset			
Pin Name	**Function**	**default**	**Descriptions**
MDC	FlowCtrlEn	1	802.3x flow control function enable. external pull_hgih =1, 802.3x flow control enable. external pull_low = 0, 802.3x flow control disable.
EECLK	BakPsureEn	1	In Half duplex mode, backpressure function enable. external pull_hgih =1, backpressure enable. external pull_low = 0, backpressure disable.
EEDATA	MiiPollEn	1	Polling PHY device's MII register function enable. external pull_hgih =1, PHY auto polling enable. external pull_low = 0, PHY auto polling disable.
LEDCLK	AgingEn	1	Aging out function for address learning enable. external pull_hgih =1, aging out function enable. external pull_low = 0, aging out function disable.
LEDDATA	BISTEn	1	Embbeded memory self-test function enable. external pull_hgih =1, memory BIST enable. external pull_low = 0, memory BIST disable.
TXEN13	FastMode	0	For chip test only. external pull_hgih =1, chip fast test mode enable. external pull_low = 0, chip fast test mode disable.
TXEN12	ScanMode	0	For chip test only. external pull_hgih =1, chip scan test mode enable. external pull_low = 0, chip scan test mode disable.
TXEN11	8KAddrTblEn	0	8K entry address table enable. external pull_hgih =1, 8K address table enable. external pull_low = 0, 8K address table disable; defaule is 1K entry.
TXEN10	EEPROMEn	0	Auto_load from EEPROM function enable. external pull_hgih =1, auto load from EEPROM function enable. external pull_low = 0, auto load from EEPROM function disable.
TXEN9	BroadStor-mEn	0	Broadcast storm protect function enable. external pull_hgih =1, broadcast storm protection enable. external pull_low = 0, broadcast storm protection disable.
TXEN8	En12PortSW	0	For 12 port switch, only Port11~Port0 enable. external pull_hgih =1, 12 port switch enable. external pull_low = 0, default is 16 port switch.
TXEN7	P15FXEn	0	Port 15 FX function indicator. external pull_hgih =1, port15 FX function enable. external pull_low = 0, port15 FX function disable.

Jumper Configuration After Power On Reset			
Pin Name	**Function**	**default**	**Descriptions**
TXEN6	P15Full	0	Port15 duplex ability indicator (under port15 configured in FX mode). external pull_hgih =1, port15 operate in full_duplex mode. external pull_low = 0, port15 operate in half_duplex mode.
TXEN5	En1522	0	VLAN tag 1522 bytes acceptance function enable. external pull_hgih =1, VLAN tag 1522 bytes acceptance enable. external pull_low = 0, VLAN tag 1522 bytes acceptance enable disable.
TXEN4	FloodCtrlEn	0	Flooding control function enable. external pull_hgih =1, flooding control function enable. external pull_low = 0, flooding control function disable.
TXEN3	FloodID[3]	0	Flooding Port ID bit 3 external pull_hgih =1. external pull_low = 0.
TXEN2	FloodID[2]	0	Flooding Port ID bit 2 external pull_hgih =1. external pull_low = 0.
TXEN1	FloodID[1]	0	Flooding Port ID bit 1 external pull_hgih =1. external pull_low = 0.
TXEN0	FloodID[0]	0	Flooding Port ID bit 0 external pull_hgih =1. external pull_low = 0.

4.0 FUNCTIONAL DESCRIPTIONS

The MTD516 is an 16 ports 10/100 Mbps fast Ethernet switch controller. It is a low cost solution for sixteen ports fast Ethernet SOHO switch design. No CPU interface is required; After power on reset, MTD516 provide an auto load configuration setting function through a 2 wire serial EEPROM interface to acess external EEPROM device, and MTD516 can easily be configured to support port_trunking, port_ VLAN, static entry, 802.3X flow control threshold setting , flooding port assignment ...etc functions. The following descriptions are MTD516's major functional blocks overview.

4.1 Packet store and forwarding

The MTD516 use simple store and forward algorithm as packet switching method. Input packet from ports will be stored to external memory first, while packet is good for forward (CRC chech ok, 64Bytes < length < 1518Bytes, not local packets, in the same VLAN group) , if this packet's DA hits, than forward this packet to the destination port, otherwise this packet will be broadcasted.

4.2 Learning and Routing

The MTD516 supports 1K or 8K MAC entries for switching. Dynamic address learning is performed by each good unicast packet is completely received. The static address learning is achieved by EEPROM configuration. On the other hand, the routing process is performed whenever the packet's DA is captured. If the DA can not get a hit result, the packet is going to switch broadcast or forward to the dedicated port according to the flooding control selction.

4.3 Aging

Only the dynamic address entries are scheduled in the aging machine. If one station does not transmit any packet for a period of time, the belonging MAC address will be kicked out from the address table. The aging out time can be program through the EEPROM auto load configuration. (Default value is 300 seconds)

4.4 Buffer Queue Management

The buffer queue manager is implemented to manage the external shared memory (use SDRAM/ SGRAM) for packet buffering. The main function of the buffer queue manager is to maintain the linked list consists of buffer IDs, which is used to show the corresponding memory address for each incoming packet. In addition, the buffer queue manager monitors the rested free spaces status of the external memory, If the packet storage achieve the predefined threshold value, the buffer queue manager will raise the alarm signal which is used to enable the flow control mechanism for avoiding transmission ID queue overflow happening. MTD516 provide 802.3x flow control in full duplex mode and back pressure control in half duplex mode.

4.5 Full Duplex 802.3x Flow Control

In full duplex mode, MTD516 supports the standard flow control defined in IEEE802.3x standard. It enables the stopping of remote node transmissions via a PAUSE frame information interactoin. When the "802.3x flow control enable" bit is setted during power on reset (MDC pin is external pull_high), it enables MTD516 supporting 802.3x flow control function in full_duplex mode; When output port buffer queue's on_using value reach the initialization setting threshold value(recommended XON_TH = 40'h under total free ID less then 100'h), MTD516 will send out a PAUSE packet with pause time equal to FFF to stop the remote node transmission; When the output port buffer queue's on_using value reduce to the initialization threshold value(recommended Xoff_TH = 1C'h when using 2Mbytes external memory), MTD516 will also send a PAUSE packet with pause time equal to zero to inform the remote node to retransmit packet.

4.6 Half Duplex Back Pressure Control

In half duplex mode, MTD516 provide a back pressure control mechanism to avoid dropping packets during network conjection situation. When the "back pressure control enable" bit is set during power on

reset (EECLK pin is external pull_high), it enables MTD516 supporting back pressure function in half_duplex mode; When output port buffer queue's on_using value reach the initialization setting threshold value (same with the Xon_TH value), MTD516 will send a JAM pattern in the input port when it senses an incoming packet , thus force a collision to inform the remote node transmission back off and will effectively avoid dropping packets. If the "back pressure control enable" bit is not set, and there is no free buffer queue available for the incoming packets, the incoming packets will be dropped.

4.7 MII Polling

The MTD516 supports PHY management through the serial MDIO/MDC interface. After power on reset, the MTD516 write related abilities to the advertisement register 4 of connected PHY devices and restart the auto_negotiation prcedure via MDIO/MDC interface using the predefined PHY addresses increasingly from "01000"b to "10111"b. The MTD516 will periodically and continuously poll and update the link status and link partner's ability which include speed, duplex mode, and 802.3x flow control capable status of the connected PHY devices through MDIO/MDC serial interface.

4.8 MAC and DMA engine

The MTD516's MAC performs all the functions in IEEE802.3 protocol, such as frame formatting, frame stripping, CRC checking, bad packet dropping, defering to line traffic, and collision handling. The MAC Rx_engine checks incoming packets and drops the bad packet which include CRC error, alignment error, short packet (less than 64 bytes), and long packet(more than 1518 bytes or 1522 bytes when the "VLAN tag 1522 bytes receive enable" bit is set during power on reset). Before transmission, The MAC Tx_engine will constantly monitor the line traffic using derfering precedure. Only if it has been idle for a 96 bits time (a minimum interpacket gap time, IPG time), actual transmmission can be started. For the half duplex mode, MAC engine will detect collision; if a collision is detected, the MAC Tx_engine will transmit a JAM pattern and then delay the re_transmission for a random time period determined by the back_off algorithm (MTD516 implements the truncated exponential back_off algorithm defined in IEEE 802.3 standard). For the full duplex mode, collision signal is ignored.
The MTD516's DMA engine performs the packets non_blocking transportation between MAC engine and external memory according to a high speed switching procedure. The switching procedure is completed by address learning/routing process and buffer queue management operation.

4.9 EEPROM interface

MTD516 provide an auto load configuration setting function through a 2 wire serial EEPROM interface to acess external EEPROM device(24C02) after power on reset . MTD516 can easily be configured to support port_trunking, port_ VLAN, static entry, 802.3X flow control threshold setting , flooding port assignment ...etc functions.

4.10 Port Based VLAN

The MTD516 supports VLAN configuration by port based methodology. One port select the certain ports to form its VLAN group by configuring the VLAN register. The packet (including broadcast packet) is not forwarding to the destination port whose VLAN group is different from the source port.

4.11 Port Trunking

The port trunking function can also be implemented by VLAN registers. One trunk port isolates the packet transmitting and receiving from the other trunk ports, which performs a logical trunk topology. The non-trunk port should choose only one trunk port for transmitting, which can achieve the load balancing and maintain the packet sequences.

4.12 Memory Interface

Two kinds of external memory interface can be selected by user -- 2M byte memory (256K32 x 2) and 4 M bytes (512K32 x 2). Maximum 4M byte external memory can be used for packet buffering. "-10 "

speed grade of SGRAM/SDRAM device is recommanded. The following table is the SGRAM application pin connection :

Memory Type	Memory Chip No	A[8]	GND
256K32	x 2	A8	-
512K32	x 2	A9	A8

4.13 Internal MII Registers Acess and Control

The MTD516 support 2 serial pins (SDIO/SDC) for internal registers acess and control; The detailed registers informations are presented in Section5.0 (Internal MII Registers).

4.14 LED Display

The MTD516 use 2 pins to output 2 kinds of LED display -- LEDDATA, LEDCLK,
Using LEDCLK rising edge with 32 bits shift register to latch LEDDATA as DATA[31:0]. DATA[15:0] report Port15~0 link/receive activity led status. DATA[29:16] report packet buffer utilization rating, and DATA[31] report external memory test result(after power reset, MTD516 will test external SDRAM automatically), DATA[30] report the buffer almost full alarm signal .

5.0 Register Description

Global Register : Control Register (addr = 5'h0)			
Bit	**Name**	**R/W**	**Descriptions**
0	Port Reg Select enable	R/W	"1" means Reg addr1-4 as Port Registers described as follows. "0" means Reg addr1-4 as Global Registers described as follows.
4-1	Port Reg Select	R/W	If bit0 = 0, bit[4:1] don't care, and under bit[0] = 1, bit[4:1] = 0, Reg1-4 switch to Port0 Registers bit[4:1] = 1, Reg1-4 switch to Port1 Registers bit[4:1] = 2, Reg1-4 switch to Port2 Registers bit[4:1] = 3, Reg1-4 switch to Port3 Registers bit[4:1] = 4, Reg1-4 switch to Port4 Registers bit[4:1] = 5, Reg1-4 switch to Port5 Registers bit[4:1] = 6, Reg1-4 switch to Port6 Registers bit[4:1] = 7, Reg1-4 switch to Port7 Registers bit[4:1] = 8, Reg1-4 switch to Port8 Registers bit[4:1] = 9, Reg1-4 switch to Port9 Registers bit[4:1] = a, Reg1-4 switch to Port10 Registers bit[4:1] = b, Reg1-4 switch to Port11 Registers bit[4:1] = c, Reg1-4 switch to Port12 Registers bit[4:1] = d, Reg1-4 switch to Port13 Registers bit[4:1] = e, Reg1-4 switch to Port14 Registers bit[4:1] = f, Reg1-4 switch to Port15 Registers
5	Scan Mode Enable	R/W	"1" Enable "0" Disable
9-6	Scanout Group Select	R/W	bit[9:6]= 0 means group 0 , etc ...
13-10	Scanout Port Select	R/W	bit[13:10] = 0 means Port0, etc,...
15-14			Reserved
15-0	Default Value		16'h0000

Global Register : XON/XOFF Register (addr = 5'h1)			
Bit	**Name**	**R/W**	**Descriptions**
7-0	XONTH	R/W	XON threshold
15-8	XOFFTH	R/W	XOFF threshold
15-0	Default Value		XON threshold default is 8'd64(2M) XOFF threshold default is 8'h28(2M) P.S while EEPROM is enabled, this register's content will be updated by EEPROM.

Global Register : Aging Register (addr = 5'h2)			
Bit	**Name**	**R/W**	**Descriptions**
15-0	AgeTH	R/W	Aging time.
15-0	Default Value		Default is 16'd300. P.S while EEPROM is enabled, this register's content will be updated by EEPROM.

Global Register : Uplink0 Register (addr = 5'h3)			
Bit	**Name**	**R/W**	**Descriptions**
15			Reserved
14-0	Port2 ID	R/W	Specify port2's uplink port ID
9-5	Port1 ID	R/W	Specify port1's uplink port ID
4-0	Port0 ID	R/W	Specify port0's uplink port ID
15-0	Default Value		Default is 16'h001f. P.S this register's writing sequence is Jumper setting ==> EEPROM ==>MII management command.

Global Register : Uplink1 Register (addr = 5'h4)			
Bit	**Name**	**R/W**	**Descriptions**
15			Reserved
14-0	Port5 ID	R/W	Specify port5's uplink port ID
9-5	Port4 ID	R/W	Specify port4's uplink port ID
4-0	Port3 ID	R/W	Specify port3's uplink port ID
15-0	Default Value		Default is 16'h0000. P.S this register's writing sequence is Jumper setting ==> EEPROM ==>MII management command.

Global Register : Uplink2 Register (addr = 5'h5)			
Bit	**Name**	**R/W**	**Descriptions**
15			Reserved
14-0	Port8 ID	R/W	Specify port8's uplink port ID
9-5	Port7 ID	R/W	Specify port7's uplink port ID
4-0	Port6 ID	R/W	Specify port6's uplink port ID
15-0	Default Value		Default is 16'h0000. P.S this register's writing sequence is Jumper setting ==> EEPROM ==>MII management command.

Global Register : Uplink3 Register (addr = 5'h6)			
Bit	**Name**	**R/W**	**Descriptions**
15			Reserved
14-0	Port11 ID	R/W	Specify port11's uplink port ID
9-5	Port10 ID	R/W	Specify port10's uplink port ID
4-0	Port9 ID	R/W	Specify port9's uplink port ID
15-0	Default Value		Default is 16'h0000. P.S this register's writing sequence is Jumper setting ==> EEPROM ==>MII management command.

Global Register : Uplink4 Register (addr = 5'h7)			
Bit	**Name**	**R/W**	**Descriptions**
15			Reserved
14-0	Port14 ID	R/W	Specify port14's uplink port ID
9-5	Port13 ID	R/W	Specify port13's uplink port ID
4-0	Port12 ID	R/W	Specify port12's uplink port ID
15-0	Default Value		Default is 16'h0000. P.S this register's writing sequence is Jumper setting ==> EEPROM ==>MII management command.

Global Register : Uplink5 Register (addr = 5'h8)			
Bit	**Name**	**R/W**	**Descriptions**
15-5			Reserved
4-0	Port15 ID	R/W	Specify port15's uplink port ID
15-0	Default Value		Default is 16'h0000. P.S this register's writing sequence is Jumper setting ==> EEPROM ==>MII management command.

Global Register : Brdcast Storm Threshold Register (addr = 5'h9)			
Bit	**Name**	**R/W**	**Descriptions**
15-9			Reserved
8		R/W	Backpressure Enhance Mode Enable.
7-0	Brdcast TH	R/W	Specify broadcast storm threshold
15-0	Default Value		Default is 16'h00ff. P.S this register's writing sequence is Jumper setting ==> EEPROM ==>MII management command.

Global Register : Status0 Register (addr = 5'ha)			
Bit	**Name**	**R/W**	**Descriptions**
15-0	fifofull	R/O	output Port15-0 RXDMA fifofull signal

Global Register : Status1 Register (addr = 5'hb)			
Bit	**Name**	**R/W**	**Descriptions**
15-0	fifoempty	R/O	output Port15-0 TXDMA TPUR(fifoempty)signal

Global Register : Status2 Register (addr = 5'hc)			
Bit	**Name**	**R/W**	**Descriptions**
15-14		R/O	Reserved
13		R/O	Reserved
12		R/O	Reserved
11		R/O	Reserved
10	FreeCntIs0	R/O	FreeCntIs0
9	EEDONE	R/O	EEDONE
8	MemBistErr	R/O	SGRAM Bist Error
7	MemBistDone	R/O	SGRAM Bist Done
6	LthTblBistErr	R/O	Length Table Bist Error
5	LthTblBistDone	R/O	Length Table Bist Done
4	AddrTblBistErr	R/O	Internal 1K address table Bist Error
3	AddTblBist-Done	R/O	Internal 1K address table Bist Done
2	BufInitDone	R/O	Buffer link initialization Done
1	BufBistErr	R/O	Buffer Table Bist Error
0	BufBistDone	R/O	Buffer Table Bist Done

Global Register : Control/Status0 Register (addr = 5'hd)			
Bit	**Name**	**R/W**	**Descriptions**
15-0	FlowCtrl	R/W	Output MII polling port15-0 flow control information. P.S "1" means flow control is enabled
15-0	Default Value		when Polling disabled, default value is 16'hffff when Polling enabled, default value is 16'h0000.

Global Register : Control/Status1 Register (addr = 5'he)			
Bit	**Name**	**R/W**	**Descriptions**
15-0	Link	R/W	Output MII polling port15-0 link information. P.S "1" means link good
15-0	Default Value		when Polling disabled, default value is 16'hffff when Polling enabled, default value is 16'h0000.

Global Register : Control/Status2 Register (addr = 5'hf)			
Bit	**Name**	**R/W**	**Descriptions**
15-0	Speed	R/W	Output MII polling port15-0 speed information. P.S "1" means 100M
15-0	Default Value		when Polling disabled, default value is 16'hffff when Polling enabled, default value is 16'h0000.

Global Register : Control/Status3 Register (addr = 5'h10)			
Bit	**Name**	**R/W**	**Descriptions**
15-0	FullDuplex	R/W	Output MII polling port15-0 full duplex information. P.S "1" means full duplex
15-0	Default Value		when Polling disabled, default value is 16'hffff when Polling enabled, default value is 16'h0000.

Global Register : DebugReg0 Register (addr = 5'h11)			
Bit	**Name**	**R/W**	**Descriptions**
15-0	LocalFilter	R/W	"1" disable port15-0 local packet filter function.
15-0	Default Value		Default is 16'h0000

Global Register : DebugReg1 Register (addr = 5'h12)			
Bit	**Name**	**R/W**	**Descriptions**
15-0	RXLengthChk	R/W	"1" disable port15-0 Rx Length Check function.
15-0	Default Value		Default is 16'h0000

Global Register : DebugReg2 Register (addr = 5'h13)			
Bit	**Name**	**R/W**	**Descriptions**
15-0	Reserved	R/W	Reserved
15-0	Default Value		Default is 16'h0000

Global Register : DebugReg3 Register (addr = 5'h14)			
Bit	**Name**	**R/W**	**Descriptions**
15-0	CRCChk	R/W	"1" disable port15-0 CRC check function.
15-0	Default Value		Default is 16'h0000

Global Register : DebugReg4 Register (addr = 5'h15)			
Bit	**Name**	**R/W**	**Descriptions**
15-0	Random#	R/W	"1" fix port15-0 random backoff number.
15-0	Default Value		Default is 16'h0000

Global Register : DebugReg5 Register (addr = 5'h16)			
Bit	**Name**	**R/W**	**Descriptions**
15-0	Reserved	R/W	Reserved
15-0	Default Value		Default is 16'h0000

Global Register : FreeHead Register (addr = 5'h17)			
Bit	**Name**	**R/W**	**Descriptions**
15-12			Reserved.
11-0	FreeHead	R/O	Output Free List Head ID

Global Register : FreeTail Register (addr = 5'h18)			
Bit	**Name**	**R/W**	**Descriptions**
15-12			Reserved.
11-0	FreeTail	R/O	Output Free List Tail ID

Global Register : FreeCnt Register (addr = 5'h19)			
Bit	**Name**	**R/W**	**Descriptions**
15-12			Reserved.
11-0	FreeCnt	R/O	Output Free List Count Value.

Global Register : PortEnable Register (addr = 5'h1a)			
Bit	**Name**	**R/W**	**Descriptions**
15-0	PortEnable	R/W	"1" disable Port 15-0
15-0	Default		Default value is 16'h0000

Port Register : TxLinkHead Register (addr = 5'h1)			
Bit	**Name**	**R/W**	**Descriptions**
15-13			Reserved
12-0	TxLinkHead	R/O	Output Port Tx Queue Head Value

Port Register : TxLinkHead Register (addr = 5'h2)			
Bit	**Name**	**R/W**	**Descriptions**
15-13			Reserved
12-0	TxLinkCnt	R/O	Output Port Tx Queue Count Value

Port Register : VLANReg Register (addr = 5'h3)			
Bit	**Name**	**R/W**	**Descriptions**
15-0	VLANReg	R/W	Select Port VLAN Group.

6.0 EEPROM Content

EEPROM Content		
Addr	**Name**	**Descriptions**
h0	EOB	Last EEPROM content address value
h1	AgeLow	Age Time bit 7-0.
h2	AgeHigh	Age Time bit 15-8.
h3	VLAN0L	Port0 VLAN Low Byte Register.
h4	VLAN0H	Port0 VLAN Low Byte Register.
h5	VLAN1L	Port1 VLAN Low Byte Register.
h6	VLAN1H	Port1 VLAN Low Byte Register.
h7	VLAN2L	Port2 VLAN Low Byte Register.

EEPROM Content		
Addr	**Name**	**Descriptions**
h8	VLAN2H	Port2 VLAN Low Byte Register.
h9	VLAN3L	Port3 VLAN Low Byte Register.
ha	VLAN3H	Port3 VLAN Low Byte Register.
hb	VLAN4L	Port4 VLAN Low Byte Register.
hc	VLAN4H	Port4 VLAN Low Byte Register.
hd	VLAN5L	Port5 VLAN Low Byte Register.
he	VLAN5H	Port5 VLAN Low Byte Register.
hf	VLAN6L	Port6 VLAN Low Byte Register.
h10	VLAN6H	Port6 VLAN Low Byte Register.
h11	VLAN7L	Port7 VLAN Low Byte Register.
h12	VLAN7H	Port7 VLAN Low Byte Register.
h13	VLAN8L	Port8 VLAN Low Byte Register.
h14	VLAN8H	Port8 VLAN Low Byte Register.
h15	VLAN9L	Port9 VLAN Low Byte Register.
h16	VLAN9H	Port9 VLAN Low Byte Register.
h17	VLAN10L	Port10 VLAN Low Byte Register.
h18	VLAN10H	Port10 VLAN Low Byte Register.
h19	VLAN11L	Port11 VLAN Low Byte Register.
h1a	VLAN11H	Port11 VLAN Low Byte Register.
h1b	VLAN12L	Port12 VLAN Low Byte Register.
h1c	VLAN12H	Port12 VLAN Low Byte Register.
h1d	VLAN13L	Port13 VLAN Low Byte Register.
h1e	VLAN13H	Port13 VLAN Low Byte Register.
h1f	VLAN14L	Port14 VLAN Low Byte Register.
h20	VLAN14H	Port14 VLAN Low Byte Register.
h21	VLAN15L	Port15 VLAN Low Byte Register.
h22	VLAN15H	Port15 VLAN Low Byte Register.
h23	Uplink0	[4:0] Port 0 flooding port. [7:5] Reserved.
h24	Uplink1	[4:0] Port 1 flooding port. [7:5] Reserved.
h25	Uplink2	[4:0] Port 2 flooding port. [7:5] Reserved.
h26	Uplink3	[4:0] Port 3 flooding port. [7:5] Reserved.
h27	Uplink4	[4:0] Port 4 flooding port. [7:5] Reserved.
h28	Uplink5	[4:0] Port 5 flooding port. [7:5] Reserved.
h29	Uplink6	[4:0] Port 6 flooding port. [7:5] Reserved.
h2a	Uplink7	[4:0] Port 7 flooding port. [7:5] Reserved.
h2b	Uplink8	[4:0] Port 8 flooding port. [7:5] Reserved.
h2c	Uplink9	[4:0] Port 9 flooding port. [7:5] Reserved.
h2d	Uplink10	[4:0] Port 10 flooding port. [7:5] Reserved.
h2e	Uplink11	[4:0] Port 11 flooding port. [7:5] Reserved.
h2f	Uplink12	[4:0] Port 12 flooding port. [7:5] Reserved.
h30	Uplink13	[4:0] Port 13 flooding port. [7:5] Reserved.
h31	Uplink14	[4:0] Port 14 flooding port. [7:5] Reserved.
h32	Uplink15	[4:0] Port 15 flooding port. [7:5] Reserved.

EEPROM Content		
Addr	**Name**	**Descriptions**
h33	BrdcastTH	Broadcast Threshold
h34	XONTh	XON Threshold
h35	XOFFTH	XOFF Threshold
h36	DisPortL	Disable Port 7-0
h37	DisPortH	Disable Port 15-8
h38	CtrlEnable	System control byte bit0-- Enhance Backpressure Enable [7:1] Reserved.
h39-h3f		Reserved
h40-h46	StaticSA1	45[7:0]~40[7:0] means Static SA[47:0], 46[3:0] means Port ID, 46[7:4] Reserved.
h47-h4d	StaticSA2	4c[7:0]~47[7:0] means Static SA[47:0], 47[3:0] means Port ID, 47[7:4] Reserved.

7.0 Electrical Characteristics

7.1 Absolute Maximum Ratings

Symbol	Parameter	RATING	Unit
V_{CC}	Power Supply Voltage	-0.3 to 3.6	V
V_{IN}	Input Voltage	-0.3 to Vcc+0.3	V
V_{OUT}	Output Voltage	-0.3 to Vcc+0.3	V
T_{STG}	Storage Temperature	-55 to 150	^{o}C

7.2 Recommended Operating Conditions

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Power Supply	3.0	3.3	3.6	V
V_{IN}	Input Voltage	0	-	Vcc	V
T_j	Commercial Junction Operating Temperature	0	25	115	^{o}C
	Industrial Junction Operating Temperature	-40	25	125	^{o}C

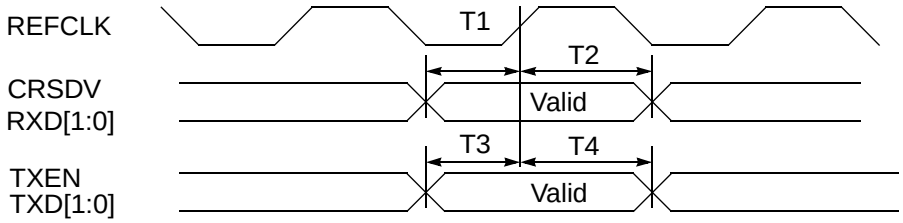
7.3 DC Electrical Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
I_{IL}	Input Leakage Current	no pull-up or down	-1		1	uA
I_{OZ}	Tri-state Leakage Current		-1		1	uA
C_{IN}	Input Capacitance			2.8		pF
C_{OUT}	Output Capacitance		2.7		4.9	pF
C_{BID3}	Bi-direction buffer Capacitance		2.7		4.9	pF
V_{IL}	Input Low Voltage	CMOS			0.3*Vcc	V
V_{IH}	Input High Voltage	CMOS	0.7*Vcc			V
V_{OH}	Output High Voltage	I_{OL}=2,4,8,12,16,24mA			0.4	V
V_{OL}	Output Low Voltage	I_{OH}=2,4,8,12,16,24mA	2.4			V
R_I	Input Pull-up/down resistance	V_{IL}=0V or V_{IH}=V_{CC}		75		KOhm

(Under recommended operating conditions and Vcc = 3.0 ~ 3.6V, Tj = 0 to +115 ^{o}C)

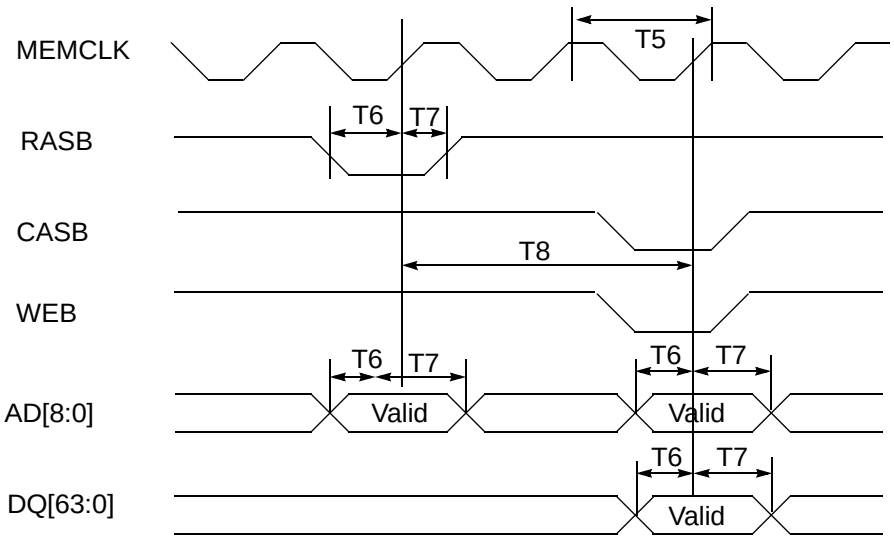
7.4 Electrical Characteristics

FIGURE 1. RMII timing



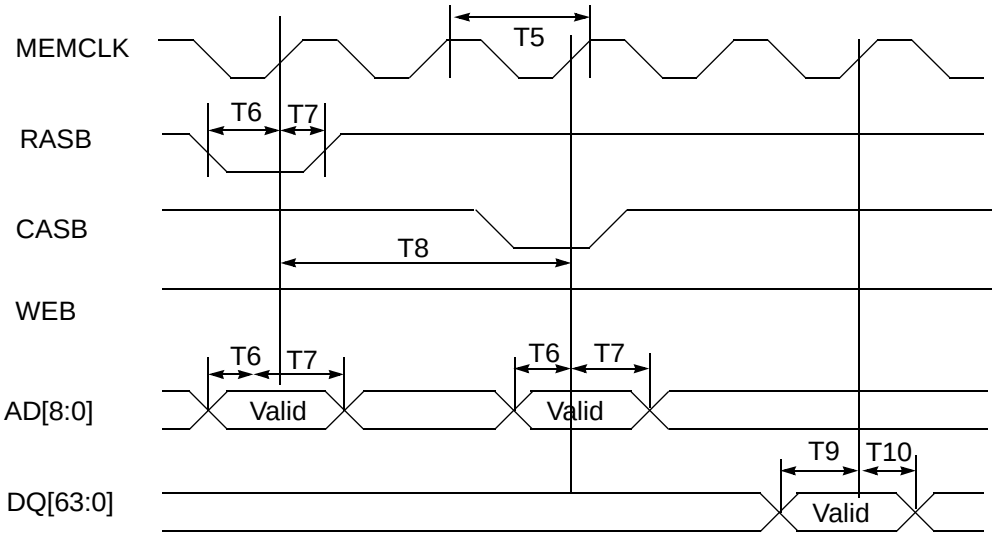
Symbol	Parameter	Min.	Typ.	Max.	Unit	Note
T1	RMII input setup time	1			nS	
T2	RMII input hold time	1			nS	
T3	RMII output setup time	3			nS	
T4	RMII output hold time	5			nS	

FIGURE 2. Memory Write Timing



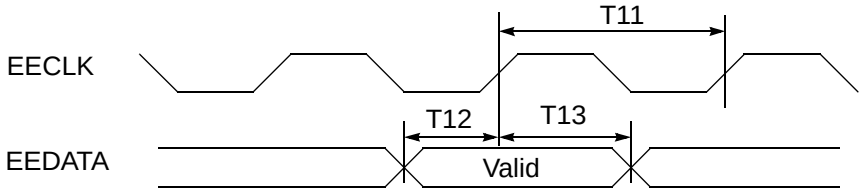
Symbol	Parameter	Min.	Typ.	Max.	Unit	Note
T5	Memory clock cycle	12			nS	
T6	Memory command/address/data setup time	6			nS	
T7	Memory command/address/data hold time	2			nS	
T8	Row active to burst write		2		CLK	

FIGURE 3. Memory Read Timing



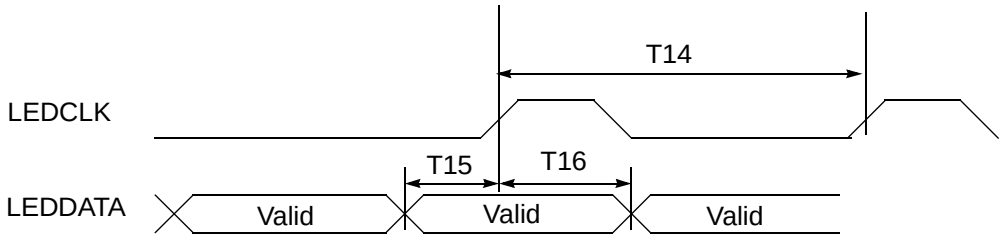
Symbol	Parameter	Min.	Typ.	Max.	Unit	Note
T10	Memory read data setup time	2			nS	
T11	Memory ead data hold time	2			nS	

FIGURE 4. EEPROM timing



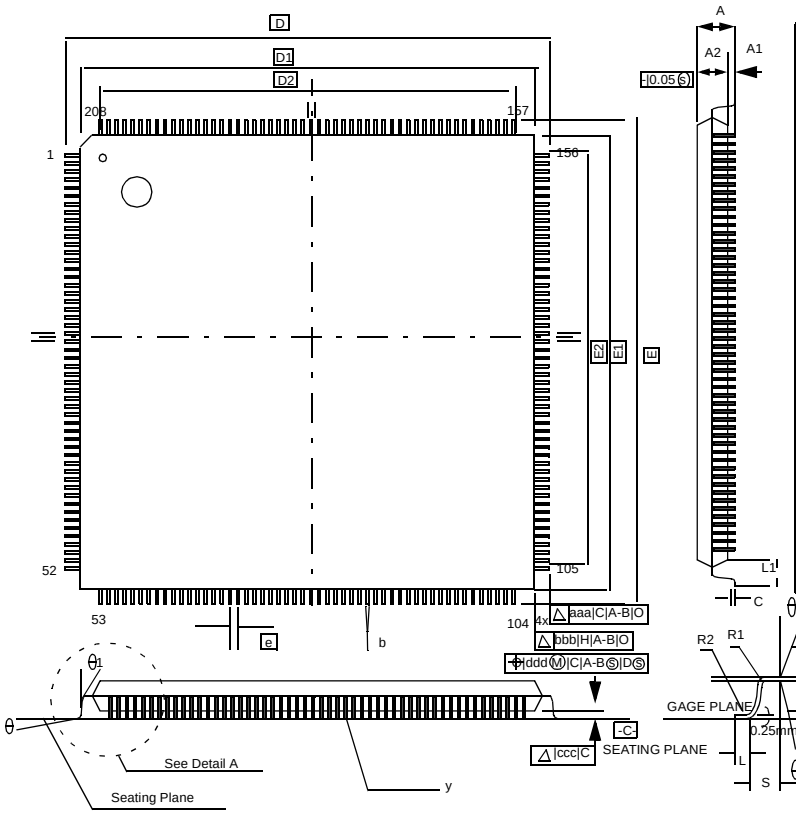
Symbol	Parameter	Min.	Typ.	Max.	Unit	Note
T11	EEPROM clock cycle		10		uS	
T12	EEDATA input setup time	1			nS	
T13	EEDATA input hold time	1			nS	

FIGURE 5. LED Interface



Symbol	Parameter	Min.	Typ.	Max.	Unit	Note
T14	Led display strobe period		20		uS	
T15	LEDCLK setup time		5		uS	
T16	LEDCLK hold time		5		uS	

8.0 208 pin PQFP Package Data



Sym-bol	Dimension in mm			Dimension in inch		
	Min	Norm	Max	Min	Norm	Max
A	-	-	4.10	-	-	0.161
A1	0.25	-	-	0.010	-	-
A2	3.20	3.32	3.60	0.126	0.131	0.142
D	30.60 BSC			1.205 BSC		
D1	28.00 BSC			1.102 BSC		
D2	25.50			1.004		
E	30.60 BSC			12.05 BSC		
E1	28.00 BSC			1.102 BSC		
E2	25.50			1.004		
R2	0.08	-	0.25	0.003	-	0.010
R1	0.08	-	-	0.003	-	-
θ	0^o	3.5^o	7^o	0^o	3.5^o	7^o
θ1	0^o	-	-	0^o	-	-
θ2	8^o REF			8^o REF		
θ3	8^o REF			8^o REF		
c	0.09	0.15	0.20	0.004	0.006	0.008
L	0.45	0.60	0.75	0.018	0.024	0.030
L1	1.30 REF			0.052 REF		
S	0.20	-	-	0.008	-	-
e	0.50 BSC			0.020 BSC		
b	0.17	0.20	0.27	0.007	0.008	0.011