



Datasheet

Small Signal IGBT/MOSFET Gate Driver Series Three-Channel Small Signal IGBT/MOSFET Gate Drivers



BD6563FV-LB

General Description

BD6563FV-LB is 3-ch gate driver to drive gate of IGBT/MOSFET from 5V input signals.

Output signals consist of each high side and low side drive signals in order to make ON/OFF timing control easy. 1 input signal generates 2 output signals which are high side output and low side output signal for 1 channel drive. High side output signal outputs "H" level and high impedance and low side output signal outputs "L" signal and high impedance.

Features

- Three-Channel Gate Drivers
- Separated Turn ON and Turn OFF Output

Applications

- Low-side IGBT/MOSFET Gate Drive for DCDC Converter
- Low-side IGBT/MOSFET Gate Drive for Inverter

•Key Specifications

- Output-side supply voltage(max.): 30V
- Input-side supply voltage: 3.0V to 5.5V
- Output peak current(≦1us):
- Input-Output delay time (at VDD=3.3V):380ns(Max.)
- Input-Output delay time (at VDD=5.0V):345ns(Max.)
- Operating temperature range: -25°C to +125°C

Package SSOP-B16

W(Typ.) x D(Typ.) x H(Max.) 5.00mm x 6.40mm x 1.35mm

±0.6A



Typical Application Circuit

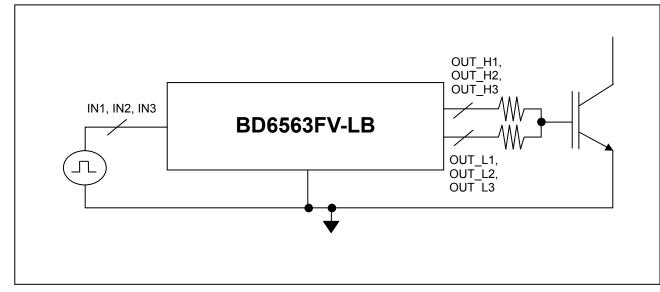


Figure 1. Typical Application Circuit

OProduct structure : Silicon monolithic integrated circuit OThis product is not designed protection against radioactive rays

●Pin Configuration

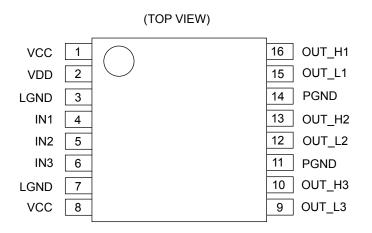


Figure 2. Pin configuration

Pin Description

Pin No.	Pin Name	Function		
1	VCC	Output-side power supply pin		
2	VDD	Input-side power supply pin		
3	LGND	Input-side ground pin		
4	IN1	Control input 1 pin		
5	IN2	Control input 2 pin		
6	IN3	Control input 3 pin		
7	LGND	Input-side ground pin		
8	VCC	Output-side power supply pin		
9	OUT_L3	Low-side output 3 pin		
10	OUT_H3	High-side output 3 pin		
11	PGND	Output-side ground pin		
12	OUT_L2	Low-side output 2 pin		
13	OUT_H2	High-side output 2 pin		
14	PGND	Output-side ground pin		
15	OUT_L1	Low-side output 1 pin		
16	OUT_H1	High-side output 1 pin		

Block Diagram

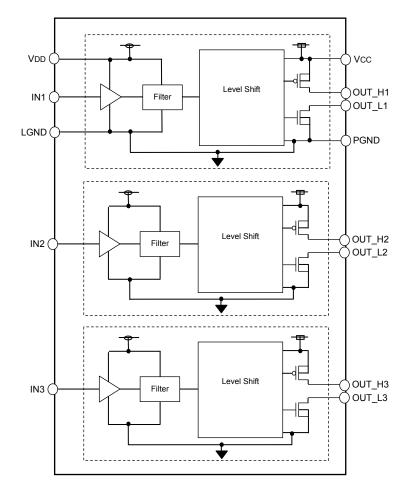


Figure 3. Block Diagram

•Absolute Maximum Ratings

Parameter	Symbol	Limits	Units
Output-side supply voltage	V _{CCMAX}	30	V
Input-side supply voltage	V _{DDMAX}	7	V
INX ^{*1} pin input voltage	V _{INXMAX}	-0.3 to VDD+0.3	V
OUT_HX / OUT_LX ^{*1} pin output voltage	Vouthxmax Voutlxmax	-0.3 to VCC+0.3	V
OUT_HX ^{*1} pin output current (Peak 1us)	I _{OUTHXMAX}	-0.6* ²	А
OUT_LX ^{*1} pin output current (Peak 1us)	IOUTLXMAX	+0.6*2	А
Power dissipation	Pd	0.87* ³	W
Operating temperature range	T _{OPR}	-25 to +125	°C
Storage temperature range	T _{stg}	-55 to +150	°C
Junction temperature	Tjmax	+150	°C

X=1,2,3

*1 *2 *3 Should not exceed Pd and Tj=150°C.

Derate above Ta=25°C at a rate of 7.0mW/°C. Mounted on a glass epoxy of 70 mm × 70 mm × 1.6 mm.

Recommended Operating Ratings

Parameter	Symbol	Min.	Max.	Units
Output-side supply voltage	V _{CC}	10	25	V
Input-side supply voltage	V _{DD}	3.0	5.5	V
INX ^{*1} high level input voltage	V _{DD}	V _{DD} ×0.7	-	V
INX ^{*1} low level input voltage	V _{DD}	-	V _{DD} ×0.3	V

*1 X=1,2,3

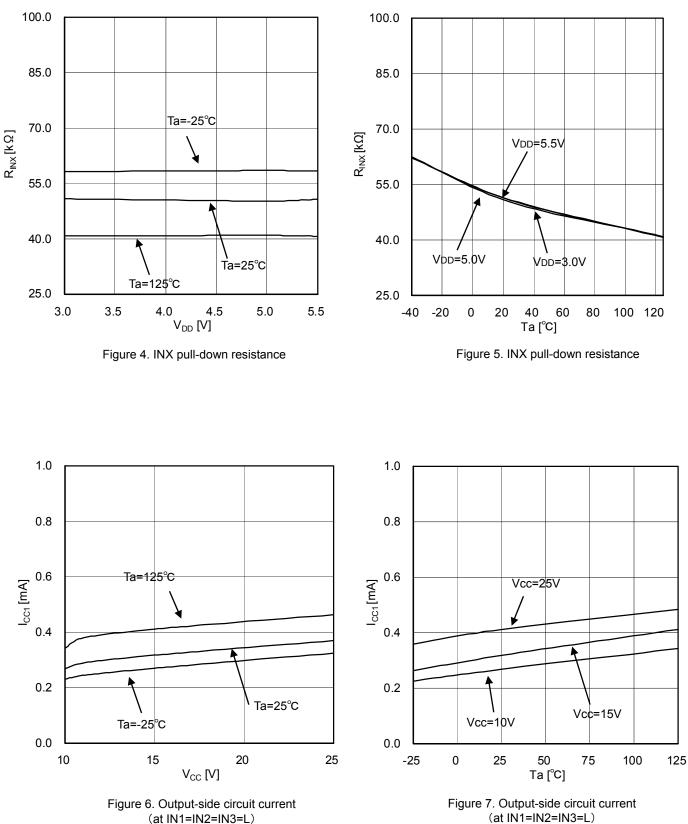
•Electrical Characteristics

(Unless otherwise specified Ta=-25°C to 125°C, V $_{\text{DD}}$ =3.0V to 5.5V, V $_{\text{CC}}$ =10V to 25V)

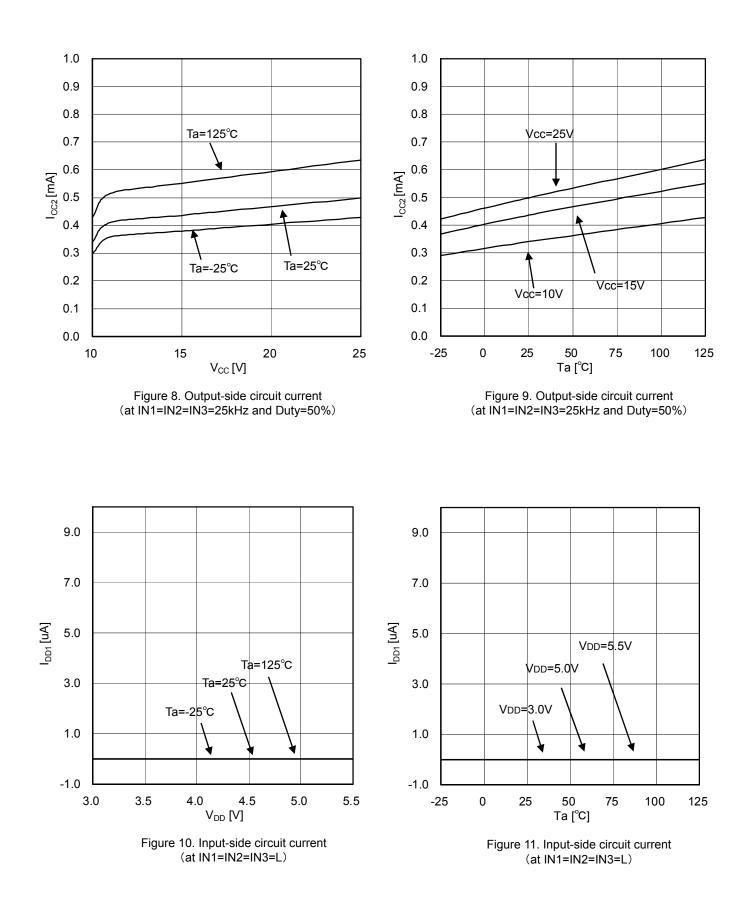
Parameter	Symbol	Min.	Тур.	Max.	Unit	Conditions
INX * ¹ pull-down resistance	R _{INX}	25	50	100	kΩ	
Output-side circuit current 1	I _{CC1}	-	0.32	1	mA	IN1=IN2=IN3=0V
Output-side circuit current 2	I _{CC2}	-	0.43	1	mA	IN1=IN2=IN3=25kHz, Duty=50%
Input-side circuit current 1	I _{DD1}	-	0	10	uA	IN1=IN2=IN3=0V
Input-side circuit current 2	I _{DD2}	-	25	100	uA	IN1=IN2=IN3=25kHz, Duty=50%
High level output voltage	V _{OUTHX}	VCC-2.0	VCC-1.0	VCC-0.4	V	I _{OUTHX} =-100mA
Low level output voltage	V _{OUTLX}	0.15	0.4	1.0	V	I _{OUTLX} =100mA
Output delay time H 1	t _{PLHX1}	170	250	330	ns	V _{DD} =5.0V
Output delay time L 1	t _{PHLX1}	185	265	345	ns	V _{DD} =5.0V
Delay matching 1, OUT_HX and OUT_LX tPLHX1 - tPHLX1 * ¹		-30	-15	0	ns	V _{DD} =5.0V
Output delay time H 2	t _{PLHX2}	170	250	330	ns	V _{DD} =3.3V
Output delay time L 2	t _{PHLX2}	220	300	380	ns	V _{DD} =3.3V
Delay matching 2, OUT_HX and OUT_LX tPLHX2 - tPHLX2 * ¹	⊿t _{PLHX2-PHLX2}	-80	-50	0	ns	V _{DD} =3.3V
Delay matching, OUT_H1,OUT_H2,OUT_H3 tPLHX - tPLHY * ^T	∕t _{PLH}	-20	0	20	ns	
Delay matching, OUT_L1,OUT_L2,OUT_L3 tPHLX - tPHLY * ^T	∕t _{PHL}	-20	0	20	ns	

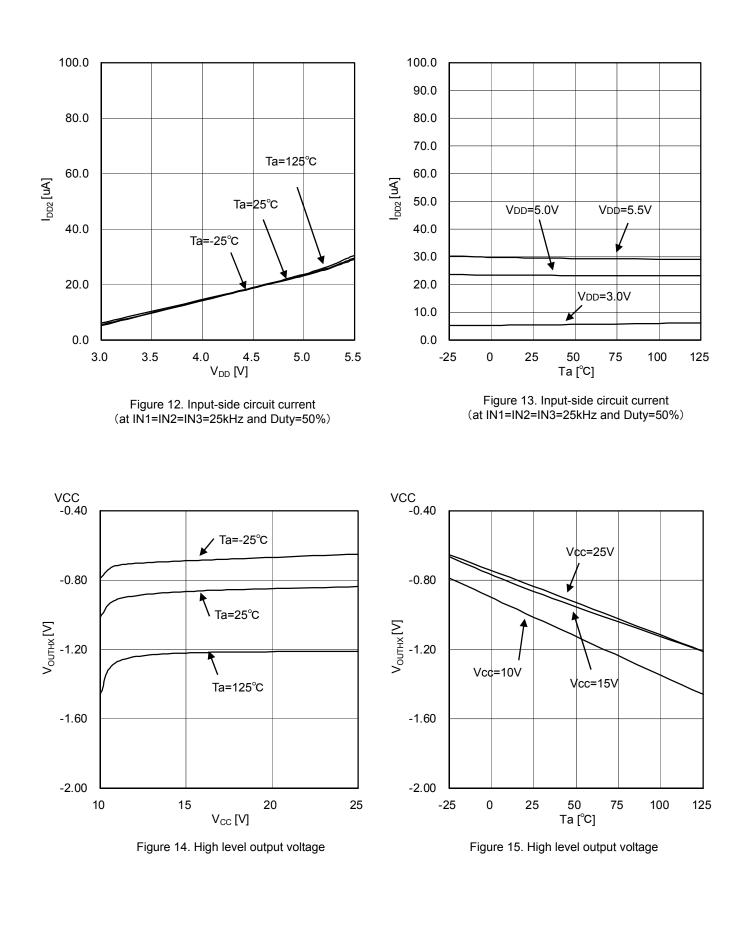
*1 X=1,2,3, Y=1,2,3

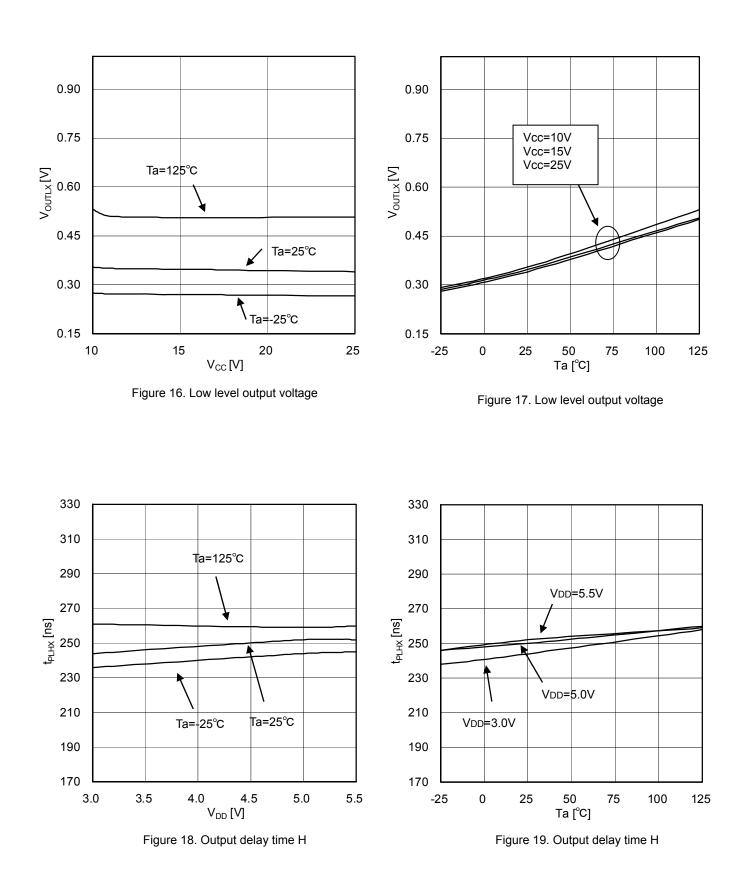
Typical Performance Curves

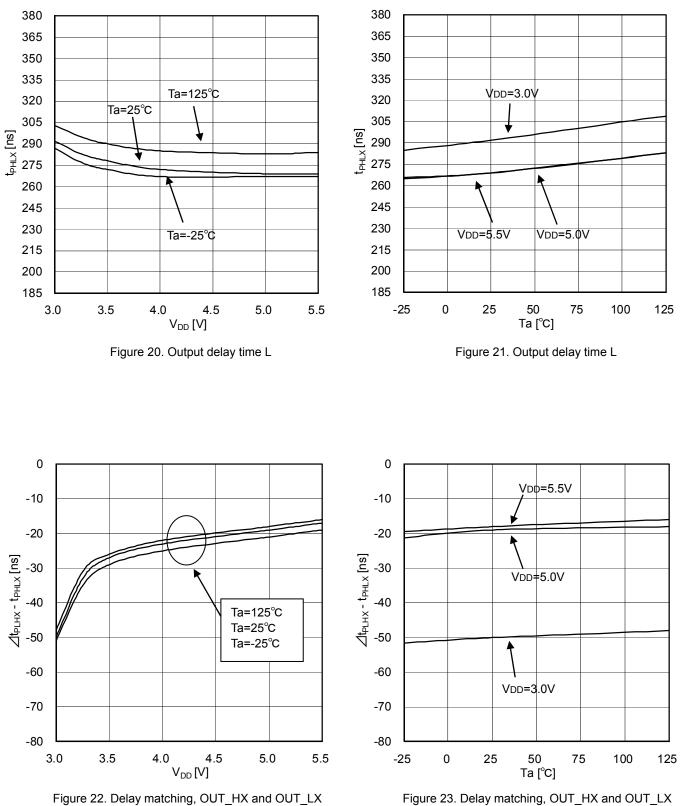


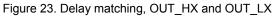
(at IN1=IN2=IN3=L)











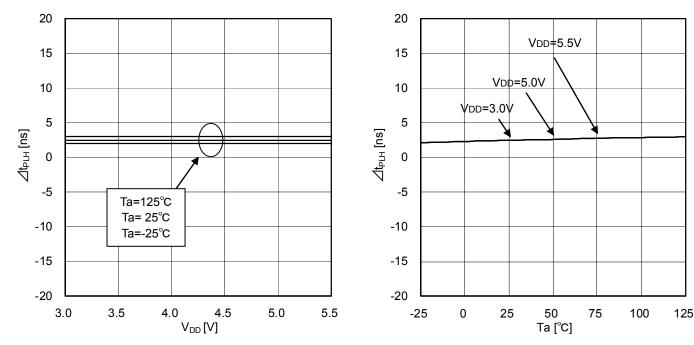
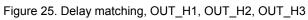


Figure 24. Delay matching, OUT_H1, OUT_H2, OUT_H3



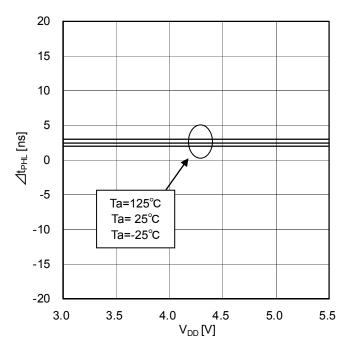


Figure 26. Delay matching, OUT_L1, OUT_L2, OUT_L3

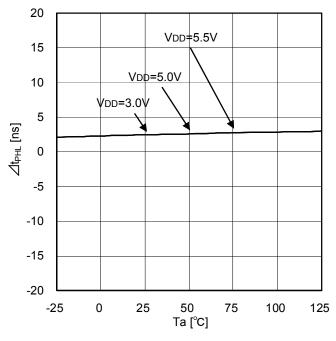
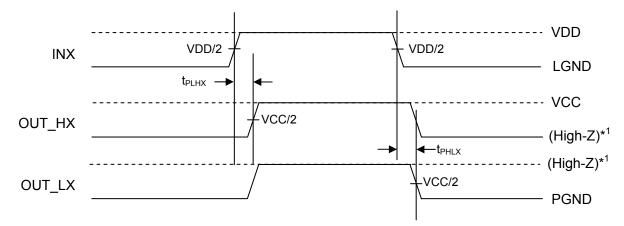


Figure 27. Delay matching, OUT_L1, OUT_L2, OUT_L3

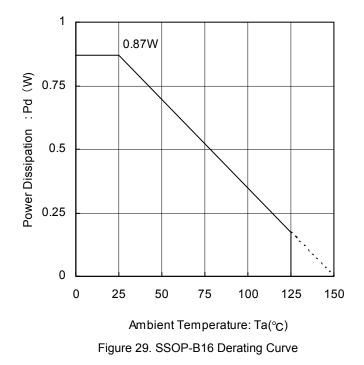
Timing Chart



*1 Under condition that OUT_HX and OUT_LX are shorted.



Power Dissipation



Please confirm that the IC's chip temperature Tj is not over 150°C, while considering the IC's power consumption (W), package power (Pd) and ambient temperature (Ta). When Tj=150°C is exceeded the functions as a semiconductor do not operate and some problems (ex. Abnormal operation of various parasitic elements and increasing of leak current) occur. Constant use under these circumstances leads to deterioration and eventually IC may destruct. Tjmax=150°C must be strictly obeyed under all circumstances.

●I/O equivalence circuits

Pin No.	Name	I/O equivalence circuits			
FIII NO.	Function				
4, 5, 6	IN1, IN2, IN3				
	Control input X pin				
9, 12, 15	OUT_L1, OUT_L2, OUT_L3				
	Low-side output X pin	OUT_L1, OUT_L2, OUT_L3			
10, 13, 16	OUT_H1, OUT_H2, OUT_H3				
	High-side output X pin	OUT_H1, OUT_H2, OUT_H3			

Operational Notes

(1) Absolute maximum ratings

An excess in the absolute maximum ratings, such as supply voltage, temperature range of operating conditions, etc., can break down the devices, thus making impossible to identify breaking mode, such as a short circuit or an open circuit. If any over rated values will expect to exceed the absolute maximum ratings, consider adding circuit protection devices, such as fuses.

(2) Connecting the power supply connector backward

Connecting of the power supply in reverse polarity can damage IC. Take precautions when connecting the power supply lines. An external direction diode can be added.

(3) Power supply Lines

Design PCB layout pattern to provide low impedance GND and supply lines. To obtain a low noise ground and supply line, separate the ground section and supply lines of the digital and analog blocks. Furthermore, for all power supply terminals to ICs, connect a capacitor between the power supply and the GND terminal. When applying electrolytic capacitors in the circuit, not that capacitance characteristic values are reduced at low temperatures.

(4) GND Potential

The potential of LGND pin and PGND pin must be minimum potential in all operating conditions.

(5) Thermal design

Use a thermal design that allows for a sufficient margin in light of the power dissipation (Pd) in actual operating conditions.

(6) Inter-pin shorts and mounting errors

When attaching to a printed circuit board, pay close attention to the direction of the IC and displacement. Improper attachment may lead to destruction of the IC. There is also possibility of destruction from short circuits which can be caused by foreign matter entering between outputs or an output and the power supply or GND.

(7) Operation in a strong electric field

Use caution when using the IC in the presence of a strong electromagnetic field as doing so may cause the IC to malfunction.

(8) Inspection of the application board

During inspection of the application board, if a capacitor is connected to a pin with low impedance there is a possibility that it could cause stress to the IC, therefore an electrical discharge should be performed after each process. Also, as a measure again electrostatic discharge, it should be earthed during the assembly process and special care should be taken during transport or storage. Furthermore, when connecting to the jig during the inspection process, the power supply should first be turned off and then removed before the inspection.

(9) Input terminal of IC

Between each element there is a P+ isolation for element partition and a P substrate. This P layer and each element's N layer make up the P-N junction, and various parasitic elements are made up.

For example, when the resistance and transistor are connected to the terminal as shown in figure 65,

OWhen GND>(Terminal A) at the resistance and GND>(Terminal B) at the transistor (NPN), the P-N junction operates as a parasitic diode.

OAlso, when GND>(Terminal B) at the transistor (NPN), The parasitic NPN transistor operates with the N layers of other elements close to the aforementioned parasitic diode.

Because of the IC's structure, the creation of parasitic elements is inevitable from the electrical potential relationship. The operation of parasitic elements causes interference in circuit operation, and can lead to malfunction and destruction. Therefore, be careful not to use it in a way which causes the parasitic elements to operate, such as by applying voltage that is lower than the GND (P substrate) to the input terminal.

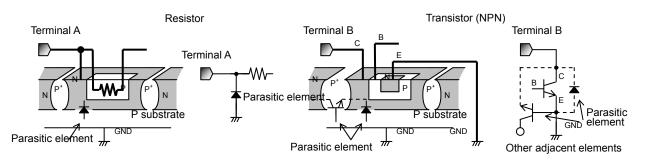


Figure 30. Pattern Diagram of Parasitic Element

(10) Ground Wiring Patterns

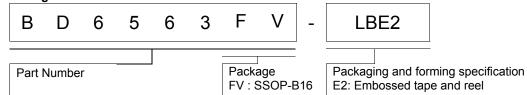
When using both small signal and large current GND patterns, it is recommended to isolate the two ground patterns, placing a single ground point at the application's reference point so that the pattern wiring resistance and voltage variations caused by large currents do not cause variations in the small signal ground voltage. Be careful not to change the GND wiring pattern potential of any external components, either.

The Japanese version of this document is formal specification. A customer may use this translation version only for a reference to help reading the formal version.

If there are any differences in translation version of this document formal version takes priority

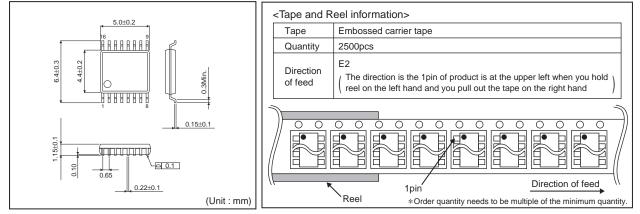
BD6563FV-LB

Ordering Information

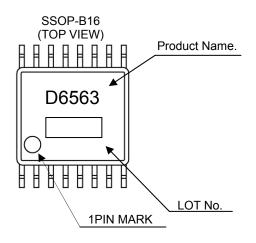


Physical Dimension Tape and Reel Information

SSOP-B16



Marking Diagram



BD6563FV-LB

Revision History

Date	Revision	Changes
05.JUL.2012	001	New Release
13.JUL.2012	002	Page 1 : Change Key Specifications 'Output peak current' Page 4 : Change Absolute Maximum Ratings 'OUT_HX pin output current' Page 4 : Change Absolute Maximum Ratings 'OUT_LX pin output current'

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 - [g] Use of our Products without cleaning residue of flux (even if you use no-clean type fluxes, cleaning residue of flux is recommended); or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
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 - [d] the Products are exposed to high Electrostatic
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