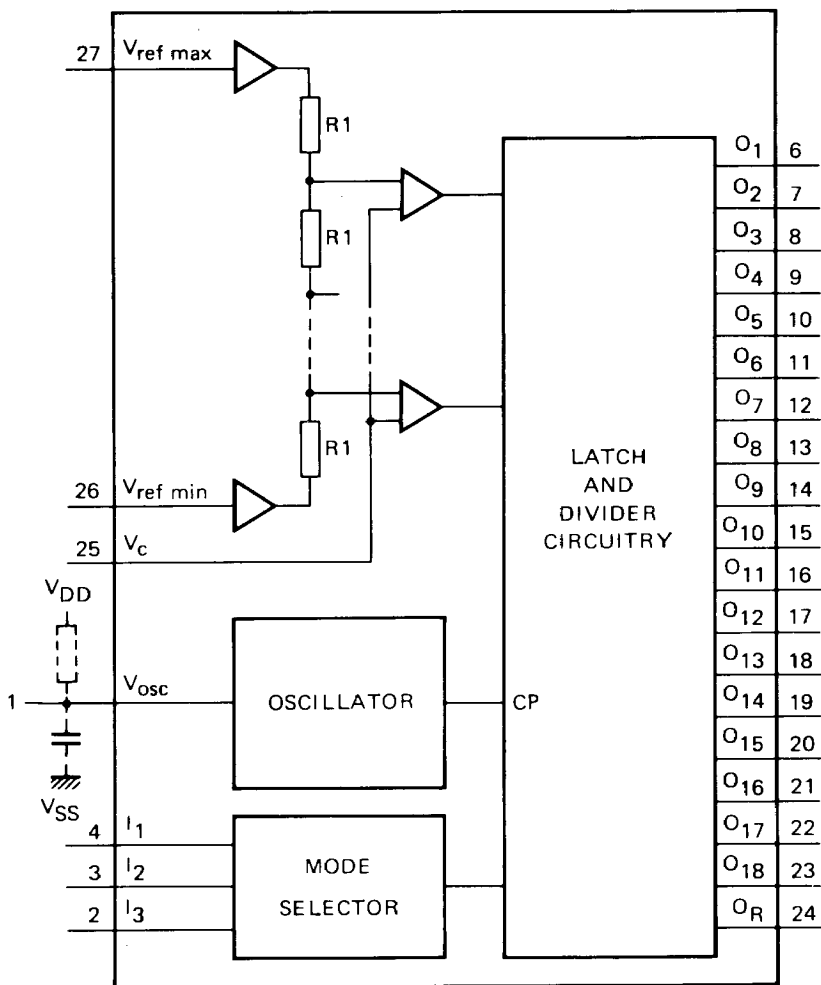# 18-ELEMENT BAR GRAPH LCD DRIVER
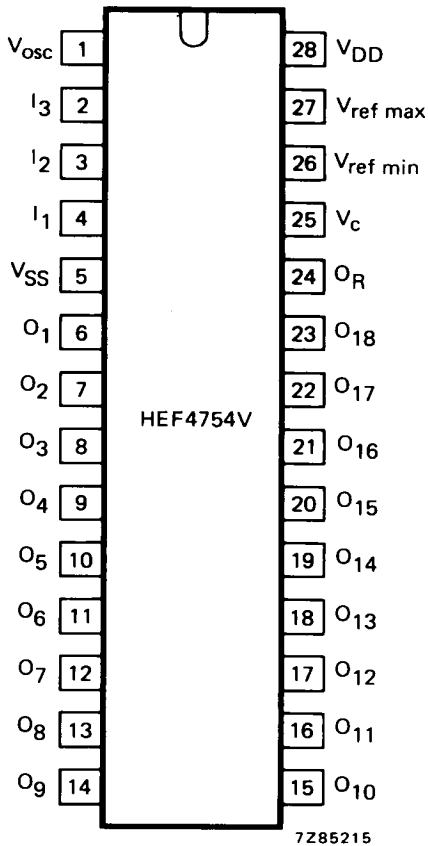
The HEF4754V drives an 18-element bar graph LCD in linear relation to the control voltage (V_c) in a pointer or thermometer mode.

7Z85217

Fig. 1 Functional diagram.

FAMILY DATA see Family Specifications

PINNING

V_{osc}	oscillator terminal
V_c	control voltage input
$V_{ref\,min}$ $V_{ref\,max}$	reference voltage inputs
I_1	thermometer/pointer (choice select input)
I_2	peak value; reset/9 or 18 bars (choice select input)
I_3	reset; repetitively reset (choice select input)
O_1 to O_{18}	bar outputs
O_R	back plate output

Pinning diagram (left to right):

Pin	Signal		Pin	Signal
1	V_{osc}		28	V_{DD}
2	I_3		27	$V_{ref\,max}$
3	I_2		26	$V_{ref\,min}$
4	I_1		25	V_c
5	V_{SS}		24	O_R
6	O_1		23	O_{18}
7	O_2		22	O_{17}
8	O_3		21	O_{16}
9	O_4		20	O_{15}
10	O_5		19	O_{14}
11	O_6		18	O_{13}
12	O_7		17	O_{12}
13	O_8		16	O_{11}
14	O_9		15	O_{10}

HEF4754V

7Z85215

Fig. 2 Pinning diagram.

HEF4754VP : 28-lead DIL; plastic (SOT-117).
HEF4754VD : 28-lead DIL; ceramic (cerdip) SOT-135A).
HEF4754VT : 28-lead mini-pack; plastic (SO-28; SOT-136A).

FUNCTION TABLE

I_1	I_2	I_3	mode
L	L	X	pointer; 18 bars
L	H	X	pointer; 9 bars
H	L	X	thermometer; no peak value
H	H	L	thermometer; peak value, repetitively reset
H	H	H	thermometer; peak value, manually reset

H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)
X = state is immaterial

GENERAL DESCRIPTION

The HEF4754V drives an 18-element bar graph LCD in linear relation to the control voltage (V_c) in a pointer or thermometer mode. The first bar lights up when V_c is smaller than $V_{T(bar)2}$ (see equation [3] below).

In the pointer mode, the circuit can drive 9 or 18 bars; in the thermometer mode, the circuit also drives the peak value indication. This can be reset or repetitively reset, after 1,5 to 2 seconds.

The circuit has analogue and digital parts. The analogue part consists of 17 comparators, with their non-inverting inputs connected together and coupled to the control input V_c. The inverting inputs of the comparators are connected in succession to the nodes of an 18-part resistor divider. The distance between the switching levels of the comparators is defined by the voltage difference across this divider. The extremities of the resistor divider are coupled via high-input amplifiers to the maximum reference voltage input and the minimum reference voltage input.

The digital part has one reference output (O_R) to drive the back plate, and 18 outputs (O_1 to O_{18}) to drive each bar. Three latches and some gates are incorporated for each bar output. An on-chip oscillator (1024 Hz) with external R and C drives the circuit. The outputs are driven at 64 Hz. The select inputs I_1 to I_3 are provided with an on-chip pull-up element, and they may therefore be left floating (equals HIGH state).

LINEARITY

V_{DD} = 10 V; $V_{ref\ max}$ = 9,5 V; $V_{ref\ min}$ = 0,5 V; T_{amb} = 25 °C

ΔV_1 = 250 mV (this is the tolerance of the step voltage).

$$V_{step} = V_{step}' + \Delta V_1 \qquad [1]$$

V_{step}' is the (internal) voltage drop across the resistor-ladder network.

$$V_{step}' = \frac{(V_{ref\ max} \pm \Delta V_2) - (V_{ref\ min} \pm \Delta V_2)}{18} \qquad [2]$$

ΔV_2 is the maximum offset voltage spread of the on-chip voltage follower.

ΔV_2 = 250 mV.

The linearity is guaranteed for $V_{DD} > 10$ V.
The monotony between V_{DD} = 5 V and 10 V is guaranteed. During ramping-up of the input voltage a maximum of two bars might be activated simultaneously.

ABSOLUTE VOLTAGE TRIGGER LEVEL

The absolute voltage trigger level at the V_c pin is $V_{T(bar)n}$:

$$V_{T(bar)n} = (V_{ref\ min} \pm \Delta V_2{}^*) + \{ (n-1)\ V_{step}' \pm \Delta V_1 \}, \text{ in which} \qquad [3]$$

n = number of bars; $2 \leqslant n \leqslant 18$.

For n = 1 (first bar) see text above.

* For ΔV_2 the same sign (+ or −) should be used as in equation [2].

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	V_{DD}	$-0,5$ to $+18$ V
Voltage on any input	V_I	$-0,5$ to $V_{DD} + 0,5$ V
D.C. current into any input or output	$\pm I_I$ max.	10 mA
Storage temperature	T_{stg}	-25 to $+125$ °C
Operating ambient temperature	T_{amb}	-20 to $+85$ °C

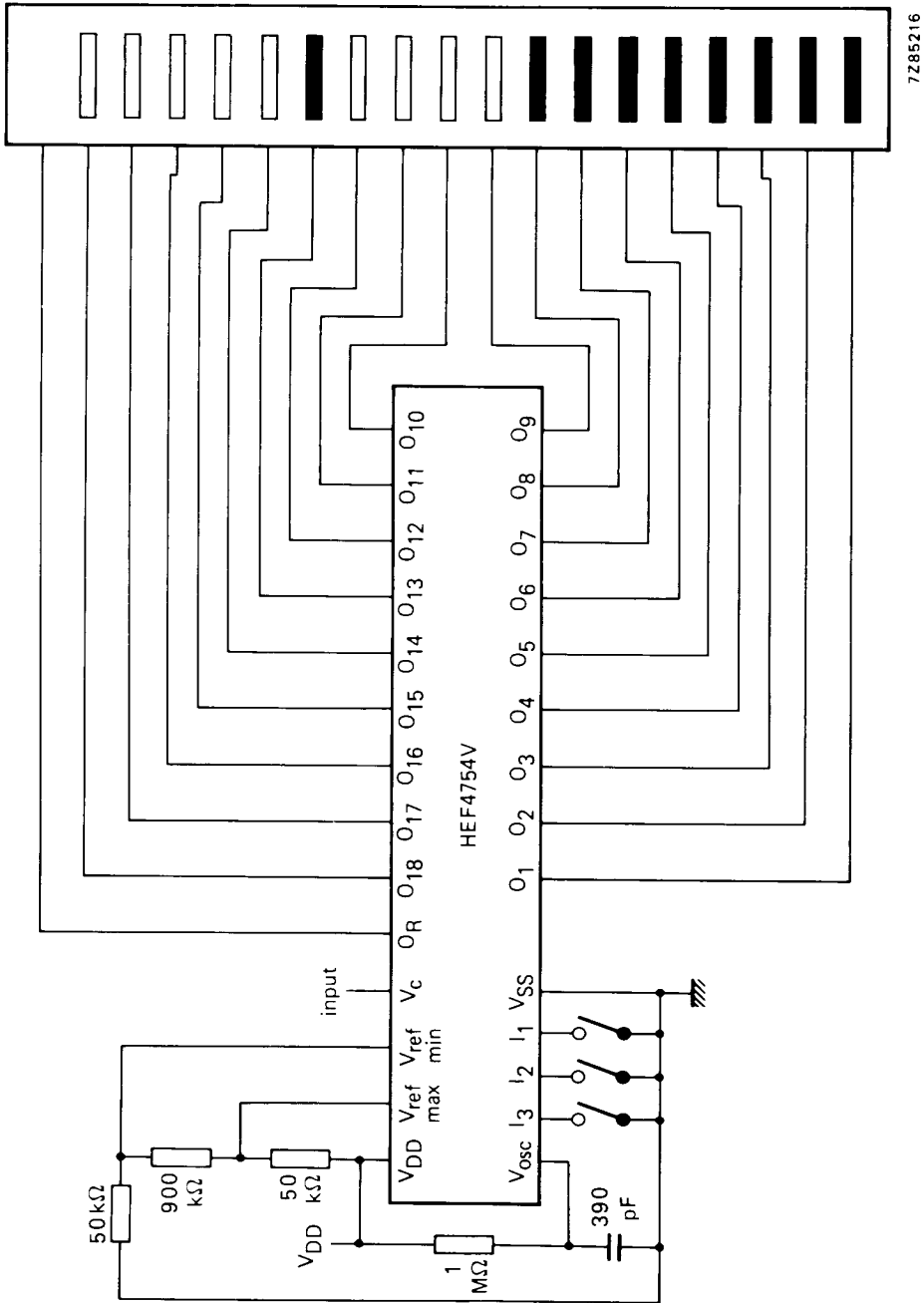## NOTES (to D.C. CHARACTERISTICS)

1. $V_{ref\,min} = 0,5$ V; $V_{ref\,max} = 9,5$ V; $V_{osc} = V_c = 0$ V; I_1, I_2 and I_3 at V_{DD}.

2. Pin under test at V_{SS} or V_{DD}, all other inputs simultaneously at V_{SS} or V_{DD}.

3. $I_O = 0$; all inputs at V_{SS} or V_{DD}.

4. At $V_{DD} = 5$ V: $V_{OH} = 4,5$ V.
   At $V_{DD} = 10$ V: $V_{OH} = 9,5$ V.
   At $V_{DD} = 15$ V: $V_{OH} = 13,5$ V.

5. At $V_{DD} = 5$ V: $V_{OL} = 0,4$ V; inputs at V_{SS} or V_{DD}.
   At $V_{DD} = 10$ V: $V_{OL} = 0,5$ V; inputs at V_{SS} or V_{DD}.
   At $V_{DD} = 15$ V: $V_{OL} = 1,5$ V; inputs at V_{SS} or V_{DD}.

6. $V_{ref\,min} + 4$ V $< V_{ref\,max}$.

D.C. CHARACTERISTICS

$V_{SS} = 0$ V

	V_{DD} V	symbol	T_{amb} (°C) −40 min.	max.	+25 min.	typ.	max.	+85 min.	max.		notes
Quiescent device current	5	I_{DD}	−	−	−	−	−	−	−	μA	1
	10		−	−	−	−	1000	−	−	μA	
	15		−	−	−	−	1600	−	−	μA	
Input leakage current (except select inputs)	5	$\pm I_{IN}$	−	−	−	−	100	−	−	nA	2
	10		−	−	−	−	100	−	−	nA	
	15		−	−	−	−	100	−	−	nA	
Input voltage HIGH select inputs	5	V_{IH}	3,5	−	3,5	−	−	3,5	−	V	
	10		7,0	−	7,0	−	−	7,0	−	V	
	15		11,0	−	11,0	−	−	11,0	−	V	
Input voltage LOW select inputs	5	V_{IL}	−	1,5	−	−	1,5	−	1,5	V	
	10		−	3,0	−	−	3,0	−	3,0	V	
	15		−	4,0	−	−	4,0	−	4,0	V	
Output voltage HIGH	5	V_{OH}	4,99	−	4,99	−	−	4,95	−	V	3
	10		9,99	−	9,99	−	−	9,95	−	V	
	15		−	−	14,99	−	−	−	−	V	
Output voltage LOW	5	V_{OL}	−	0,01	−	−	0,01	−	0,05	V	3
	10		−	0,01	−	−	0,01	−	0,05	V	
	15		−	0,01	−	−	0,01	−	0,05	V	
Output current HIGH	5	$-I_{OH}$	0,36	−	0,3	−	−	0,24	−	mA	4
	10		0,80	−	0,7	−	−	0,56	−	mA	
	15		3,0	−	2,8	−	−	2,60	−	mA	
Output current LOW	5	I_{OL}	0,34	−	0,3	−	−	0,24	−	mA	5
	10		1,00	−	0,9	−	−	0,72	−	mA	
	15		4,40	−	4,0	−	−	3,20	−	mA	
Input voltage control input V_c	5	V_{IC}	−	−	0	−	5	−	−	V	6
	10		−	−	0	−	10	−	−	V	
	15		−	−	0	−	15	−	−	V	
Max. input voltage $V_{ref\ max}$ input	5	V_{IRmax}	−	−	4,5	−	4,5	−	−	V	6
	10		−	−	4,5	−	9,5	−	−	V	
	15		−	−	4,5	−	14,5	−	−	V	
Min. input voltage $V_{ref\ min}$ input	5	V_{IRmin}	−	−	0,5	−	0,5	−	−	V	6
	10		−	−	0,5	−	5,5	−	−	V	
	15		−	−	0,5	−	10,5	−	−	V	
Operating supply current	10	I_{DD}	−	−	−	750	−	−	−	μA	Fig. 3

For notes see opposite page.

Fig. 3 Typical operating set-up.