National Semiconductor Corporation

PRELIMINARY
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TP3110/TP3112/TP3120/TP3122 Digital Line Interface Controllers (DLIC)

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General Description

The TP3110, TP3120, TP3112, TP3122 Digital Line Interface Controllers (DLIC) are general purpose switching components primarily intended to serve as controllers of subscriber line, service and trunk circuit cards of a digital switching system. They are also useful as general purpose data controllers for data switching and multiplexing applications.

The DLIC performs a three-way control function when used for digital switching applications. The block diagram (*Figure 1*) displays this tri-port arrangement. First, the DLIC controls the space and time switching function between subscriber line PCM CODECs/filters (COMBO™) and the switching system time division multiplex (TDM) highways. Second, the DLIC controls the flow of information between the per line circuit devices and the line card's local processor. Last, it performs all protocol control functions, using the HDLC protocol format, for information passing between the local line card processor and the main switching system processor (or any other system processor).

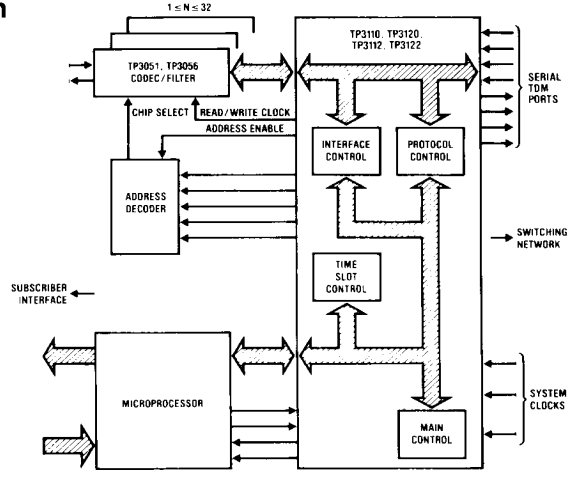
The DLIC is configured with a parallel interface for the per line and local processor circuits and with full duplex multiple port serial highways for the system interface. All system related communications with the DLIC controlled circuit card are handled via channel assignments on the serial TDM interface. In this way, all system data communications, subscriber PCM, data, signaling and system control information are transported and switched with a single network. This approach improves the overall flexibility and modularity of the total system design.

The DLIC contains a time-slot memory map for up to 128 duplex TDM channels, four high speed serial port transceivers, interface logic to allow the local processor to communicate with the per line circuit devices (COMBO circuits and the SLIC), a complete HDLC protocol controller for system control messages, a vectored interrupt controller for the HDLC protocol, signaling and timing control and finally, a buffer memory for per line signaling data.

Features

- A complete interface controller for up to 32 subscribers of a digital switching system
- Performs all time division multiplex (TDM) channel assignments for the circuit card it controls
- 2 Tx and Rx TDM ports (TP3110, TP3112)
- 4 Tx and Rx TDM ports (TP3120, TP3122)
- Interfaces TP3051/6 parallel CODEC/Filter COMBO
- Only 1 Time Slot delay
- System control uses the HDLC protocol with all zero insertion/deletion, checksum and flag control functions performed by the DLIC
- Assignable addressing plus a "broadcast" address allows up to 255 controllers per subsystem control group without address field overlap
- Master mode allows DLIC to function as the group controller
- Single 5V power supply operation

System Diagram



TL/H/6699–1

FIGURE 1. DLIC Signal Flows

TRI-STATE® is a registered trademark of National Semiconductor Corp.
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RRD-B20M125/Printed in U. S. A.

Absolute Maximum Ratings

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

V_{DD} Relative to V_{SS}	7.0V
Voltage at Any Input or Output	V_{SS} − 0.3V to V_{DD} + 0.3V
Operating Temperature Range (Ambient)	−25°C to +70°C
Storage Temperature Range (Ambient)	−65°C to +150°C
Maximum Lead Temp. (Soldering, 10 seconds)	300°C

DC Electrical Characteristics

Unless otherwise noted, limits printed in **BOLD** characters are guaranteed for V_{DD} = +5V ±5%, V_{SS} = GNDD (digital ground), T_A = 0°C to +70°C by correlation with 100% electrical testing at T_A = +25°C. All other limits are assured by correlation with other production tests and/or product design and characterization.

Parameter	Conditions	Min	Typ	Max	Units
Input Voltage Levels					
V_{IH}, Logic High		**2.0**			V
V_{IL}, Logic low				**0.7**	V
Output Voltage Levels					
V_{OH}, Logic High	I_{OUT} = 10 μA (Note 1)	**4.0**			V
	I_{OUT} = 100 μA	**2.4**			V
V_{OL}, Logic low	I_{OUT} = −2.0 mA			**0.4**	V
TRI-STATE® Leakages					
μP Bus	V = V_{DD}	**−10**			μA
	V = GNDD			**500**	μA
Data Bus	V = V_{DD}	**−10**			μA
	V = GNDD			**500**	μA
Input Currents					
All Non-TRI-STATE Inputs	0 < V_{IN} < V_{DD}	**−10**		**10**	μA
Pin Capacitances					
Inputs				10	pF
Outputs				15	pF
TRI-STATE Busses				15	pF
Power Dissipation	Temperature = 25°C V_{DD} = 5.0V Master Clock = 2 MHz No Outputs Loaded		250	**330**	mW

Note 1: Tested at 5.0V ±0V.

AC Electrical Characteristics

Unless otherwise noted, limits printed in **BOLD** characters are guaranteed for V_{DD} = +5V ±5%, V_{SS} = GNDD (digital ground), T_A = 0°C to +70°C by correlation with 100% electrical testing at T_A = +25°C. All other limits are assured by correlation with other production tests and/or product design and characterization.

Parameter	Conditions	Min	Typ	Max	Units
Clock Inputs					
Master Clock Frequency				**2.2**	MHz
Master Clock High		**185**			ns
Master Clock Low		**185**			ns
Frame Clock Frequency			8		kHz
Frame Clock Duty Cycle	(Note 2)				
Clock Rise/Fall Times				20	ns
Data Bus Timing	(*Figure 2*)				
t_{CD}, Clock Delay				**70**	ns
t_{EL}, Address Enable Low				**70**	ns
t_{EH}, Address Enable High				**70**	ns
t_{AV}, Address Output Valid				**150**	ns
t_{DV}, Data Output Valid				**330**	ns
t_{DF}, Data Bus Float		**20**		**80**	ns
t_{DS}, Data In Set-Up		**50**			ns
t_{DH}, Data In Hold		**20**			ns

Note 2: Frame clocks $\overline{F_O}$ and $\overline{F_I}$ are low during only one clock cycle of a transmit or receive frame, respectively. Each must go low shortly before the rising edge of the first clock cycle of a frame and return high shortly after the same clock edge, i.e., both edges of the frame clocks must be nominally aligned with falling edges of Master Clock.

AC Electrical Characteristics (Continued)

Unless otherwise noted, limits printed in **BOLD** characters are guaranteed for V_{DD} = +5V ±5%, V_{SS} = GNDD (digital ground), T_A = 0°C to +70°C by correlation with 100% electrical testing at T_A = +25°C. All other limits are assured by correlation with other production tests and/or product design and characterization.

Symbols	Parameter	Conditions	Min	Max	Units
t_{FL}	Serial Port Timing Frame Clock Low	(*Figure 2*)	**150**		ns
t_{FH}	Frame Clock High		**150**		ns
t_{PV}	Port Output Valid		80	**200**	ns
t_{PVH}	Port Output Hold		35		ns
t_{PS}	Port Input Set-Up		**65**		ns
t_{PH}	Port Input Hold		**30**		ns
t_{SL}	Output Strobe Low			**150**	ns
t_{SH}	Output Strobe High			**150**	ns
t_{CY}	Microprocessor Interface Timing Cycle Time	(*Figure 3*)	**1.0**		μs
t_{LL}	ALE Pulse Width		**125**		ns
t_{AS}	ALE to $\overline{DS}$ Output		**130**		ns
t_{CC}	$\overline{DS}$ Pulse Width		**300**		ns
t_{AL}	Address Set-Up to ALE		**70**		ns
t_{LA}	Address Hold from ALE		**50**		ns
t_{DW}	Data Set-Up to $\overline{DS}$		**250**		ns
t_{WD}	Data Hold from $\overline{DS}$		**15**		ns
t_{RD}	Data Out Delay			**270**	ns
t_{DR}	Data Out Hold			**85**	ns
t_{DL}	Data Ready Low			**500**	ns
t_{DD}	Data Ready Delay TP3110, TP3120 only	Any register Read/ Write operation except Interface Register in one-shot mode		**700**	ns
t_{DD}	Data Ready Delay TP3110, TP3120 only	Signaling Memory Read/Write operation		**700 + 6 x $T_{master\ clock}$**	ns
t_{DD}	Data Ready Delay TP3110, TP3120 only	Interface Register one-shot Read/ Write operation		Depends on the content of the Time-Slot Map (See Table II)	Depends on the content of the Time-Slot Map (See Table II)

Note 3: AC characteristics measured at V_{OH} = 2.0V and V_{OL} = 0.7V. Load conditions are:

(a) Data Bus, $\overline{PCM}$/CNTL, R/W Output, and Address Outputs — C_{LOAD} = 200 pF

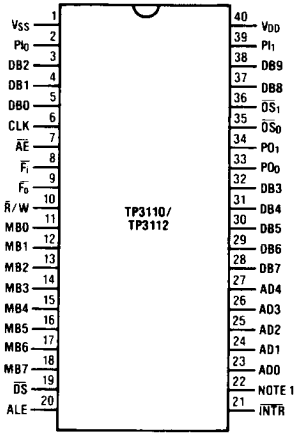
(b) Serial Output Ports, Output Strobes and AE Output — C_{LOAD} = 50 pF, R_{LOAD} = 2 kΩ to V_{DD}

(c) Microprocessor Bus TRI-STATE lines — C_{LOAD} = 150 pF

(d) Interrupt Request and Data Ready Outputs — C_{LOAD} = 80 pF

Connection Diagrams

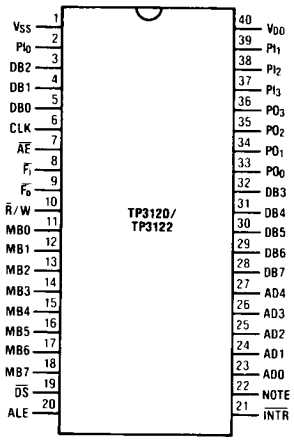
Dual-In-Line Package



TL/H/6699–2

Top View

Dual-In-Line Package



TL/H/6699–3

Top View

Note 1: Pin 22 = DR on TP3110, TP3120
Pin 22 = $\overline{PCM}$/CNTL on TP3112, TP3122

Pin Descriptions

SYSTEM INTERFACE PINS

Symbol	Description
CLK	Master Clock Input. This clock determines the serial port data rates and is also used to control the data flow over the line circuit Data Bus.
$PO_0 - PO_3$	Serial Port Outputs. These outputs are the main TDM transmission ports for the DLIC. The signal transmitted over these outputs must be inverted once before it is applied to a DLIC Serial Port Input ($PI_0 - PI_3$). PO_2 and PO_3 are available only on the TP3120 in lieu of $\overline{OS_0}$ and $\overline{OS_1}$.
$PI_0 - PI_3$	Serial Port Inputs. These inputs are the main TDM receive ports for the DLIC. PI_2 and PI_3 are available only on the TP3120 and TP3122 in lieu of DB8 and DB9.
$\overline{OS_0} - \overline{OS_1}$	Output Strobes. These active-low outputs indicate when PO_0 and PO_1 respectively are transmitting valid data. These outputs are not present on the TP3120, TP3122.
$\overline{F_o}$	Master Transmit Frame Sync. All Serial Port Output transmissions are synchronized by this signal.
$\overline{F_i}$	Master Receive Frame Sync. All Serial Port Input receptions are synchronized by this signal.
V_{DD}	5 V_{DC} power input pin.
V_{SS}	Digital Ground Power Input Pin (GNDD). All DLIC signal levels are referenced to the voltage level at this pin.

Pin Descriptions (Continued)

SUBSCRIBER CIRCUIT INTERFACE PINS

Symbol — **Description**

DB0-DB7 — Bidirectional eight-bit subscriber circuit interface bus. This bus normally handles the per line PCM COMBO data flowing to or from a TP3051/TP3056 parallel I/O COMBO circuit.

Data Type	DB0	DB7
PCM	Sign Bit	LSB
Control Data	C0	C7

DB8-DB9 — Additional Data Bus I/O pins for the 80 kHz channel option of the DLIC. These two functions are not available on the TP3120 (see PO_2, PO_3, PI_2 and PI_3). DB9 becomes the last bit of each time slot on each serial port.

AD0-AD4 — Subscriber circuit address output pins. These pins are used to select one of 32 different subscriber or special service circuits associated with the DLIC. AD4 is the MSB.

$\overline{AE}$ — An active low output that indicates a stable and valid subscriber circuit address on pins AD0 through AD4.

$\overline{R}$/W — Data Bus read/write select output and COMBO master clock. The $\overline{R}$/W output frequency is one-half of the main clock input frequency. A read operation on the DLIC Data Bus (reading an external device) occurs while this clock is low and the corresponding write operation occurs while it is high.

MICROPROCESSOR INTERFACE PINS

Symbol — **Description**

MB0-MB7 — A bidirectional interface bus used by a local processor to control all DLIC operations. Address, control and information data flow between DLIC and its associated microprocessor will pass over this bus. MB7 is the MSB.

ALE — Address Latch Enable input pin. It is used by the DLIC to determine when address data is crossing the MB0-MB7 Microprocessor Bus.

$\overline{DS}$ — Data Strobe input pin. A low true input signal pin to indicate when data is crossing the MB0-MB7 Microprocessor Bus.

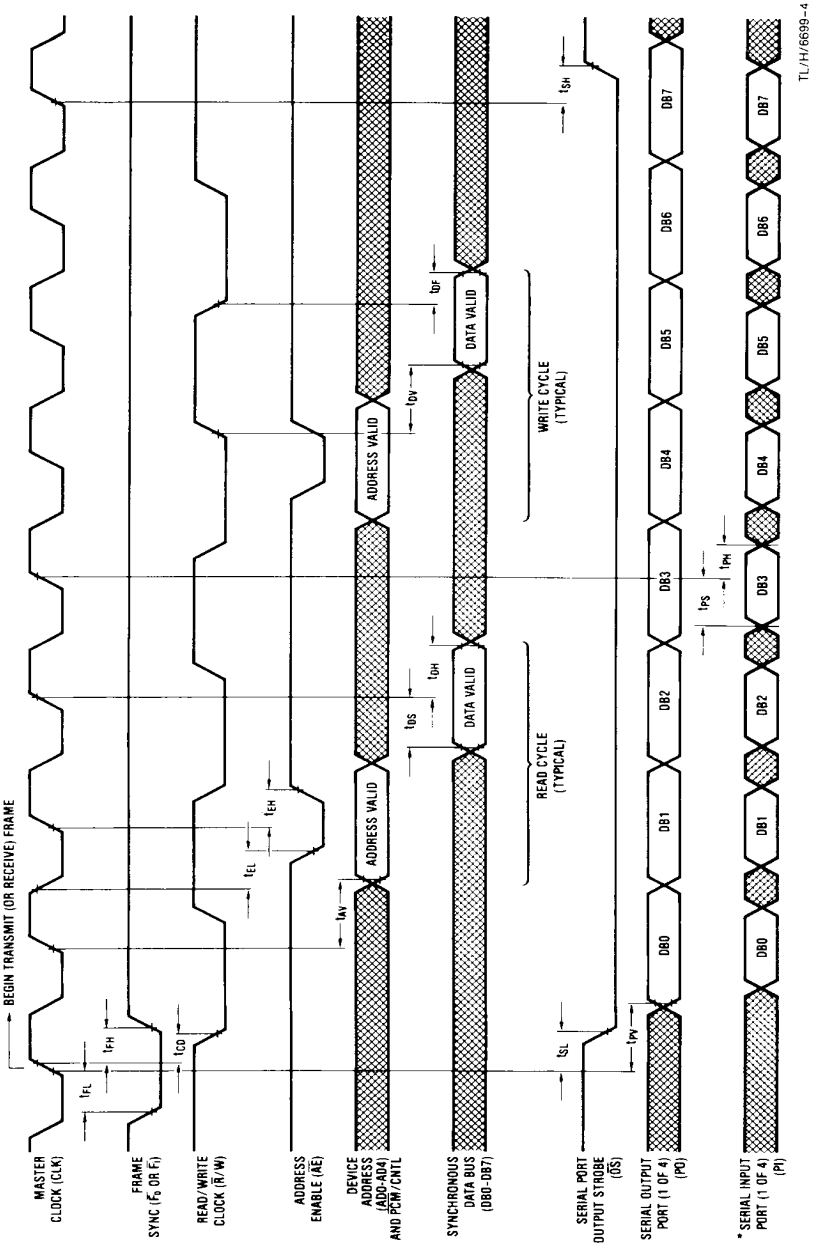
$\overline{INTR}$ — Interrupt control output pin. A low true output that indicates when a DLIC generated interrupt is active.

DR — Data Ready output pin. This signal goes low on the falling edge of $\overline{DS}$ when data is written to or read from the DLIC. It goes back high again (a) when the write operation has been executed inside the DLIC or (b) when the previously addressed data is available at the output of the DLIC.

The primary use of this signal is for Signaling Memory or Interface Register Read operations, since for these operations the addressed data may not be immediately available.

$\overline{PCM}$/CNTL — $\overline{PCM}$/control output pin. This signal is normally low and goes high during an interface instruction in NOP mode. Thus the $\overline{PCM}$/CNTL inputs of up to 32 TP3051 or TP3056 COMBO devices can be driven by this output, leaving all address outputs AD0-AD4 available for decoding 32 $\overline{CS}$ lines.

Timing Waveforms



*The input and output data bit coincidence is true only if $\overline{F_O}$ and $\overline{F_I}$ are phase synchronous.

FIGURE 2. Synchronous Data Bus and a Serial Port Transceiver Signal Flow

Timing Waveforms (Continued)

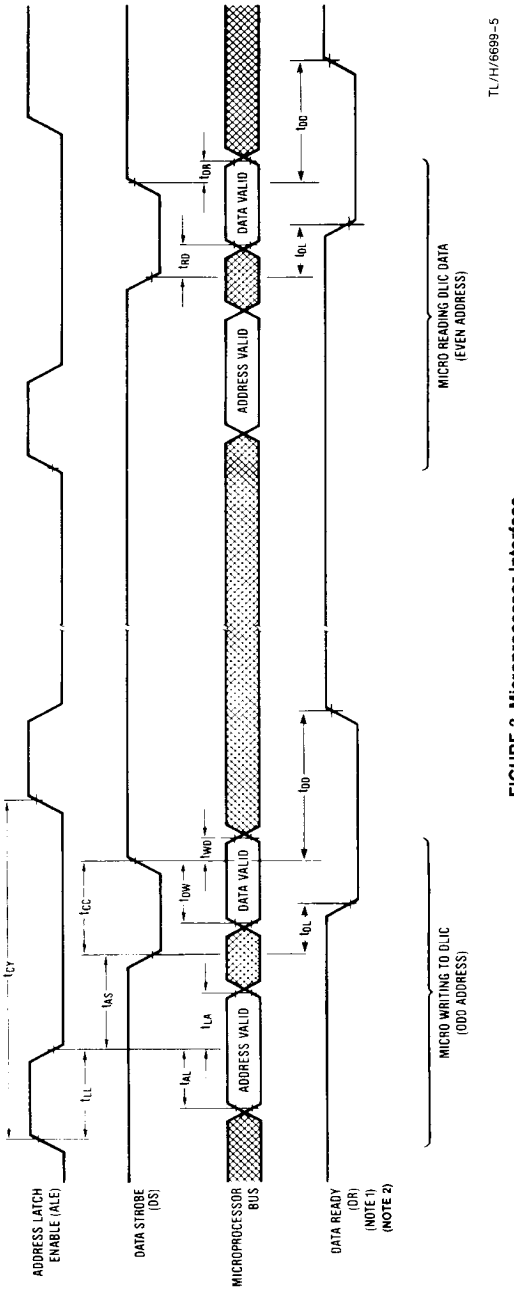


FIGURE 3. Microprocessor Interface

Note 1: TP3110, TP3120 only.

Note 2: For any Read or Write operation which is not related to the Interface Register or to the Signaling Memory, the state of line DR can be ignored by the Microprocessor.

Functional Description

Referring to *Figure 4*, the primary purpose of the DLIC is to control the flow of data between three I/O interfaces. These interfaces are the System Interface, COMBO (or other subscriber circuit) Interface and the Microprocessor Interface. Data that moves between the COMBO Interface and the System Interface is converted from an eight or ten-bit parallel format to a synchronous serial format. In addition, up to four bidirectional serial transmission interfaces are included in this first data movement group. Data that moves between the Microprocessor Interface and the System Interface is processed by Transmit and Receive High-level Data Link Control (HDLC) protocol controllers. This data is always in an eight-bit format with two "don't care" stuffing bits if necessary for ten-bit compatibility. The third and final type of data movement is between the COMBO Interface and the Microprocessor Interface ports. This movement allows interaction between the synchronous data flow of the COMBO to System Interface bus and the asynchronous flow of the Microprocessor Interface bus. A description of these data movements and their relation to the circuit blocks of *Figure 4* is the main purpose of this Functional Description.

The DLIC is available in four configurations. The TP3110 and TP3112 are arranged with a ten-bit wide COMBO interface and only two System Interface port circuits. These two port circuits include separate serial input and output highways and individual output strobes ($\overline{OS_0}$ and $\overline{OS_1}$) to indicate when the PO_0 and PO_1 signals are valid. The TP3120 and TP3122 DLIC eliminate two bits of the ten-bit COMBO Interface and the output strobes to provide a four-port System Interface. In this case, the serial output ports must be used with open-collector or open drain line drivers because the output strobes are not available for TRI-STATE output control. Otherwise, all aspects of these parts are identical.

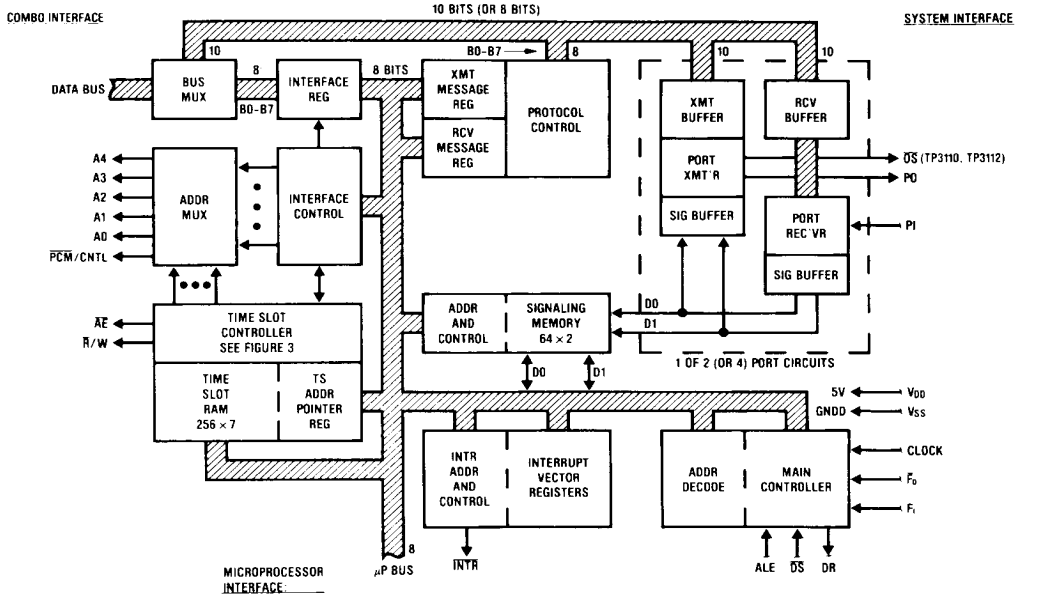
Summarizing,

Feature	TP3110, TP3112	TP3120, TP3122
■ ~~10-~~bit COMBO Interface bus	yes	no
■ Output strobes for PO_0 and PO_1	yes	no
■ I/O ports PI_2, PI_3 and PO_2, PO_3	no	yes

The DLIC is composed of seven major circuit blocks as listed below. The interaction between these circuit functions and the three interface ports will be described separately.

The DLIC circuit blocks are:

1. Time Slot Map
2. Serial Port Transceivers
3. HDLC Protocol Logic
4. Interface Register and Controller
5. Vectored Interrupt Control Logic
6. Signaling Memory
7. Main Controller



TL/H/6699–6

FIGURE 4. DLIC Block Diagram

Functional Description (Continued)

TIME SLOT MAP

The Time Slot Map and its associated circuitry control all of the synchronous data movements in the DLIC. The Map is organized as 256 seven-bit registers, each register directly corresponding to one clock cycle of the master input clock when in the eight-bit per channel format. For channels programmed to operate at ten bits per channel (as will be described later), the first eight clock cycles of each channel correspond to eight Map instructions and the last two cycles are skipped by the Time Slot Map. Each Map register can hold an instruction which will cause one of four basic operations. See Table VII for a listing of the Time Slot Map instruction set.

The data entered into the Map is arranged as a two-bit instruction code and a five-bit external device address code (i.e., COMBO, or SLIC select address). An eighth bit, not actually stored in the Map, is derived from an internal read/write clock that alternates data bus operations from read to write. This internal clock is exactly one-half the main clock frequency and it forces adjacent instructions from the Map to be read and write instructions.

Map addressing determines the actual time or space division switching function to be performed by the DLIC. As shown in *Figure 5,* the Map addresses are arranged so the LSB determines serial transmission direction. The next two bits are decoded as the system interface port transceiver address and the top five address bits select one of 32 time slots in the frame. By loading a Time Slot Map register, the position of the instruction within the Map will determine the channel, port and direction of the data flow over the System Interface, while the contents of the Map register will determine the source or destination of the data.

Time Slot Map instructions are executed sequentially and in complete synchronism with the master clock. The Map control logic, however, does allow the instruction sequence for transmit and receive operations to be skewed in time. Clock inputs $\overline{F_O}$ and $\overline{F_I}$ provide the DLIC Map with the timing relationship between the transmit and receive frames, respectively. This arrangement requires bit synchronization between the System Interface serial transmit and receive ports, but does not require frame or channel (time slot) synchronization.

To accommodate frames of less than 256 clock cycles, a maximum clock count register is loaded with a binary number for the maximum number of clock cycles per frame. This number is always a multiple of eight minus one (i.e., 7, 15, 31...255).

An associated microprocessor accesses the Time Slot Map through the DLIC Microprocessor Interface port. The access is a two step process to allow the synchronization of data that must be written to or read from the Map. First, the microprocessor must write a Map address into the Address Pointer Register (address 01 hex), see Table I. Next, the microprocessor can execute a Map read (address 40 hex) or write (address 41 hex) command to move data to or from the Map. A read command must be executed a minimum of 125 μs after an address load to allow the desired Map data to be "down-loaded" into the access holding register. A write command can be executed immediately after an address load, but further Map read or write operations must be suspended for at least 125 μs or one frame period. This pause allows the written data to be loaded into the proper Map location during the next complete Map scan. To facilitate a Map reset operation, the Address Pointer Register will automatically increment to the next address count at the end of each Map write command cycle (again, address 41 hex). This feature allows the microprocessor to write 256 NOP instructions into the Map, one instruction load per frame period, using only a single microprocessor write operation per cycle.

SERIAL PORT TRANSCEIVERS

Two or four serial port transceivers are provided for the DLIC System Interface. Under control of the Time Slot Map, data is either parallel loaded for serial transmission or parallel read after serial reception. The exact timing for all operations is dependent upon the instructions in the Map and the beginning of each TDM channel relative to the start of the

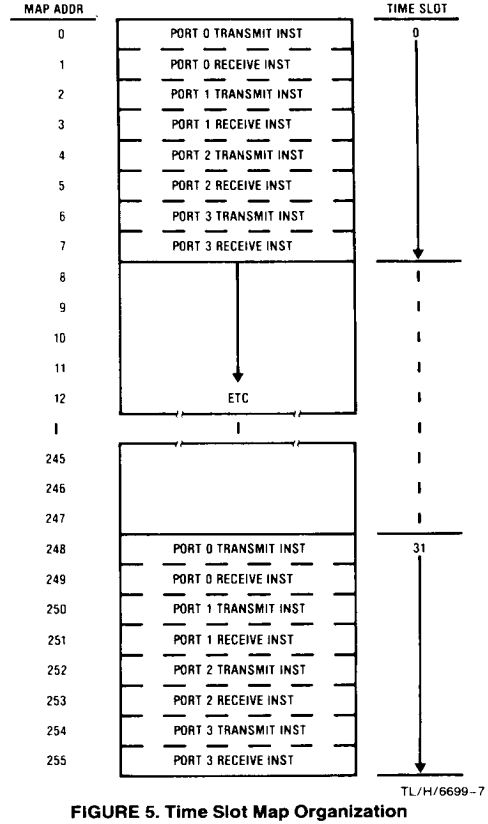


FIGURE 5. Time Slot Map Organization

Functional Description (Continued)

frame. While all serial exchanges begin and end in alignment with the TDM channels, parallel exchanges are only synchronized to master clock cycles. Incidentally, for normal DLIC operation a channel is eight clock cycles long and the first channel begins with the positive master clock edge while the appropriate frame clock is low.

The idle state for any Serial Output Port is logic low. This signal must be externally inverted to logic high before it can be applied to a Serial Input Port on any DLIC. The inverted signal corresponds to the idle channel code of a PCM COMBO and the idle or abort sequence of the HDLC protocol. The normal hardware arrangement would use an inverting bus driver between the DLIC Serial Output Ports and the system backplane highways, and no inverter between the backplane and the DLIC Serial Input Ports.

In the ten-bit operating mode, the beginning of channel one is still the rising clock edge while the appropriate frame clock is low. The length of each channel, however, is ten bits or clock cycles and for a full 32-channel frame, 320 clock cycles are required. The transceivers will serially shift the extra two bits per channel after the normal eight-bit sequence is complete.

Transmission order for the serial System Interface is always LSB first, for data and sign bit first for PCM. This is compatible with the normal protocol of PCM transmission. The ordering of the data from the parallel interface of the TP3051 or TP3056 PCM COMBOs is thus reversed from the normal arrangement, and is shown below:

Serial Transmission Order	Data Bus Order
First bit in or out	DB0
Second bit	DB1
Third bit	DB2
Fourth bit	DB3
Fifth bit	DB4
Sixth bit	DB5
Seventh bit	DB6
Eighth bit	DB7
Ninth bit (10-bit mode only)	DB8
Tenth bit (10-bit mode only)	DB9

Whenever the ninth and tenth serial bits are delivered to or from the signaling memory circuit block (a programmable option), the ninth bit internally passes through the DLIC as bit D0 while the tenth bit passes as D1 (*Figure 4*). Over the Microprocessor Interface bus, these bits correspond to MB0 and MB1 respectively.

PROTOCOL LOGIC

System control messages are transmitted between the main processor and the DLIC local processor by way of System Interface TDM channels. This data passes through the DLIC under direct control of the Time Slot Map. Because the integrity of this control information is very important to the total system operation, the DLIC includes High-level Data Link Control (HDLC) protocol circuits to process these control messages. These are independent Transmit and Receive HDLC circuits that allow simultaneous both-way control messages if required.

The HDLC format used in the DLIC follows the CCITT X.25, Section 2.1 and 2.2 recommendation. This recommendation calls for an opening flag sequence of 01111110 followed by the device address, control, data, checksum and closing flag fields. The closing flag of one message can be used as the opening flag to the next message. To avoid the unintentional simulation of a flag sequence, the DLIC will insert a zero after any string of five ones except where a flag or abort code is desired. Again, this is in conformance with the CCITT recommendation.

Before starting a transmit message the microprocessor must first load the DLIC Address Register with the unique address for that subscriber line card; write the Time Slot(s) for the message channel in the Time Slot Map; and enable the necessary interrupts (see Table V). Then the first data byte must be loaded in the Transmit Message Register. The message channel is activated by setting Control Register bit 5 high (see Table III). An opening flag is transmitted in the selected channel, then the DLIC address and then the first data byte, with zeroes inserted according to the HDLC protocol. Each time the Transmit Message Register is emptied, the DLIC automatically generates a "register empty" interrupt to force the microprocessor into loading the next data byte of the message. If the microprocessor responds to this interrupt by turning the HDLC transmit logic off, the DLIC will close out the current message with the CRC checksum and a closing flag. Failure to service this interrupt before the next message Time Slot arrives will result in the abort sequence of all 1's being transmitted.

For receive messages the microprocessor must first load the associated DLIC registers as described for the transmit section. The DLIC monitors the message channel until an opening flag is detected, then compares the address field with the contents of the DLIC Address Register. If there is a match, or if the address field contains the broadcast address, Hex FF, the message is accepted. (Inserted zeroes are automatically deleted.) As each message data byte is received it is stored in the Receive Message register and an interrupt generated to summon the microprocessor. When the register is read, the interrupt signal is reset to await the next data byte. If the interrupt is not serviced before the next data byte arrives, or if an abort sequence is received, the receive CRC checksum will be corrupted to indicate that the message is not valid. The receive protocol logic automatically computes the CRC checksum on the incoming message and compares it with the CRC field (which is not known until the closing flag is detected) to determine the final interrupt for this message, i.e., Checksum Correct or Checksum Incorrect.

It should be noted that the DLIC can receive only a single control message at a time (i.e., the receive message channel must be one channel of one serial highway). It can, however, transmit a control message over one, two, three or four ports simultaneously, although the same channel must be used for each of the ports. This is a useful feature that simplifies overall system design.

MASTER MODE

This mode allows the DLIC to be used as the master controller for a group of line cards connected to a common backplane. It forces the receive protocol logic to ignore the contents of the address field on an incoming message so that it will accept a message from any source. Internally the address comparison is inhibited and the address byte is

Functional Description (Continued)

forwarded to the microprocessor in the same manner as a data byte.

The transmit HDLC logic operation is not changed in this mode. Before transmitting a new message the microprocessor must load the DLIC Address Register with the destination address. Alternatively, a message can be "broadcasted" to all DLIC's in a control group by setting the address field to hex FF. Master Mode is selected by setting Control Register bit 4 high.

INTERFACE REGISTER AND CONTROLLER

This circuit block provides a direct data access path between the DLIC associated microprocessor and any of the circuit devices connected to the COMBO Interface bus. This allows the two internal data busses, which are operating in asynchronism with each other, to communicate control and signaling information through the DLIC. This need for additional access ports on the per channel circuits is eliminated with this communications scheme.

The Interface Register operates in one of two control modes and handles the flow of data in only one direction at a time. Data written into the register from the Microprocessor Interface bus can be moved onto the COMBO Interface bus during either the next available Time Slot Map NOP (direct mode) or when a particular Map instruction is executed (frame mode). In a similar fashion, data can be moved in from the COMBO Interface bus to be written onto the Microprocessor Interface bus in either the direct or frame mode fashion. Control of the Interface Register is handled by matching instructions in the Time Slot Map and Interface Register Controller. See Table II for additional details.

Control data is written to DLIC address 03 hex. The microprocessor can read the Interface Register with hex address 42 and it can write to the Register with hex address 43. Reading the Register from either the Microprocessor or COMBO Interface busses does not alter its contents. Any operation which takes place during a Time Slot Map NOP will occur only once. The Register Controller will reset to a NOP control condition after the "one-shot" execution. The data READY output (TP3120 and TP3110) indicates the pending nature of this control cycle by remaining low from the time the instruction is loaded until execution is complete. On the TP3122 and TP3112 only, the $\overline{\text{PCM}}$/CNTL output goes high when a "one-shot" control instruction is being executed. Operations which occur as the result of a match between a Time Slot Map instruction and the control byte loaded into the Interface Register Controller will occur every frame and must be halted by direct command from the microprocessor. This latter operating mode is interrupt driven and is useful in generating PCM test signals with the local microprocessor.

INTERRUPT LOGIC

The DLIC contains an on-board Vectored Interrupt Controller. This Controller will process the seven built-in interrupts of the DLIC. In addition, these interrupts are prioritized so that important operations are never missed. See Table V for more information.

The DLIC microprocessor can directly read or write the seven DLIC interrupt registers. This allows a specific program address to be loaded into the DLIC interrupt control logic so that the occurrence of the interrupt can cause a program vector to be read from the DLIC by the microprocessor. The DLIC read address for a pending interrupt is 00 hex. The information read with the 00 address is then directly used by the microprocessor to compute an address jump to the appropriate software routine to service this interrupt. The address 00 read operation will automatically reset and clear the interrupt request and its output signal on the $\overline{\text{INTR}}$ line.

Interrupts that require simultaneous service are handled in the priority order given in Table V. Additional features of this logic section include a single DLIC Command Register control bit to activate and deactivate the interrupt logic output signal and a control register within the interrupt logic block for selective masking of individual interrupts. It should be noted that turning all interrupts off with the single control bit does not disable the generation of the interrupts inside the DLIC. When the control bit reactivates the interrupt output line, any interrupts that have occurred during the idle state will immediately request service in the proper priority order. However, masking an interrupt off by storing a zero in the proper place within the interrupt control register (address 3F hex) will totally disable the interrupt. Internal circuitry will not recognize the activity that normally causes the interrupt request and the interrupt, when enabled, starts from a reset condition.

SIGNALING MEMORY

This memory block operates as either a buffer store for the two bits of the ten-bit 80 kHz channel or as a general purpose RAM. DLIC control bit D3 of Table III will determine the operating state. In either state, the Signaling Memory is arranged as 64 two-bit cells that interface the microprocessor bus through the two least significant bits MB0 and MB1. Internal to the DLIC, these two bits are called D0 and D1.

When the Signaling Memory is used for general storage, the DLIC control bit D3 is set to zero. Each two-bit cell of the memory is accessed with one of 64 read or write addresses as shown in Table VIII. The interface between the Signaling Memory function and the System Interface transceivers is totally disabled while in this operating state.

While using the Signaling Memory RAM for general storage, the extra two bits of the ten-bit serial channel System Interface format can only be accessed through the DB8 and DB9 lines of the COMBO Interface bus. This means that only the TP3110 and TP3112 can simultaneously operate with ten-bit serial channels and the Signaling Memory in the general storage operating state.

When DLIC control bit D3 is high, the Signaling Memory RAM is switched to an operational state known as Extended Channel Signaling (ECS). In this operating mode, the data for bits 9 and 10 of a ten-bit serial channel are buffered by the Signaling Memory. This data is not accessible through the COMBO Interface bus pins DB8 and DB9 when ECS is enabled. The extra two bits of data are accessible only through the 32 transmit and 32 receive cells in the Signaling Memory RAM. Each of the cells corresponds to an address of the COMBO Interface bus. This allows any device connected to this bus to utilize the Signaling Memory RAM, loaded and unloaded through the DLIC microprocessor, for end-to-end system data communications at speeds of up to 16 kHz.

Functional Description (Continued)

MAIN CONTROLLER

While most of the DLIC features and functions are controlled by the various circuit blocks already described, some master control functions still remain to be explained. These include the setting of overall frame timing and length, power on reset conditions, and the initialization of Time Slot Map, Signaling Memory and HDLC protocol control power-up states. Also available through the DLIC main control are status flags for the HDLC protocol logic and the interface register.

Because of the pipelined architecture of the DLIC, the Time Slot Map is actually operated in a "look ahead" fashion. This structure requires a maximum TDM frame length register on the DLIC. It is microprocessor loaded during initialization and it provides the DLIC with address counter "wrap" information during less than full length TDM frames.

The DLIC maximum count is determined on a eight-bit per channel basis. If the DLIC is set for ten-bit operation, the maximum count is still related to eight bits per channel. This is because the Time Slot Map will skip two clock cycles out of every ten during this latter operating mode. The maximum count register is set to the number of channels in a frame (on one of the highways) times eight. As an example, a 24-channel system would require a maximum count frame length of 192 (24 x 8) and the DLIC maximum count register would be set to hex BF which corresponds to the decimal 192 clock cycles per frame.

TABLE I. Microprocessor Interface

Hex Address	Description of Interface Data Flow
0 0	Microprocessor READ of current interrupt vector after detecting a logic low condition on DLIC output $\overline{INTR}$.
0 1	Microprocessor WRITE cycle to the address pointer register of the Time Slot Map controller.
0 2	Not used.
0 3	Microprocessor WRITE cycle to the control logic of the Interface Register. See Table II.
0 4	Not used.
0 5	The WRITE cycle used by the microprocessor to load the DLIC Address Register.
0 6	Not used.
0 7	The WRITE cycle used by the microprocessor to set the maximum number of clock cycles per frame.
0 8	Microprocessor READ of current DLIC status conditions.
0 9	Microprocessor WRITE cycle to set the DLIC Control Register. For addresses 08 and 09, see Table III.
0 A ↓ 1 F	Not used.
2 0 ↓ 3 F	READ and WRITE operations to the Interrupt Vector Registers of the DLIC. See Table V.
4 0	A microprocessor READ cycle of Time Slot Map data. The Map address must be preset using hex address 01.
4 1	The complementary WRITE operation for hex address 40. See Table VII.
4 2	The microprocessor READ cycle of the Interface Register. Control conditions must be preset with hex address 03.
4 3	The complementary WRITE operation for hex address 42. Control conditions are normally set after this WRITE cycle.
4 4 ↓ 4 F	Not used.
5 0	A microprocessor READ operation to retrieve data from the Receive Message Register after the appropriate interrupt has been received.
5 1	A microprocessor WRITE operation to the Transmit Message Register. Again, the appropriate interrupt will normally initiate this microprocessor operation.
5 2 ↓ 7 F	Not used.
8 0 ↓ F F	Microprocessor access to the DLIC Signaling Memory. Even addresses correspond to READ cycles for the 64 two-bit memory cells while odd addresses correspond to complementary WRITE cycles. See Table VIII.

Functional Description (Continued)

POWER-UP INITIALIZATION

During power-up initialization, the DLIC will automatically clear its control register. This action will disable the Time Slot Map and System Interface output ports, set the $\overline{INTR}$ output high, deactivate the HDLC transmit protocol logic and place the DLIC in the eight-bit per channel operating mode. No other reset functions will occur. As described earlier, the DLIC associated microprocessor is responsible for clearing the Time Slot Map, setting the interrupt vectors, loading the DLIC Address Register, and in general, establishing all of the DLIC control and operating states. Through the Control Register, the microprocessor can quickly activate and deactivate the major functions of the DLIC with a single write operation to hex address 09.

TABLE II. Interface Register Control

Data Byte								Description of Interface Register Control Operation
D7	D6	D5	D4	D3	D2	D1	D0	
0	0						0	A control instruction to move data from an external device into the DLIC Interface Register during the next Time Slot Map NOP while the $\overline{R}$/W line is low. This cycle will automatically reset to a no operate state after execution.
0	0						1	The complementary operation to the above with the data movement from the preloaded Interface Register into an external device. Again, this is a one-shot operation.
0	1			↑ Address field for devices connected to the data bus ↓			0	A control instruction to move data from an external device into the DLIC Interface Register whenever this control byte matches a Time Slot Map instruction byte. This instruction remains in effect until manually cleared by the microprocessor.
0	1						1	The complementary operation to the above with the data movement from the Interface Register into an external device any time this control byte matches a Time Slot Map instruction byte.
1	0			Don't care			0	Reserved.
1	0						1	Reserved.
1	1			Don't care ↓			0	No operation.
1	1						1	No operation.

TABLE III. DLIC Status and Control Data

Data Bit	DLIC Status Register READ Cycle; Address 08	DLIC Control Register WRITE Cycle; Address 09
D0	Transmit Message Register empty.	Enable Time Slot Map controller.
D1	Receive Message Register full.	Enable $\overline{INTR}$ (interrupt) request output.
D2	An Interface Register command is in effect.	Enable the 10-bit/channel operating mode.
D3	HDLC opening receive flag detected.	Enable Signaling Memory for Extended Channel Signaling.
D4	CRC error detected on incoming message.	Enable Master Mode.
D5	HDLC receive logic in idle state.	Enable HDLC Transmit Message Logic.
D6	HDLC transmit logic in the active state.	Not used.
D7	HDLC transmit channel in the idle state.	Should always be zero.

Functional Description (Continued)

TABLE IV. DLIC Control States

Function	Control Register D7	D3	D2	TP3110, 3112 Option	TP3120, 3122 Option	Description
Normal	0	0	0	yes	yes	Up to 32 eight-bit channels per frame on each serial highway. No other options.
Ten-Bit	0	0	1	yes	no	32 ten-bit channels/frame with bits 9 and 10 accessed through 10-bit data bus.
ECS	0	1	1	yes	yes	32 ten-bit channels/frame with bits 9 and 10 accessed through the Signaling Memory.

TABLE V. Interrupt Vector Registers

Hex Address	Priorty Level	Description of Register READ and WRITE Operations
2 0 2 1	5	Direct READ of vector register for Interface Register instruction executed interrupt. WRITE operation for the same interrupt register.
2 2 2 3	4	Direct READ of vector register for Transmit Message Register empty interrupt. WRITE operation for the same interrupt register.
2 4 2 5	1	Direct READ of vector register for Receive Message Register full interrupt. WRITE operation for the same interrupt register.
2 6 2 7	2	Direct READ of vector register for Receive Message Checksum Correct interrupt. WRITE operation for the same interrupt register.
2 8 2 9	3	Direct READ of vector register for Receive Message Checksum Incorrect interrupt. WRITE operation for the same interrupt register.
2 A 2 B	6	Direct READ of vector register for End of Transmit Frame interrupt. WRITE operation for the same interrupt register.
2 C 2 D	7	Direct READ of vector register for End of Receive Frame interrupt. WRITE operation for the same interrupt register.
2 E ↓ 3 D	X	Not used.
3 E 3 F	X	READ operation for Interrupt Masking Register. WRITE operation for Interrupt Masking Register. (See Table VI for details).

Note: Interrupt priority levels are associated with the service order if simultaneous interrupts request attention via the microprocessor 00 hex address READ cycle. All interrupts automatically reset only after the appropriate vector is read through this same 00 hex address.

TABLE VI. Interrupt Masking

Data Bit	Description of Masking Control with Interrupt Mask Register
D0	If high, Receive Message Register full interrupt is on.
D1	If high, Receive Message Checksum Correct interrupt is on.
D2	If high, Receive Message Checksum Incorrect interrupt is on.
D3	If high, Transmit Message Register empty interrupt is on.
D4	If high, Interface Register instruction executed interrupt is on.
D5	If high, End of Transmit Frame interrupt is on.
D6	If high, End of Receive Frame interrupt is on.
D7	Not used.

Functional Description (Continued)

TABLE VII. Time Slot Map Instructions

Data Byte D7	D6	D5	D4	D3	D2	D1	D0	Description of Time Slot Map Instruction Code
0	0	↑ Address field for devices connected to the data bus ↓					0	Move data from an external device (e.g., parallel COMBO) to a serial port transmitter. The Map address identifies the proper transmitter.
0	0						1	Move data from a serial port receiver to an external device. The Map address identifies the proper receiver.
0	1						0	Move data from an external device to the Interface Register whenever a match occurs between this data byte and the contents of the Interface Register Controller.
0	1						1	Move data from the Interface Register to an external device whenever a match occurs between this data byte and the contents of the Interface Register Controller.
1	0	↑ Don't care (Note 1) ↓					0	Move data from the Transmit Message Register, through the protocol logic section to a serial port transmitter. The Map address identifies the proper transmitter.
1	0						1	Move data from a serial port receiver, through the protocol logic section to the Receive Message Register. The Map address identifies the proper receiver.
1	1						0	No operation.
1	1						1	No operation.

Note 1: To minimize bus and system noise it is recommended that this field be set to all '1's.

TABLE VIII. Signaling Memory Addressing

Hex Address	Description of Memory Access with ECS Disabled	Description of Memory Access with ECS Enabled
8 0	READ bits D0 and D1 of cell number 0.	READ signaling data received for external device 0.
8 1	WRITE bits D0 and D1 of cell number 0.	Not used.
8 2	READ bits D0 and D1 of cell number 1.	READ signaling data received for external device 1.
8 3	WRITE bits D0 and D1 of cell number 1.	Not used.
•	•	•
•	•	•
•	•	•
B E	READ bits D0 and D1 of cell number 31.	READ signaling data received for external device 31.
B F	WRITE bits D0 and D1 of cell number 31.	Not used.
C 0	READ bits D0 and D1 of cell number 32.	Not used.
C 1	WRITE bits D0 and D1 of cell number 32.	WRITE into memory, external device 0 transmit signal data.
C 2	READ bits D0 and D1 of cell number 33.	Not used.
C 3	WRITE bits D0 and D1 of cell number 33.	WRITE into memory, external device 1 transmit signal data.
•	•	•
•	•	•
•	•	•
F E	READ bits D0 and D1 of cell number 63.	Not used.
F F	WRITE bits D0 ad D1 of cell number 63.	WRITE into memory, external device 31 transmit signal data.

Typical Application

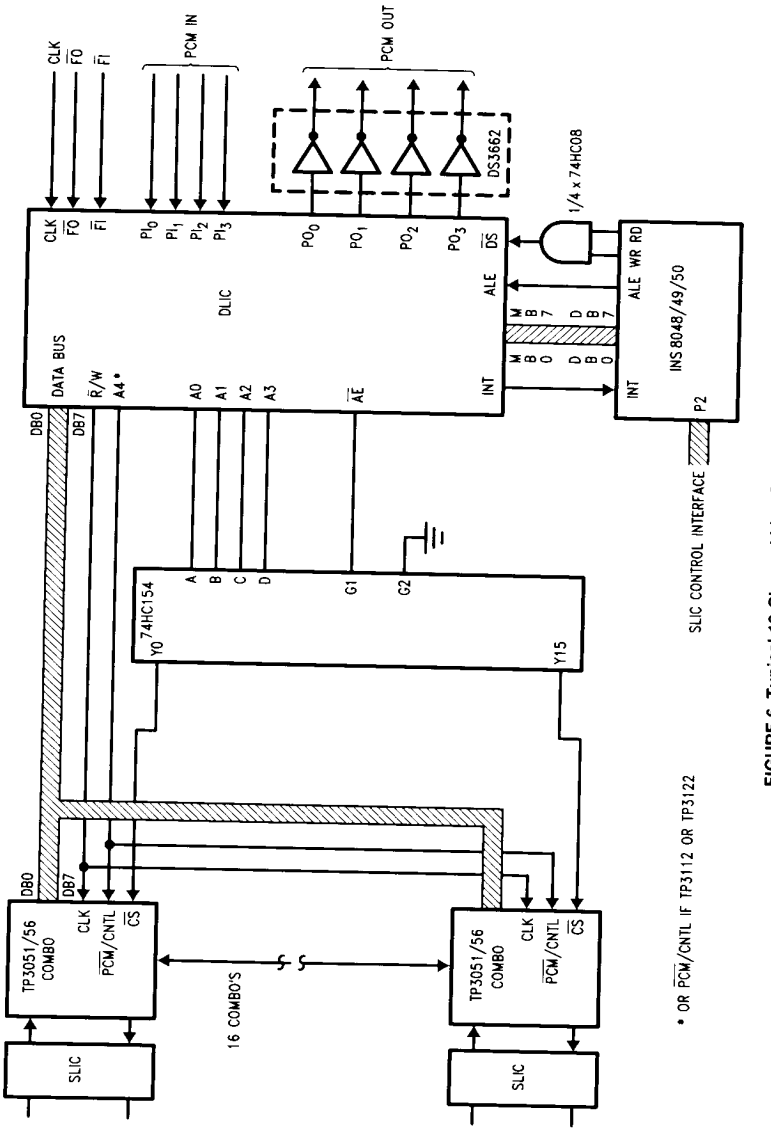
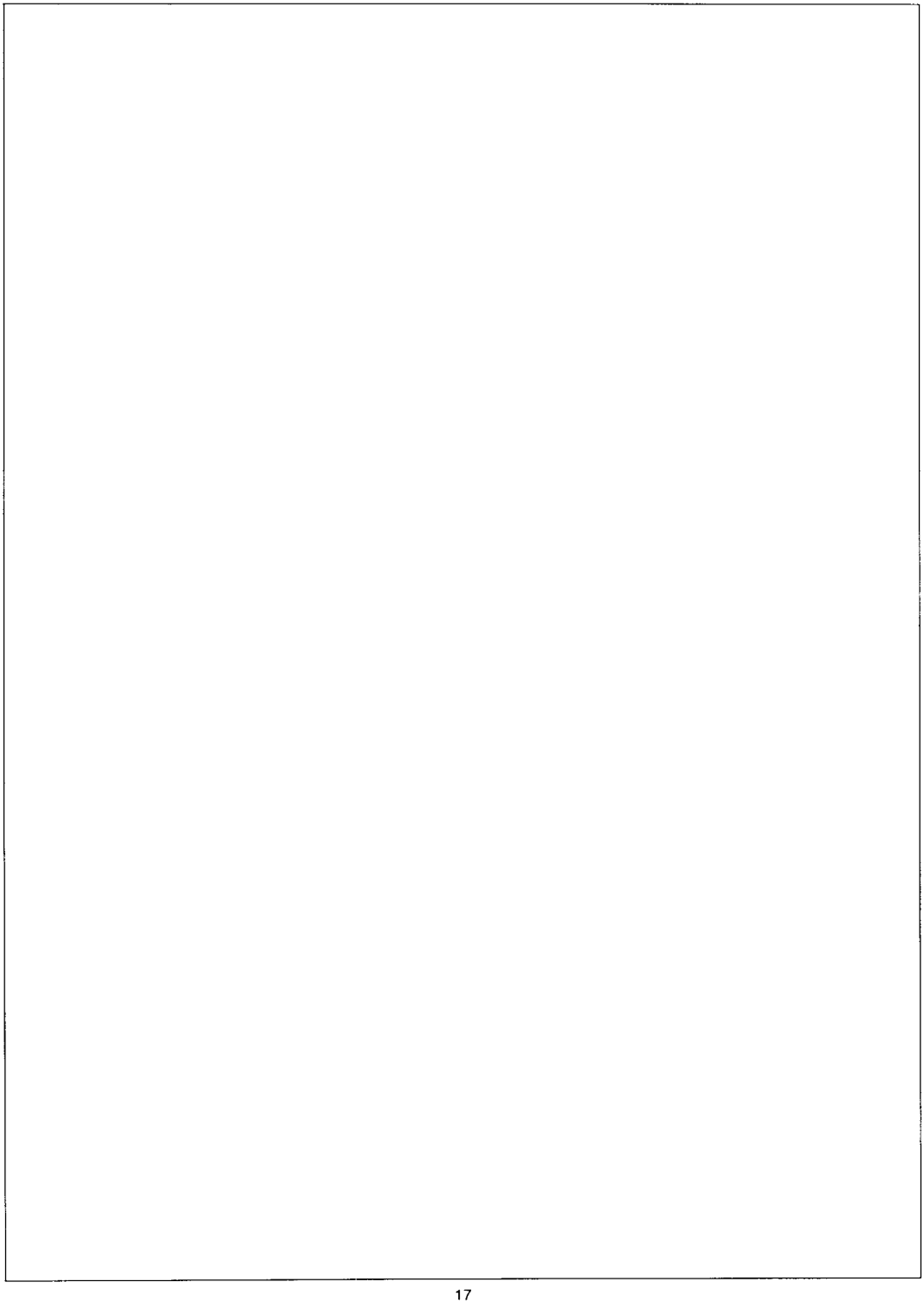
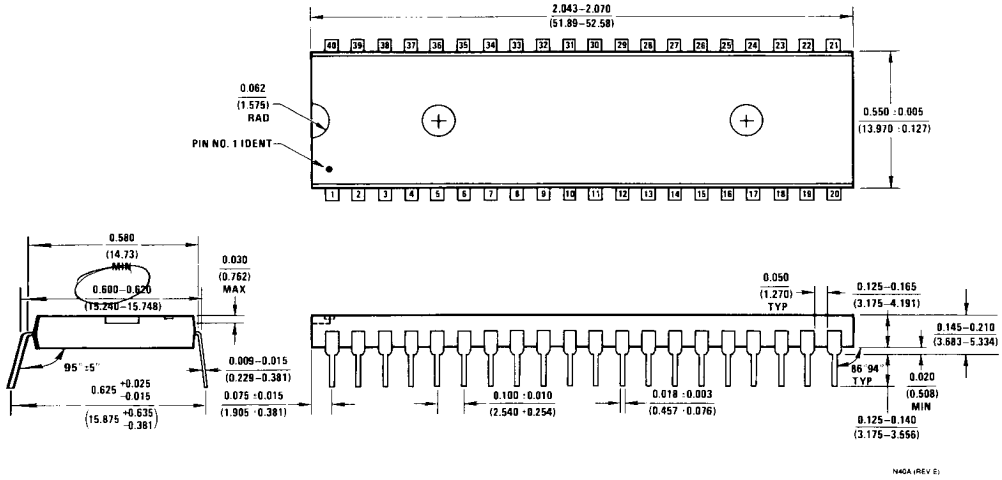


FIGURE 6. Typical 16-Channel Line Card Application



Physical Dimensions inches (millimeters)

Lit. # 113980



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Order Number TP3120J or TP3122J or TP3110J or TP3112J
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