Multi-Channel Power Management IC for Portable Device

General Description

The RT9912A is a multi-channel power management IC providing power conversion and system power management functions for one or two alkaline battery powered portable handheld device.

The RT9912A integrates one high efficiency synchronous buck regulator, one high efficiency boost regulator, one linear regulator and one adjustable voltage detector for reset function.

Ordering Information

RT9912A □□

- Package Type
  QW : WQFN-24L 4x4 (W-Type)
- Lead Plating System
  G : Green (Halogen Free and Pb Free)

Note :

Richtek products are :

- RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- Suitable for use in SnPb or Pb-free soldering processes.

Marking Information

For marking information, contact our sales representative directly or through a Richtek distributor located in your area.

Features

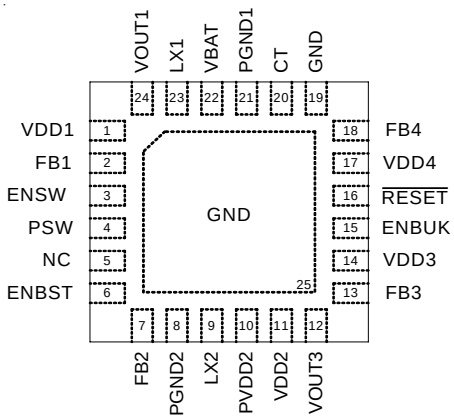
- **300mA Sync. Step Down Converter for V_{CORE}**
- **300mA Sync. Step Up Converter for IO and Memory**
- **High Efficiency Up to 92%**
- **Low Dropout Linear Regulator**
- **Adjustable Voltage Detector for Reset Function**
- **Current Limit Protection**
- **Thermal Shutdown Protection**
- **Low Operation Current Consumption**
- **Small 24-Lead WQFN Package**
- **RoHS Compliant and Halogen Free**

Applications

- DSC
- Portable Multimedia Player
- GPS

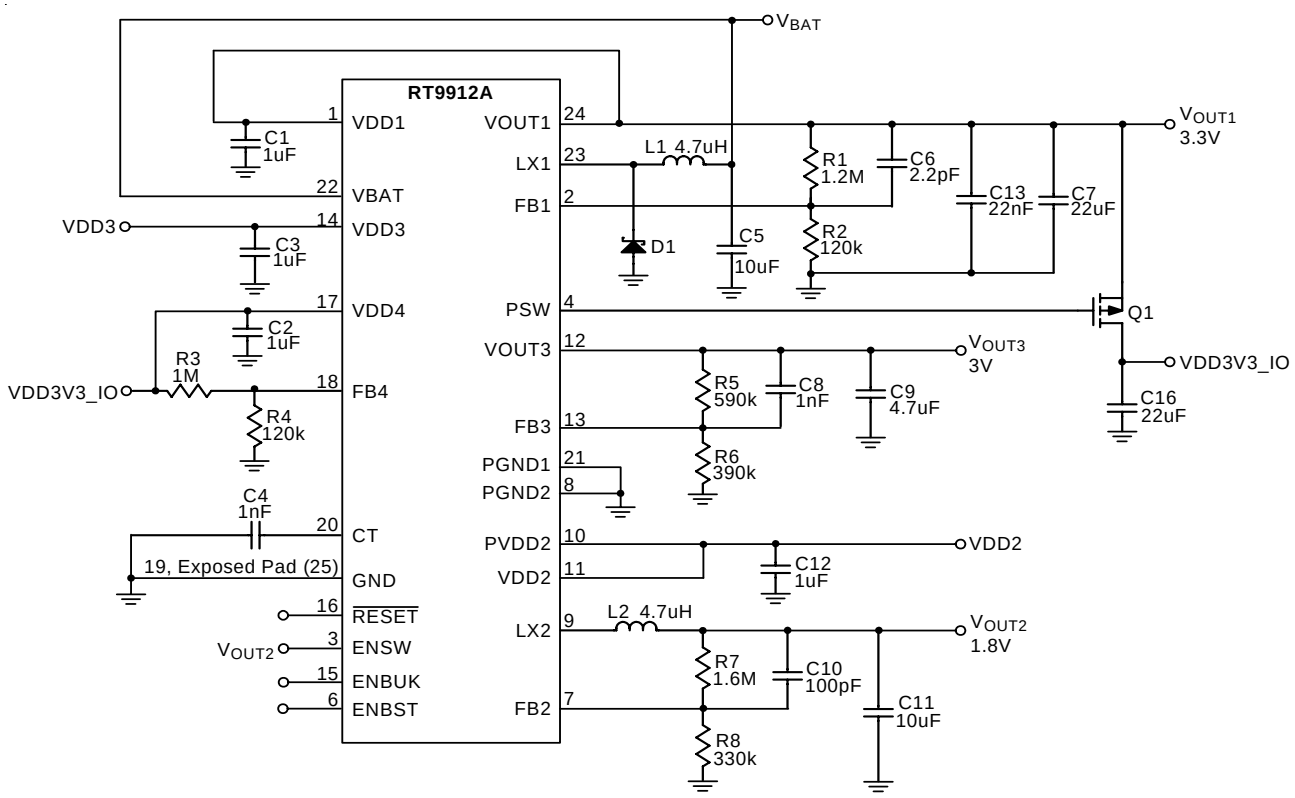
Pin Configurations

(TOP VIEW)

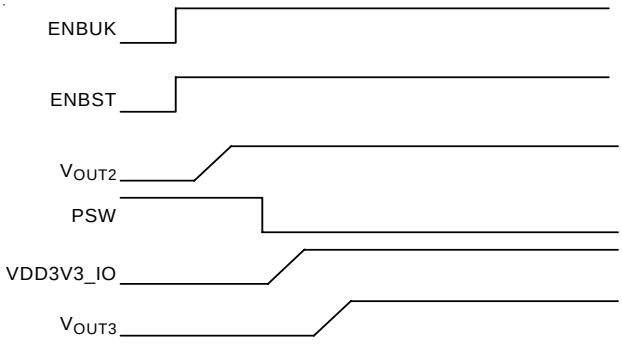


WQFN-24L 4x4

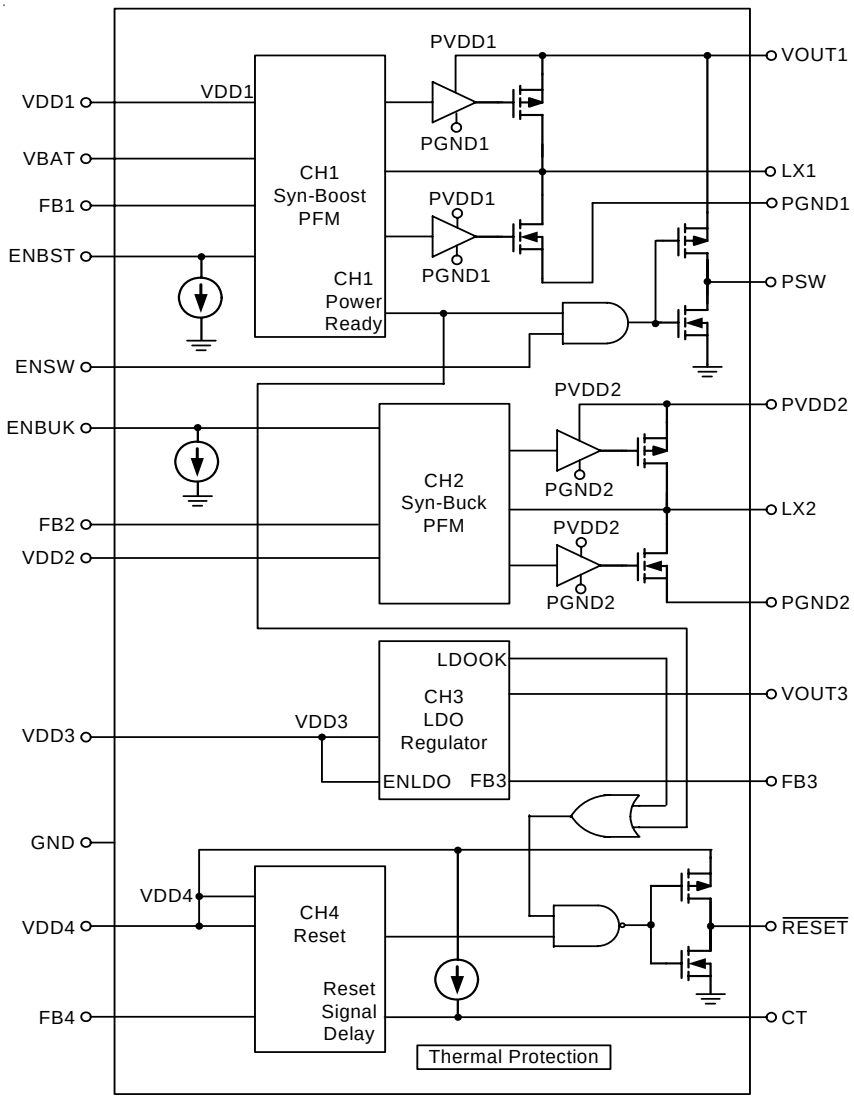
Typical Application Circuit



Power ON Sequence : V_{OUT2} → VDD3V3_IO → V_{OUT3}



Function Block Diagram



Functional Pin Description

Pin No.	Pin Name	Pin Function
1	VDD1	CH1 Power Input Pin.
2	FB1	CH1 Feedback Input Pin.
3	ENSW	Load Disconnect Enable Pin.
4	PSW	Load Disconnect P-MOSFET Gate Drive Pin.
5	NC	No Internal Connection. This pin must be floating.
6	ENBST	Boost Enable Pin.
7	FB2	CH2 Feedback Input.
8	PGND2	Power Ground for CH2.
9	LX2	CH2 Switch Node.
10	PVDD2	CH2 Power Input Pin.
11	VDD2	CH2 Power Input Pin for Analog.
12	VOUT3	CH3 Output Voltage.
13	FB3	CH3 Feedback Input.
14	VDD3	CH3 Power Input Pin.
15	ENBUK	BUCK Enable Pin.
16	RESET	Reset Pulse Output, Negative Pulse.
17	VDD4	CH4 Power Input Pin.
18	FB4	CH4 Feedback Input.
19, Exposed Pad (25)	GND	Analog Ground. The exposed pad must be soldered to a large PCB and connected to GND for maximum power dissipation.
20	CT	External Delay Adjust Pin.
21	PGND1	Power Ground for CH1.
22	VBAT	Battery Power Input Pin.
23	LX1	CH1 Switch Node.
24	VOUT1	CH1 Output Voltage.

Absolute Maximum Ratings (Note 1)

- Supply Voltage, V_{DD1}, V_{DD2}, V_{DD3}, V_{DD4}, PV_{DD2} ---------- –0.3V to 6.5V
- LX1 and LX2 Pin Switch Voltage ---------- –0.3V to 6.5V
- Other I/O Pin Voltage ---------- –0.3V to 6.5V
- Power Dissipation, P_D @ T_A = 25°C
  WQFN-24L 4x4 ---------- 1.852W
- Package Thermal Resistance (Note 2)
  WQFN-24L 4x4, θ_{JA} ---------- 54°C/W
  WQFN-24L 4x4, θ_{JC} ---------- 7°C/W
- Junction Temperature ---------- 150°C
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Storage Temperature Range ---------- –65°C to 150°C
- ESD Susceptibility (Note 3)
  HBM (Human Body Mode) ---------- 2kV
  MM (Machine Mode) ---------- 200V

Recommended Operating Conditions (Note 4)

- Supply Input Voltage, V_{BAT} ---------- 1.7V to 5V
- Junction Temperature Range ---------- –40°C to 125°C
- Ambient Temperature Range ---------- –40°C to 85°C

Electrical Characteristics

(V_{DD1} = V_{DD2} = V_{DD3} = V_{DD4} = 3.3V, T_A = 25°C, unless otherwise specified)

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Supply Voltage						
Minimum Operating Input Voltage		R_L = 3kΩ	--	--	1.7	V
Minimum Startup Voltage (Boost)	V_{ST}	R_L = 3kΩ	--	0.8	1.1	V
VDD1 Operating Voltage	V_{DD1}		1.7	--	5	V
VDD2 Operating Voltage	V_{DD2}	VDD2, PVDD2 Pin Voltage	1.7	--	5	V
VDD3 Operating Voltage	V_{DD3}		2.5	--	5	V
VDD4 Operating Voltage	V_{DD4}		1.5	--	5	V
VDD1 Over Voltage Protection			5.1	6	6.5	V
Supply Current						
Shutdown Supply Current	I_{OFF}	V_{ENBST} = V_{ENSW} = 0V V_{DD4} = 0V = V_{DD3}	--	--	10	uA
Boost Supply Current	I_{VDD1}	V_{DD1} = 3.3V, V_{FB1} = 0.9V V_{ENBST} = V_{ENSW} = 3.3V V_{OUT1} = 3.3V V_{DD2} = V_{DD3} = V_{DD4} = 0V (no switching)	--	45	70	uA
Buck Supply Current	I_{VDD2}	V_{DD2} = 3.3V, V_{FB2} = 0.9V V_{ENBST} = V_{ENSW} = 0V V_{DD1} = V_{DD3} = V_{DD4} = 0V (no switching)	--	85	140	uA

To be continued

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
LDO Supply Current	I_{VDD3}	V_{DD3} = 5V V_{ENBST} = V_{ENSW} = 0V V_{DD1} = V_{DD2} = V_{DD4} = 0V	--	90	130	uA
Voltage Detector Supply Current	I_{VDD4}	V_{DD4} = 3.3V V_{ENBST} = V_{ENSW} = 0V V_{DD1} = V_{DD3} = V_{DD3} = 0V	--	10	--	uA
Feedback Voltage (CH1, CH2)						
Feedback Voltage	V_{FB}	FB1, FB2	0.292	0.3	0.312	V
Line Regulation of Feedback Voltage of CH1	$\lvert \Delta V_{FB} \rvert$	I_L = 30mA, V_{OUT} = 2.8V V_{BAT} = 0.9 to 1.5V	--	--	8	mV
Power Switch						
CH1 On Resistance of MOSFET	$R_{DS(ON)}$	N-MOSFET, V_{OUT1} = 3.3V	--	200	400	mΩ
		P-MOSFET, V_{OUT1} = 3.3V				
CH1 Current Limitation (Note 5)			--	1.2	--	A
CH2 On Resistance of MOSFET	$R_{DS(ON)}$	N-MOSFET, V_{DD2} = 3.3V	--	320	450	mΩ
		P-MOSFET, V_{DD2} = 3.3V	--	400	560	mΩ
CH2 Current Limitation		P-MOSFET	--	0.6	--	A
Voltage Detector						
Feedback Voltage	V_{FB4}	FB4 Falling Edge	0.292	0.3	0.308	V
Threshold Hysteresis		Refer to FB4	--	25	--	mV
RESET Output Current		N-MOSFET, V_{DD4} = 3.3V, V_{DS} = 0.5V	--	3	--	mA
		P-MOSFET, V_{DD4} = 3.3V, V_{DS} = -0.5V				
CT Pin Threshold Voltage	V_{CT}	V_{DD4} = 3.3V	0.65	0.8	1	V
CT Pin Output Current	I_{CT}		--	1	--	uA
Linear Regulator						
Output Voltage Accuracy		I_L = 1mA, V_{OUT3} = 3.5V, 3.3V, 3V	–2	--	+2	%
Feedback Voltage	V_{FB3}		--	1.2	--	V
Current Limit	I_{OUT3_LIM}		400	600	--	mA
Dropout Voltage	V_{DROP}	I_{VOUT3} = 200mA	--	0.3	0.4	V
Line Regulation	ΔV_{LINE}	V_{DD3} = (V_{OUT3} + 1V) to 5.5V I_{OUT3} = 1mA	--	--	0.5	%
Load Regulation	ΔV_{OUT3}	I_{OUT3} = 50mA to 200mA V_{DD3} = 4.8V, V_{OUT3} = 3.3V	--	--	30	mV
Control						
ENLDO Input High Level Threshold		V_{DD1} = 2.8V	--	--	1.1	V

To be continued

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
ENLDO Input Low Level Threshold		V_{DD1} = 2.8V	0.4	--	--	V
ENBST/ ENSW Input High Level Threshold		V_{BAT} = 1V	--	--	0.7	V
ENBST/ ENSW Input Low Level Threshold		V_{BAT} = 1V	0.2	--	--	V
ENBST Pull Low Current			--	1	--	uA
ENBUK Pull Low Current			--	1	--	uA
Thermal Protection						
Thermal Shutdown	T_{SD}		--	160	--	°C
Thermal Shutdown Hysteresis	ΔT_{SD}		--	10	--	°C

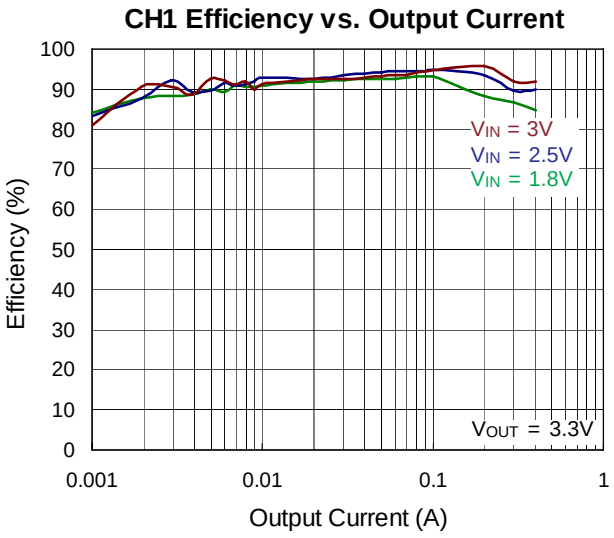
Note 1. Stresses listed as the above "Absolute Maximum Ratings" may cause permanent damage to the device. These are for stress ratings. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may remain possibility to affect device reliability.

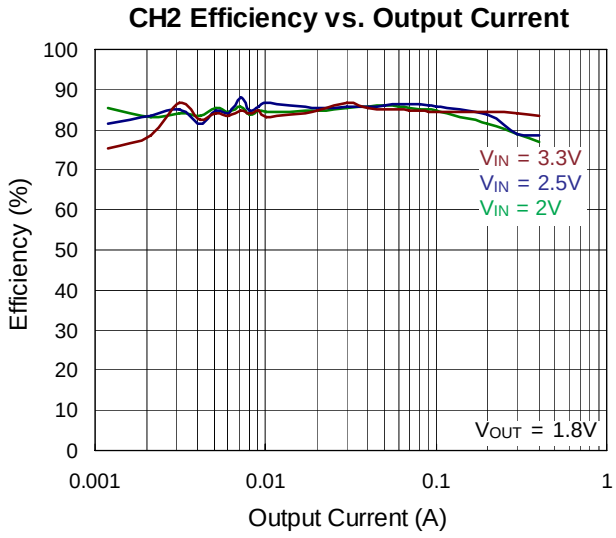
Note 2. θ_{JA} is measured in the natural convection at T_A = 25°C on a high effective four layers thermal conductivity test board of JEDEC 51-7 thermal measurement standard. The case point of θ_{JC} is on the expose pad for the package.

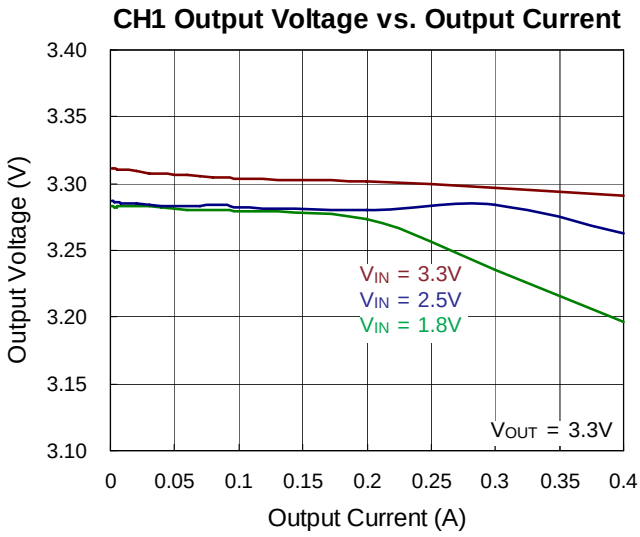
Note 3. Devices are ESD sensitive. Handling precaution is recommended.

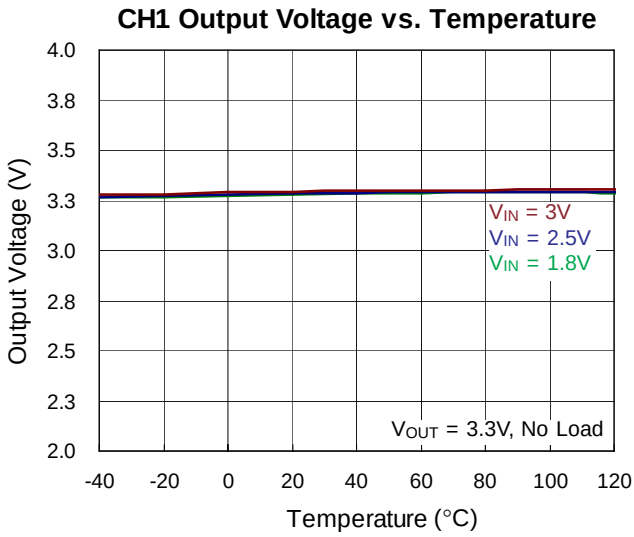
Note 4. The device is not guaranteed to function outside its operating conditions.

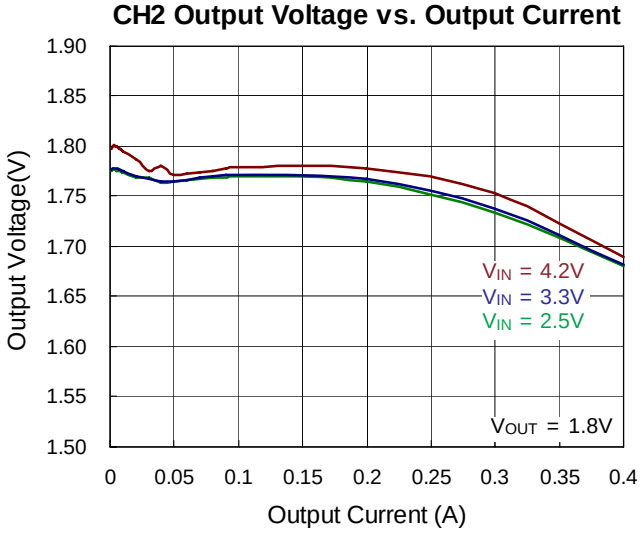
Typical Operating Characteristics

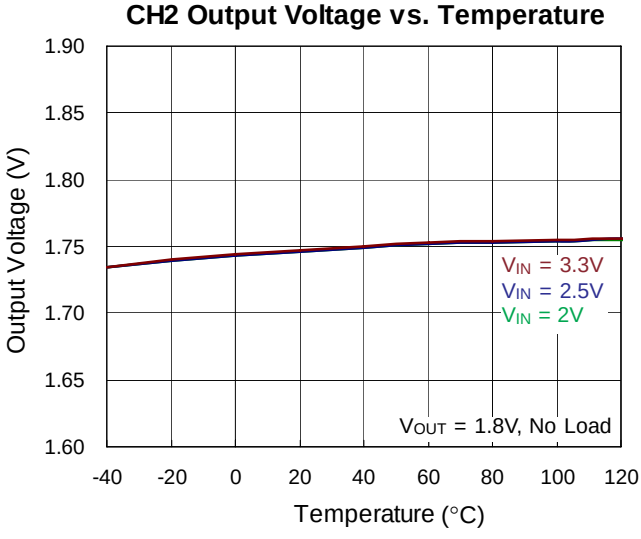


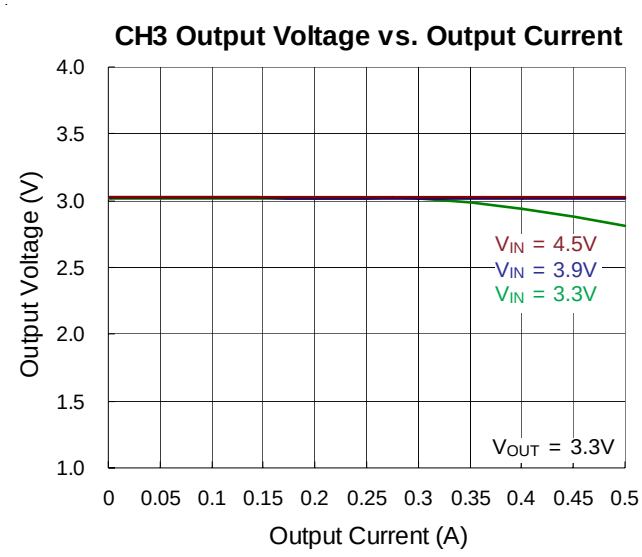


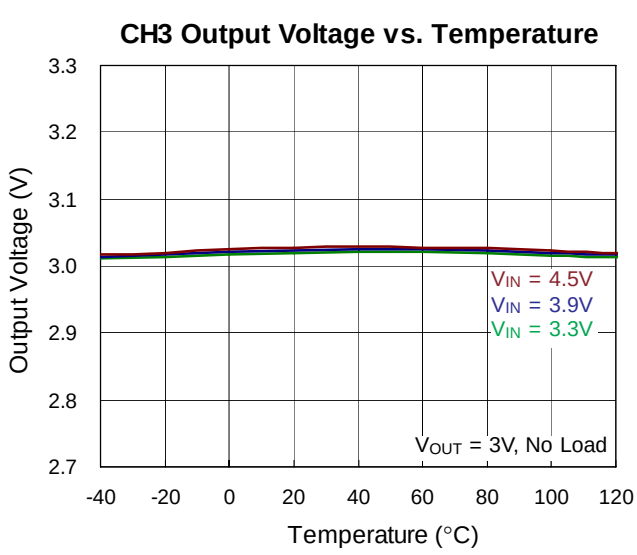


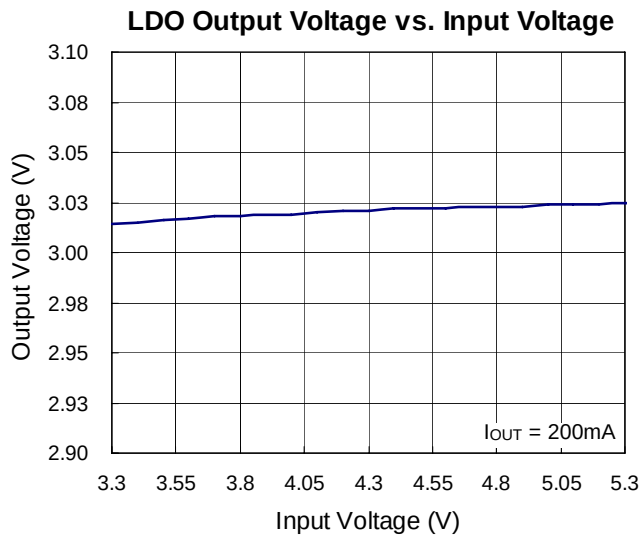


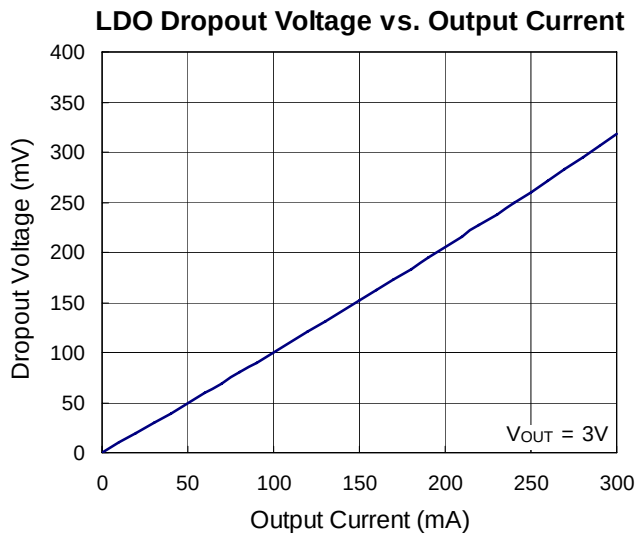


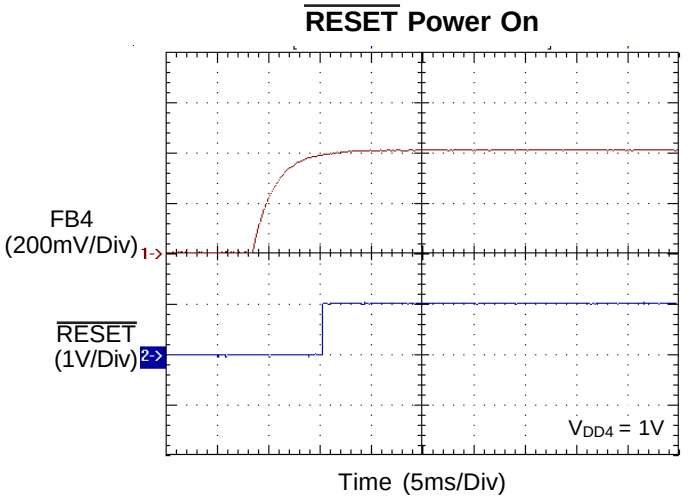


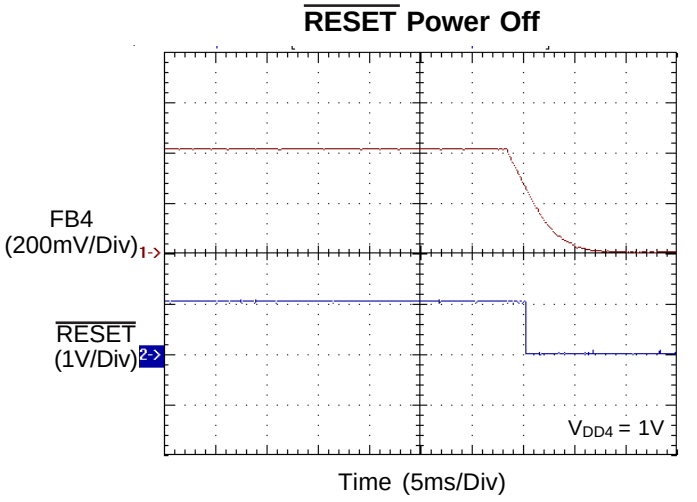

CH3 Output Voltage vs. Output Current
Output Voltage (V)
4.0
3.5
3.0
2.5
2.0
1.5
1.0
0 0.05 0.1 0.15 0.2 0.25 0.3 0.35 0.4 0.45 0.5
Output Current (A)
VIN = 4.5V
VIN = 3.9V
VIN = 3.3V
VOUT = 3.3V


CH3 Output Voltage vs. Temperature
Output Voltage (V)
3.3
3.2
3.1
3.0
2.9
2.8
2.7
-40 -20 0 20 40 60 80 100 120
Temperature (°C)
VIN = 4.5V
VIN = 3.9V
VIN = 3.3V
VOUT = 3V, No Load


LDO Output Voltage vs. Input Voltage
Output Voltage (V)
3.10
3.08
3.05
3.03
3.00
2.98
2.95
2.93
2.90
3.3 3.55 3.8 4.05 4.3 4.55 4.8 5.05 5.3
Input Voltage (V)
IOUT = 200mA


LDO Dropout Voltage vs. Output Current
Dropout Voltage (mV)
400
350
300
250
200
150
100
50
0
0 50 100 150 200 250 300
Output Current (mA)
VOUT = 3V


RESET Power On
FB4
(200mV/Div)
1->
RESET
(1V/Div)
2->
VDD4 = 1V
Time (5ms/Div)


RESET Power Off
FB4
(200mV/Div)
1->
RESET
(1V/Div)
2->
VDD4 = 1V
Time (5ms/Div)

Application Information

RT9912A is a four-channel power management IC (PMIC) including one step-up DC-DC converter (Boost), one step-down DC-DC converter (Buck), one low dropout regulator (LDO) and one voltage detector. For optimizing the application of portable hand-held system with one or two alkaline battery, several special logics are designed in this chip. An external P-MOSFET is also needed for load-disconnected function.

Step-Up DC-DC Converter (Boost)

The step-up DC-DC convert can start up even with the input voltage as low as 0.8V and operates with the input voltage down to 0.7V. The cost of system is reduced by the internal synchronous rectifier from eliminating an external Schottky diode. The efficiency of light load is improved by the pulse frequency modulation mode (PFM) low quiescent current 30uA. The efficiency of heavy load is also maintained by the internal synchronous rectifier with resistance low to 0.2Ω.

The step-up DC-DC converter is designed as a bootstrapped structure. As the chip is in the start-up period, a low voltage start-up circuit will pull the output voltage to a higher voltage (~1.5V). After the output voltage reaches a certain level, the main DC-DC circuitry will keep working to pull the output voltage to the expected value set by output divided resistor. The control scheme of the step-up DC-DC converter is pulse frequency modulation mode (PFM) with constant-on-time and minimum-off-time. This scheme can keep high efficiency during a wide load range. An internal soft-start is also included in the step-up DC-DC converter to limit the inrush current to less than a half of the OCP level. As the ENBST is pulled low, the step-up DC-DC converter will enter shutdown mode and all function will be disabled.

As the ENSW is pulled high, the PSW will be pulled low when the output of the step-up DC-DC converter is ready (soft-start is finished). An external P-MOSFET is needed to be a load-disconnected switch. The PSW is a signal to control the external P-MOSFET. All loadings of the system should be connected to the drain pin of the P-MOSFET to prevent the step-up DC-DC converter start-up in heavy load condition.

The maximum duty (D) of the step-up DC-DC converter is around 50% so that the maximum output voltage is ideally to be V_{IN} / (1-D) = 2 x V_{IN}. Actually, some voltage will drop on the internal N-MOSFET and inductor. Therefore, the maximum output voltage will be lower than the ideal value and to be 2 x V_{IN}.

The function of R9 and C14 is preventing the charge sharing issue from the capacitor in Q1's source pin to the capacitor in Q1's drain pin. If the capacitor in Q1's source pin is 10 times larger than the capacitor in Q1's drain pin, R9 and C14 can be removed.

Step-Down DC-DC Converter (Buck)

The step-down DC-DC convert can reduce the cost of system by the internal synchronous rectifier from eliminating an external Schottky diode. The light load efficiency is improved by the pulse frequency modulation mode (PFM) and internal synchronous rectifier. For heavy load, the efficiency is maintained by the internal synchronous rectifier with the resistance low to 0.4Ω. The control scheme of the step-down DC-DC converter is pulse frequency modulation mode (PFM) with over-current-protection (OCP) and minimum-off-time. This scheme can keep high efficiency during a wide load range. An internal soft-start is also included in the step-down DC-DC converter to limit the inrush current less than a half of OCP level.

This step-down converter can operate in low-drop mode and its output voltage depends on the voltage drop cross the internal P-MOSFET and inductor. Normally, the value is near VDD2 as the ESR of inductor is 0.1Ω and 60mA loading. The minimum output voltage is 0.6V, which is decided by the operation range of the internal circuit.

Low Dropout Regulator (LDO)

The low dropout regulator can regulate the output voltage by setting the external resistor of FB3. An internal compensation structure is designed for keeping stability as wide range output capacitor and wide range loading. The voltage detector is a comparator with reference to detect the voltage of FB4.

The maximum output voltage for LDO depends on the voltage drop cross the internal P-MOSFET. Normally, the value is (VDD3 – 0.4V) as 200mA loading. The minimum output voltage is 1.6V, which is decided by the working range of the internal circuit.

Output Voltage Setting

The regulated output voltage can be calculated following formula :

$$V_{OUT} = V_{FB} \times \left(1 + \frac{R1}{R2}\right)$$

To place the resistor-divider as close as possible to chip can reduce noise sensitivity.

Voltage Detector

The RT9912A integrates a voltage detector with push-pull output. The voltage detector senses VDD3V3_IO through a resistor divider and compares it with internal 0.3V reference voltage. When the sensed voltage is lower than the reference voltage, the RESET pin output logic low signal for system access. Connecting a capacitor from the CT pin to GND can set the detect delay time according to Figure 1.

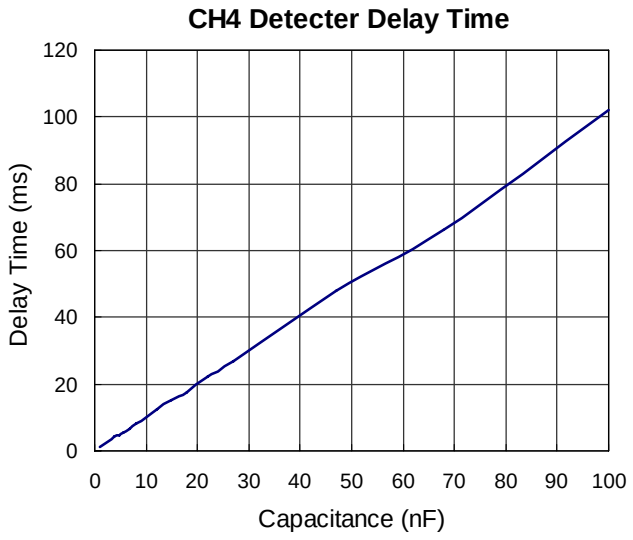


Figure 1. Detector Delay Time

Inductor Selection

To select suitable inductance value is very important for optimal performance. For boost converter, the control method is constant on time and minimum off time. If the inductance is low, it will cause effects of high in ductor current and high output voltage ripple. The inductance value can be calculated by following formula.

$$L_{MIN} \geq \frac{V_{IN(MAX)} \times T_{ON}}{V_{LIM(MIN)}}$$

Where L_{MIN} = minimum inductance

$V_{IN(MAX)}$ = maximum input voltage

T_{ON} = 0.75us

$I_{LIM(MIN)}$ = 0.8A

A 4.7uH inductor is recommended for typical application.

For buck converter, a 4.7uH inductor is recommended when V_{IN} is less than 2.6V.

In addition, make sure the inductor saturation current rating should be greater than the inductor peak current.

Input Capacitor Selection

For better input bypassing, low-ESR ceramic capacitor is recommended for better performance. A 10uF input capacitor is sufficient and it is flexible to reduce the value for a lower output power requirement.

Output Capacitor Selection

For lower output voltage ripple, low-ESR ceramic capacitor is recommended. The output voltage ripple consists of two components : one is the pulsating output ripple current flowing through the ESR, and the other is the capacitive ripple caused by charging and discharging.

For ceramic capacitor, the voltage ripple value is approximated by :

$$V_{RIPPLE} \cong V_{RIPPLE\_C}$$

For boost converter, calculate the minimum output capacitance as the following formula :

$$C_{OUT} \geq \frac{L \times 0.5 I_{PEAK}^2}{V_{REPPLE\_C}}$$

For buck converter, calculate the minimum output capacitance as the following formula :

$$C_{OUT} \geq \frac{I_{OUT(MAX)} \times \left(1 - \frac{I_{OUT(MAX)}}{I_{PEAK}}\right)^2}{f \times V_{REPPLE\_C}}$$

THERMAL CONSIDERATIONS

For continuous operation, do not exceed absolute maximum operation junction temperature. The maximum power dissipation depends on the thermal resistance of IC package, PCB layout, the rate of surroundings airflow and temperature difference between junction to ambient. The maximum power dissipation can be calculated by following formula :

$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$

Where $T_{J(MAX)}$ is the maximum operation junction temperature 125°C, T_A is the ambient temperature and the θ_{JA} is the junction to ambient thermal resistance.

For recommended operating conditions specification of RT9912A, where $T_{J(MAX)}$ is the maximum junction temperature of the die (125°C) and T_A is the maximum ambient temperature. The junction to ambient thermal resistance θ_{JA} is layout dependent. For WQFN-24L 4x4 packages, the thermal resistance θ_{JA} is 54° C/W on the standard JEDEC 51-7 four layers thermal test board. The maximum power dissipation at T_A = 25°C can be calculated by following formula :

$P_{D(MAX)}$ = (125°C – 25°C) / (54°C/W) = 1.852W for WQFN-24L 4x4 packages

The maximum power dissipation depends on operating ambient temperature for fixed $T_{J(MAX)}$ and thermal resistance θ_{JA}. For RT9912A packages, the Figure 2 of derating curves allows the designer to see the effect of rising ambient temperature on the maximum power allowed.

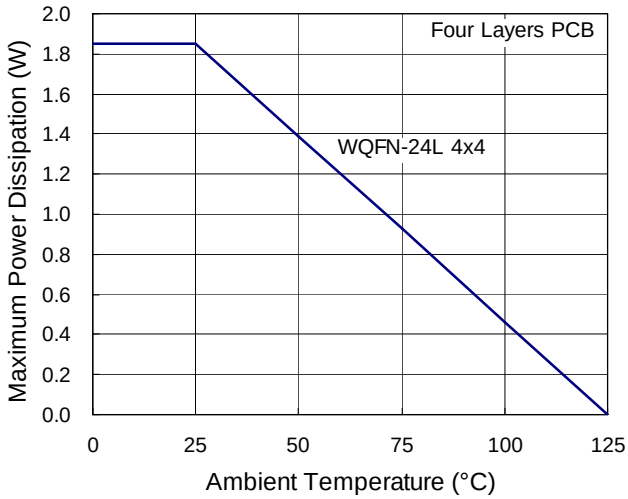


Figure 2. Derating Curves for RT9912A Packages

Layout Considerations

For the best performance of the RT9912A, the following PCB Layout guidelines must be strictly followed.

- Place the input and output capacitors as close as possible to the input and output pins respectively for good filtering.
- Keep the main power traces as possible as wide and short.
- The switching node area connected to LX and inductor should be minimized for lower EMI.
- Place the feedback components as close as possible to the FB pin and keep these components away from the noisy devices.
- Connect the GND and Exposed Pad to a strong ground plane for maximum thermal dissipation and noise protection.

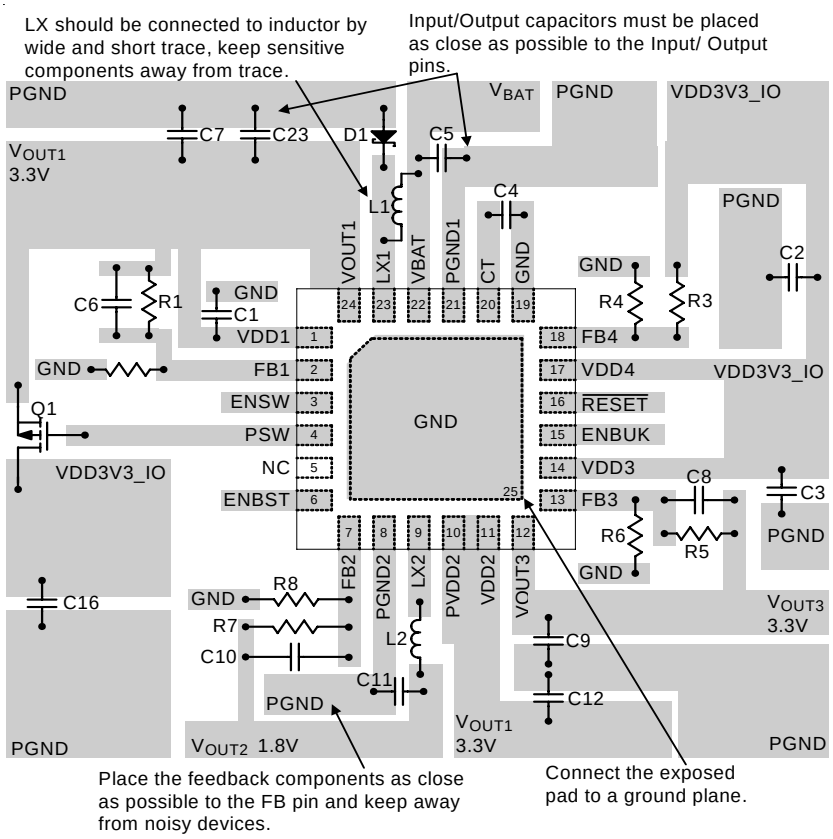
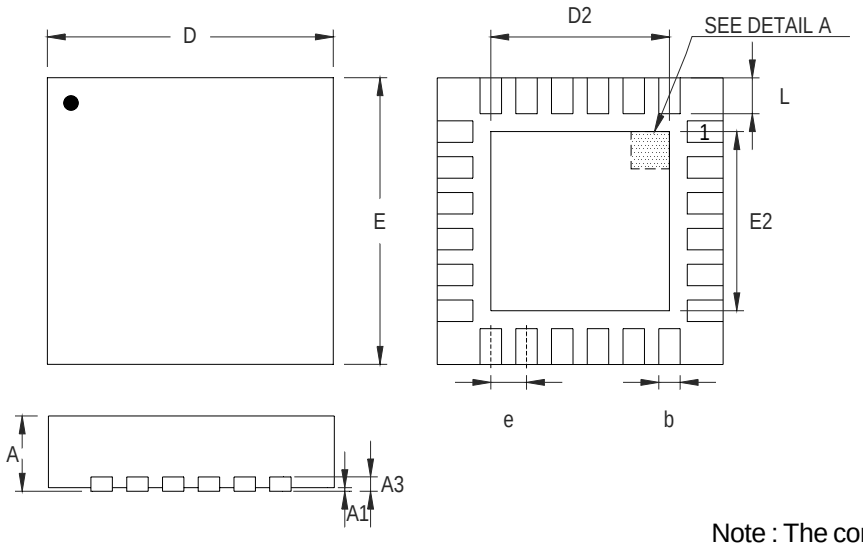
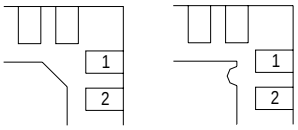


Figure 3. PCB Layout Guide

Outline Dimension





DETAIL A

Pin #1 ID and Tie Bar Mark Options

Note : The configuration of the Pin #1 identifier is optional, but must be located within the zone indicated.

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A3	0.175	0.250	0.007	0.010
b	0.180	0.300	0.007	0.012
D	3.950	4.050	0.156	0.159
D2	2.300	2.750	0.091	0.108
E	3.950	4.050	0.156	0.159
E2	2.300	2.750	0.091	0.108
e	0.500		0.020	
L	0.350	0.450	0.014	0.018

W-Type 24L QFN 4x4 Package

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