DATA SHEET

TDA8761
9-bit analog-to-digital converter for digital video

Preliminary specification
File under Integrated Circuits, IC02

1995 Mar 20

Philips Semiconductors

PHILIPS

9-bit analog-to-digital converter for digital video

TDA8761

FEATURES

- 9-bit resolution
- Sampling rate up to 30 MHz
- DC sampling allowed
- One clock cycle conversion only
- High signal-to-noise ratio over a large analog input frequency range (8.5 effective bits at 10 MHz full-scale input at f_{clk} = 30 MHz)
- No missing codes guaranteed
- In range (IR) 3-state TTL output
- TTL compatible digital inputs and outputs
- Low-level AC clock input signal allowed
- External reference voltage regulator
- Power dissipation only 360 mW (typical)
- Low analog input capacitance, no buffer amplifier required
- No sample-and-hold circuit required.

APPLICATIONS

Analog-to-digital conversion for:

- Video data digitizing
- Digital Video Broadcasting (DVB)
- Cable TV.

GENERAL DESCRIPTION

The TDA8761 is a 9-bit analog-to-digital converter (ADC) for professional video and digital video set box applications. It converts the analog input signal into 9-bit binary-coded digital words at a maximum sampling rate of 30 MHz. Its linearity performance ensures the required conversion accuracy in case of 256QAM demodulator concept and for all symbol frequencies. All digital inputs and outputs are TTL compatible, although a low-level sine wave clock input signal is allowed.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{CCA}	analog supply voltage		4.75	5.0	5.25	V
V_{CCD}	digital supply voltage		4.75	5.0	5.25	V
V_{CCO}	output stages supply voltage		4.4	5.0	5.25	V
I_{CCA}	analog supply current		–	30	tbf	mA
I_{CCD}	digital supply current		–	22	tbf	mA
I_{CCO}	output stages supply current		–	22	tbf	mA
AINL	AC integral non-linearity	note 1; full scale input sine wave	–	±0.75	tbf	LSB
		note 1; 50% full scale input sine wave	–	±0.5	tbf	LSB
ADNL	AC differential non-linearity	note 1; full scale input sine wave	–	±0.5	tbf	LSB
		note 1; 50% full scale input sine wave	–	±0.3	tbf	LSB
$f_{clk(max)}$	maximum clock frequency		30	–	–	MHz
P_{tot}	total power dissipation		–	360	tbf	mW

Note

1. f_i = 11 MHz and f_{clk} = 30 MHz; f_i = 8 MHz and f_{clk} = 20 MHz.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA8761M	SSOP28	plastic shrink small outline package; 28 leads; body width 5.3 mm	SOT341-1

BLOCK DIAGRAM

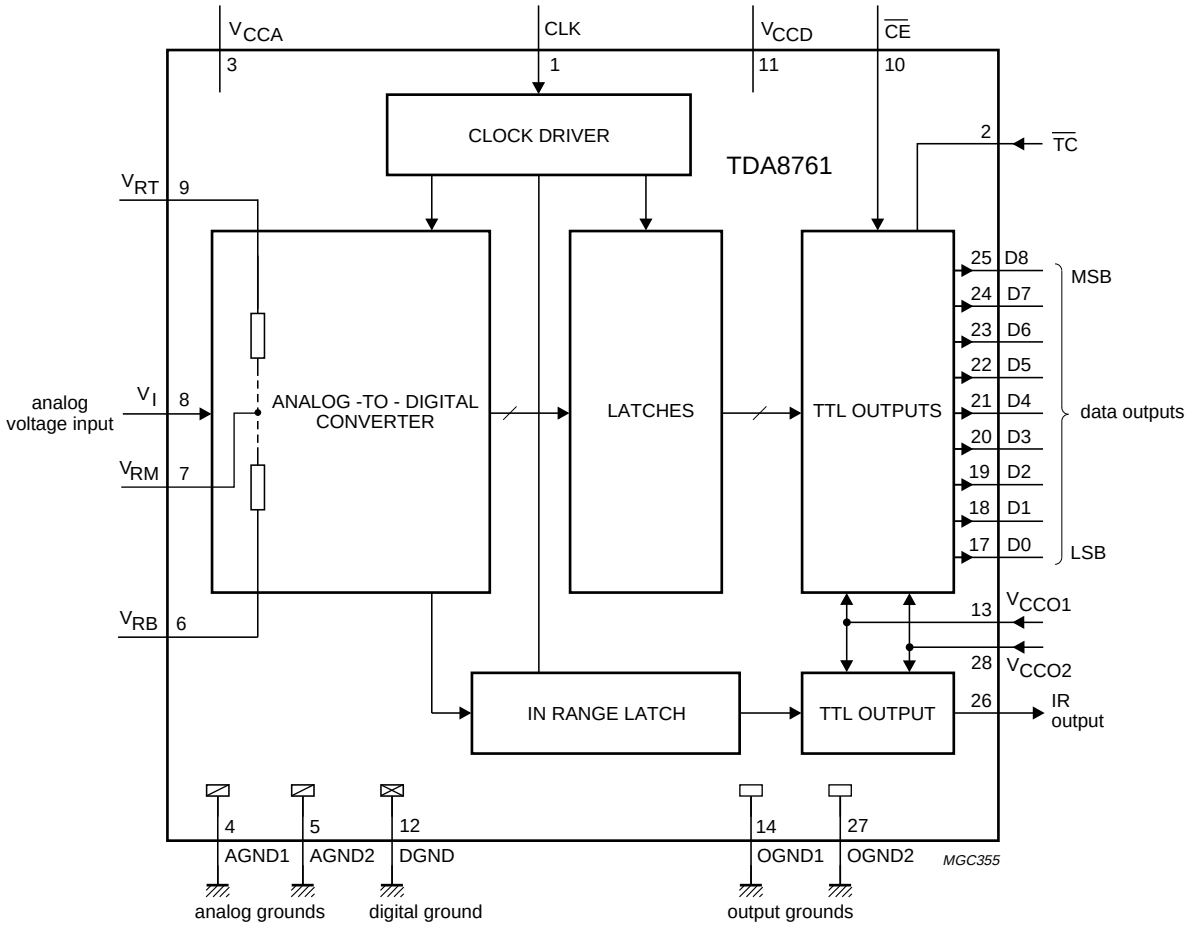


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
CLK	1	clock input
$\overline{TC}$	2	two's complement input (active LOW)
V_{CCA}	3	analog supply voltage (+5 V)
AGND1	4	analog ground 1
AGND2	5	analog ground 2
V_{RB}	6	reference voltage BOTTOM input
V_{RM}	7	reference voltage MIDDLE
V_I	8	analog input voltage
V_{RT}	9	reference voltage TOP input
$\overline{CE}$	10	chip enable input (TTL level input, active LOW)
V_{CCD}	11	digital supply voltage (+5 V)
DGND	12	digital ground
V_{CCO1}	13	supply voltage for output stages 1 (+5 V)
OGND1	14	output ground 1
n.c.	15	not connected
n.c.	16	not connected
D0	17	data output; bit 0 (LSB)
D1	18	data output; bit 1
D2	19	data output; bit 2
D3	20	data output; bit 3
D4	21	data output; bit 4
D5	22	data output; bit 5
D6	23	data output; bit 6
D7	24	data output; bit 7
D8	25	data output; bit 8 (MSB)
IR	26	in range data output
OGND2	27	output ground 2
V_{CCO2}	28	supply voltage for output stages 2 (+5 V)

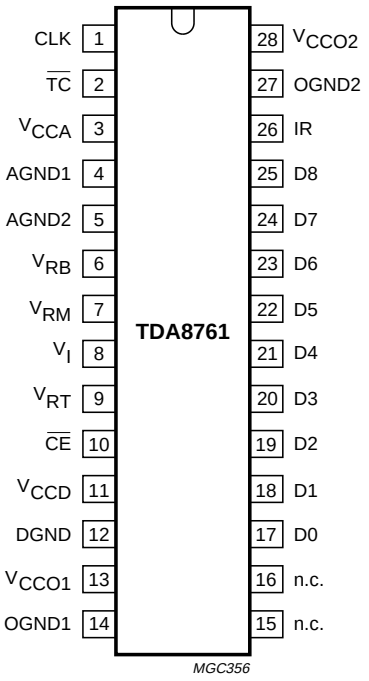


Fig.2 Pin configuration.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CCA}	analog supply voltage	note 1	–0.3	+7.0	V
V_{CCD}	digital supply voltage	note 1	–0.3	+7.0	V
V_{CCO}	output stages supply voltage	note 1	–0.3	+7.0	V
ΔV_{CC}	supply voltage differences between				
	V_{CCA} and V_{CCD}		–1.0	+1.0	V
	V_{CCO} and V_{CCD}		–1.0	+1.0	V
	V_{CCA} and V_{CCO}		–1.0	+1.0	V
V_I	input voltage	referenced to AGND	–0.3	+7.0	V
$V_{i(p-p)}$	AC input voltage for switching (peak-to-peak value)	referenced to DGND	–	V_{CCD}	V
I_O	output current		–	10	mA
T_{stg}	storage temperature		–55	+150	°C
T_{amb}	operating ambient temperature		0	+70	°C
T_j	junction temperature		–	+150	°C

Note

1. The supply voltages V_{CCA}, V_{CCD} and V_{CCO} may have any value between –0.3 V and +7.0 V provided the difference between V_{CCA}, V_{CCD} and V_{CCO} is between –1 and +1 V.

HANDLING

Inputs and outputs are protected against electrostatic discharges in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling integrated circuits.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient in free air	110	K/W

CHARACTERISTICS

V_{CCA} = V_3 to V_4 and V_5 = 4.75 to 5.25 V; V_{CCD} = V_{11} to V_{12} = 4.75 to 5.25 V; V_{CCO} = V_{13} and V_{28} to V_{14} and V_{27} = 4.4 to 5.25 V; AGND and DGND shorted together; T_{amb} = 0 to +70 °C; typical values measured at V_{CCA} = V_{CCD} = V_{CCO} = 5 V; $V_{i(p-p)}$ = 1.5 V; C_L = 15 pF and T_{amb} = 25 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{CCA}	analog supply voltage		4.75	5.0	5.25	V
V_{CCD}	digital supply voltage		4.75	5.0	5.25	V
V_{CCO}	output stages supply voltage		4.4	5.0	5.25	V
ΔV_{CC}	supply voltage differences between					
	V_{CCA} and V_{CCD}		–0.25	–	+0.25	V
	V_{CCA} and V_{CCO}		–0.4	–	+0.4	V
	V_{CCD} and V_{CCO}		–0.4	–	+0.4	V
I_{CCA}	analog supply current		–	30	tbf	mA
I_{CCD}	digital supply current		–	22	tbf	mA
I_{CCO}	output stages supply current		–	22	tbf	mA
Inputs						
CLOCK INPUT CLK (REFERENCED TO DGND); note 1						
V_{IL}	LOW level input voltage		0	–	0.8	V
V_{IH}	HIGH level input voltage		2.0	–	V_{CCD}	V
I_{IL}	LOW level input current	V_{clk} = 0.4 V	–1	0	+1	µA
I_{IH}	HIGH level input current	V_{clk} = 2.7 V	–	–	20	µA
Z_I	input impedance	f_{clk} = 30 MHz	–	2	–	kΩ
C_I	input capacitance	f_{clk} = 30 MHz	–	2	–	pF
INPUT $\overline{CE}$ (REFERENCED TO DGND); see Table 2						
V_{IL}	LOW level input voltage		0	–	0.8	V
V_{IH}	HIGH level input voltage		2.0	–	V_{CCD}	V
I_{IL}	LOW level input current	V_{IL} = 0.4 V	–400	–	–	µA
I_{IH}	HIGH level input current	V_{IH} = 2.7 V	–	–	20	µA
V_I (ANALOG INPUT VOLTAGE REFERENCED TO AGND)						
I_{IL}	LOW level input current	V_I = 1.3 V	–	0	–	µA
I_{IH}	HIGH level input current	V_I = 3.8 V	–	70	–	µA
Z_I	input impedance	f_i = 10 MHz	–	5	–	kΩ
C_I	input capacitance	f_i = 10 MHz	–	8	–	pF

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Reference voltages for the resistor ladder; see Table 1						
V_{RB}	reference voltage BOTTOM		1.2	1.3	–	V
V_{RT}	reference voltage TOP		–	3.3	V_{CCA} – 0.8 V	V
V_{diff}	differential reference voltage $V_{RT} - V_{RB}$		1.8	2.0	3.0	V
I_{ref}	reference current		–	30	–	mA
R_{LAD}	resistor ladder		–	85	–	Ω
TC_{RLAD}	temperature coefficient of the resistor ladder		–	1.86	–	ppm
			–	158	–	mΩ/K
V_{osB}	offset voltage BOTTOM	note 2	–	250	–	mV
V_{osT}	offset voltage TOP	note 2	–	250	–	mV
$V_{i(p-p)}$	analog input voltage (peak-to-peak value)	note 3	1.3	1.5	2.5	V
Outputs						
DIGITAL OUTPUTS D8 TO D0 AND IR (REFERENCED TO OGND)						
V_{OL}	LOW level output voltage	I_O = 1 mA	0	–	0.4	V
V_{OH}	HIGH level output voltage	I_O = 0 mA	2.7	–	V_{CCO} – 0.5	V
		I_O = –0.4 mA	2.7	–	V_{CCO} – 1.3	V
		I_O = –1 mA	2.4	–	V_{CCO} – 1.4	V
I_{OZ}	output current in 3-state mode	0.4 V < V_O < V_{CCO}	–20	–	+20	µA
Switching characteristics						
CLOCK INPUT CLK; see Fig.3; note 1						
$f_{clk(max)}$	maximum clock frequency		30	–	–	MHz
t_{CPH}	clock pulse width HIGH		10	–	–	ns
t_{CPL}	clock pulse width LOW		10	–	–	ns
Analog signal processing						
LINEARITY						
AINL	AC integral non-linearity	note 5; full scale input sine wave	–	±0.75	tbf	LSB
		note 5; 50% full scale input sine wave	–	±0.5	tbf	LSB
ADNL	AC differential non-linearity	note 5; full scale input sine wave	–	±0.5	tbf	LSB
		note 5; 50% full scale input sine wave	–	±0.3	tbf	LSB
OFER	offset error	middle code; V_{RB} = 1.3 V; V_{RT} = 3.3 V	–	±1	–	LSB
GER	gain error (from device to device)	V_{RB} = 1.3 V; V_{RT} = 3.3 V; note 4	–	±0.1	–	%

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
BANDWIDTH (f_{clk} = 30 MHz)						
B	analog bandwidth	full-scale sine wave; note 6	–	40	–	MHz
		75% full-scale sine wave; note 6	–	55	–	MHz
		small signal at mid-scale; V_I = ±10 LSB at code 256; note 6	–	700	–	MHz
t_{STLH}	analog input settling time LOW-to-HIGH	full-scale square wave; Fig.5; note 7	–	2.0	tbf	ns
t_{STHL}	analog input settling time HIGH-to-LOW	full-scale square wave; Fig.5; note 7	–	2.5	tbf	ns
HARMONICS (f_{clk} = 30 MHz)						
THD	total harmonic distortion	f_i = 10 MHz	–	–64	–	dB
SIGNAL-TO-NOISE RATIO; see Fig.7; note 8						
S/N	signal-to-noise ratio (full scale)	without harmonics; f_{clk} = 30 MHz; f_i = 10 MHz	53	55	–	dB
EFFECTIVE BITS; see Fig 6; note 8						
EB	effective bits	f_{clk} = 30 MHz; f_i = 10 MHz	–	8.5	–	bits
TWO-TONE; note 9						
TTIR	two-tone intermodulation rejection	f_{clk} = 30 MHz	–	–64	–	dB
BIT ERROR RATE						
BER	bit error rate	f_{clk} = 30 MHz; f_i = 10 MHz; V_I = ±16 LSB at code 256	–	10^{-13}	–	times/ sample
DIFFERENTIAL GAIN; note 10						
G_{diff}	differential gain	f_{clk} = 30 MHz; PAL modulated ramp	–	tbf	–	%
DIFFERENTIAL PHASE; note 10						
φ_{diff}	differential phase	f_{clk} = 30 MHz; PAL modulated ramp	–	tbf	–	deg
Timing (f_{clk} = 30 MHz; C_L = 15 pF); see Fig.3; note 11						
t_{ds}	sampling delay time		–	–	2	ns
t_h	output hold time		5	–	–	ns
t_d	output delay time		–	10	14	ns
C_L	digital output load		–	15	40	pF

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
3-state output delay times; see Fig.4						
t_{dZH}	enable HIGH		–	tbf	tbf	ns
t_{dZL}	enable LOW		–	tbf	tbf	ns
t_{dHZ}	disable HIGH		–	tbf	tbf	ns
t_{dLZ}	disable LOW		–	tbf	tbf	ns

Notes

1. In addition to a good layout of the digital and analog ground, it is recommended that the rise and fall times of the clock must not be less than 0.5 ns.
2. Analog input voltages producing code 0 up to and including code 511:
   a) V_{osB} (voltage offset BOTTOM) is the difference between the analog input which produces data equal to 00 and the reference voltage BOTTOM (V_{RB}) at T_{amb} = 25 °C.
   b) V_{osT} (voltage offset TOP) is the difference between V_{RT} (reference voltage TOP) and the analog input which produces data outputs equal to code 511 at T_{amb} = 25 °C.
3. Analog input voltage range can be derived from $V_{RT} - V_{RB}$ difference. It is $\frac{(V_{RT} - V_{RB}) \times 8}{9}$
4. $GER = \frac{(V_{511} - V_0) - 1.5\ V}{1.5\ V} \times 100$
5. f_i = 11 MHz and f_{clk} = 30 MHz; f_i = 8 MHz and f_{clk} = 20 MHz.
6. The analog bandwidth is defined as the maximum input sine wave frequency which can be applied to the device. No glitches greater than 2 LSBs, neither any significant attenuation are observed in the reconstructed signal.
7. The analog input settling time is the minimum time required for the input signal to be stabilized after a sharp full-scale input (square-wave signal) in order to sample the signal and obtain correct output data.
8. Effective bits are obtained via a Fast Fourier Transform (FFT) treatment taking 8K acquisition points per equivalent fundamental period. The calculation takes into account all harmonics and noise up to half of the clock frequency (NYQUIST frequency). Conversion to signal-to-noise ratio: S/N = EB × 6.02 + 1.76 dB.
9. Intermodulation measured relative to either tone with analog input frequencies of 10.0 MHz and 10.10 MHz. The two input signals have the same amplitude and the total amplitude of both signals provides full scale to the converter.
10. Measurement carried out using video analyser VM700A, where the video analog signal is reconstructed through a digital-to-analog converter.
11. Output data acquisition: the output data is available after the maximum delay time of t_d.

Table 1 Output coding and input voltage (typical values; referenced to AGND, V_{RB} = 1.3 V, V_{RT} = 3.3 V)

STEP	$V_{I(p-p)}$	IR	BINARY OUTPUT BITS									TWO'S COMPLEMENT OUTPUT BITS								
			D8	D7	D6	D5	D4	D3	D2	D1	D0	D8	D7	D6	D5	D4	D3	D2	D1	D0
U/F	<1.55	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	1.55	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
1	.	1	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	1
.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.
510	.	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0
511	3.05	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
O/F	>3.05	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Table 2 Mode selection

$\overline{TC}$	$\overline{CE}$	D8 TO D0	IR
X	1	high impedance	high impedance
0	0	active; two's complement	active
1	0	active; binary	active

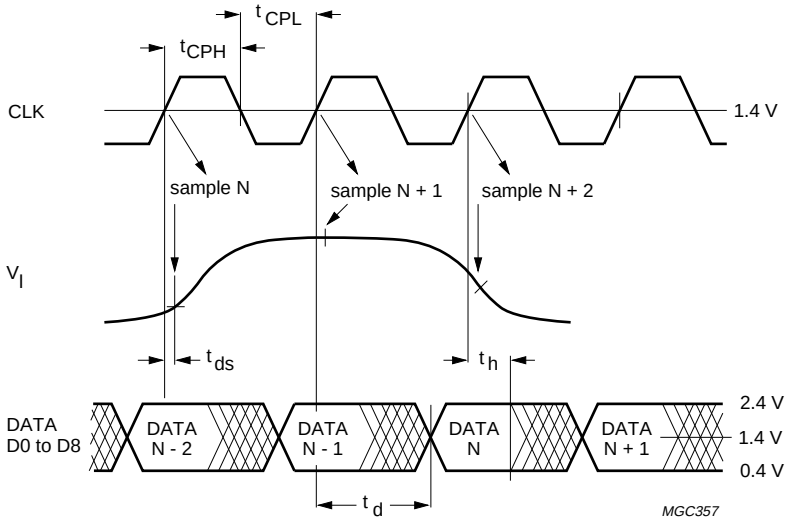
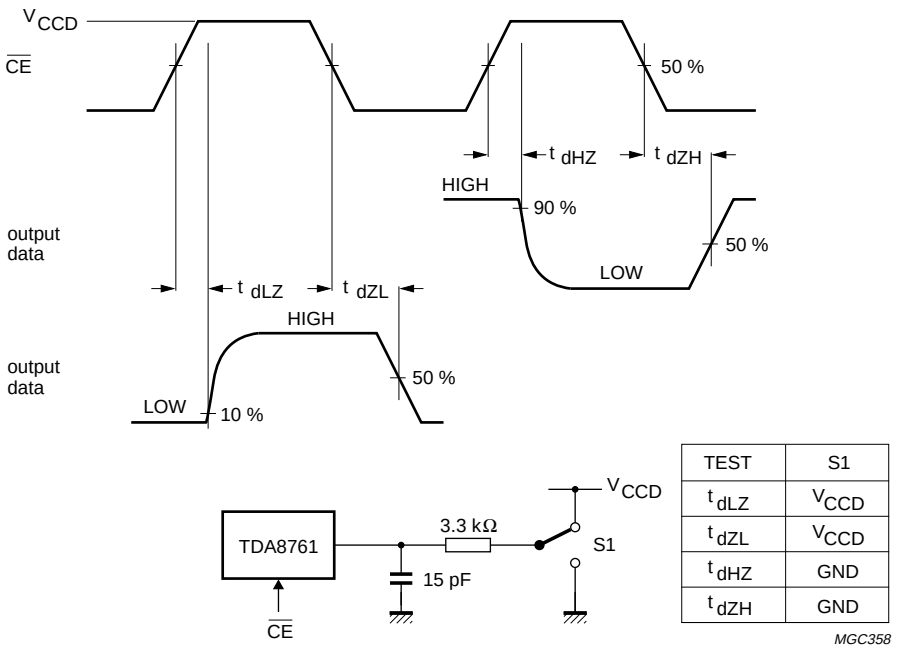


Fig.3 Timing diagram.



TEST	S1
t_{dLZ}	V_{CCD}
t_{dZL}	V_{CCD}
t_{dHZ}	GND
t_{dZH}	GND

$f_{\overline{CE}}$ = 100 kHz.

Fig.4 Timing diagram and test conditions of 3-state output delay time.

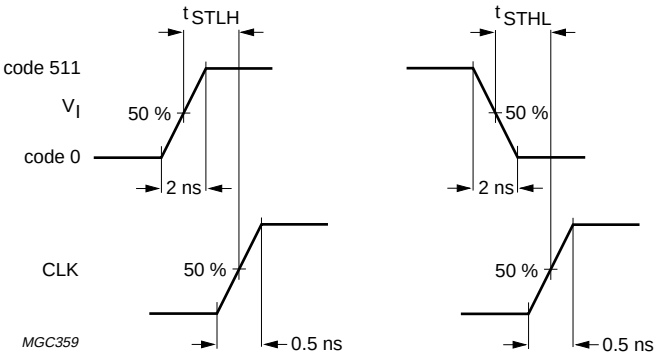
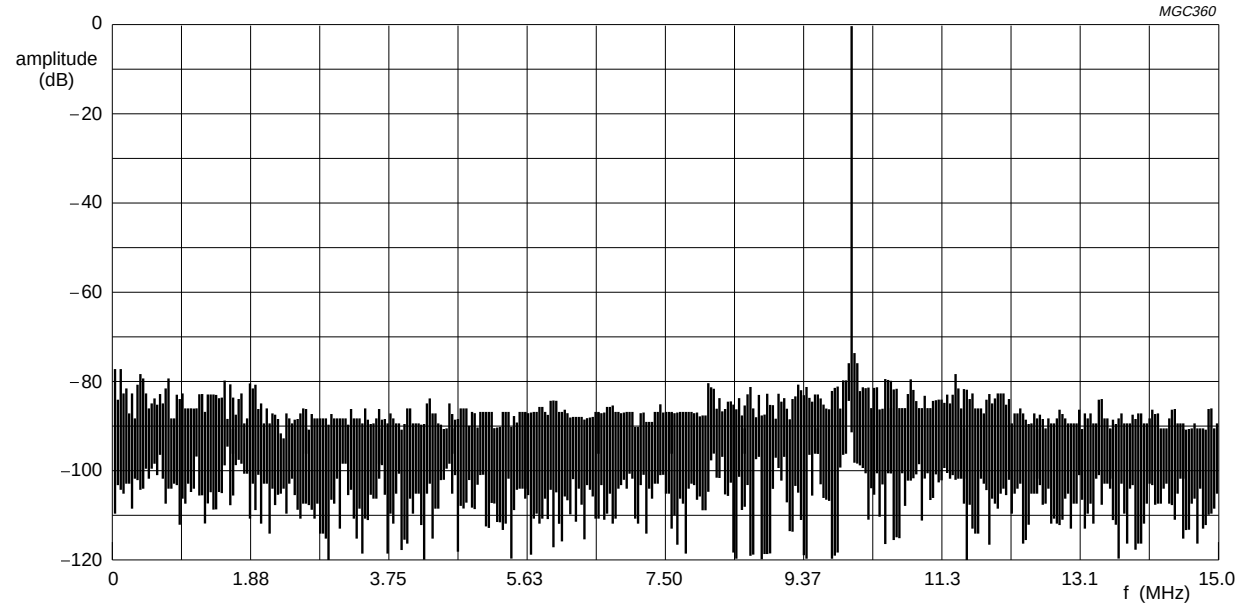


Fig.5 Analog input settling-time diagram.



Effective bits: 8.58; THD = −61.80 dB.
Harmonic levels (dB): 2nd = −64.77; 3rd = −79.30; 4th = −71.90; 5th = −66.12; 6th = −82.29.

Fig.6 Fast Fourier Transform (f_{clk} = 30 MHz; f_i = 10 MHz).

INTERNAL PIN CONFIGURATIONS

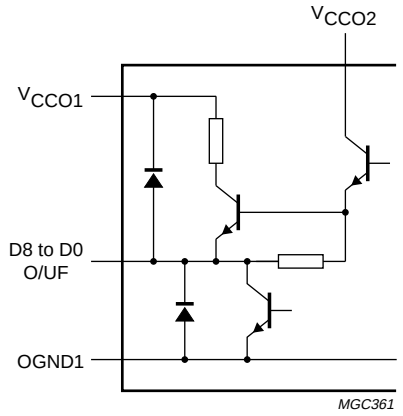


Fig.7 TTL data and in-range outputs.

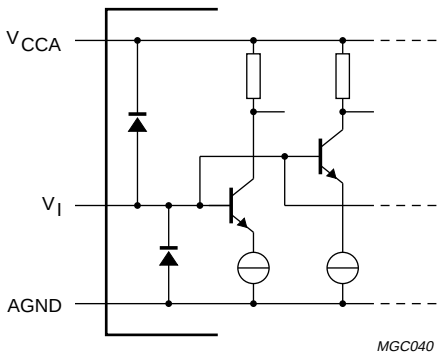


Fig.8 Analog inputs.

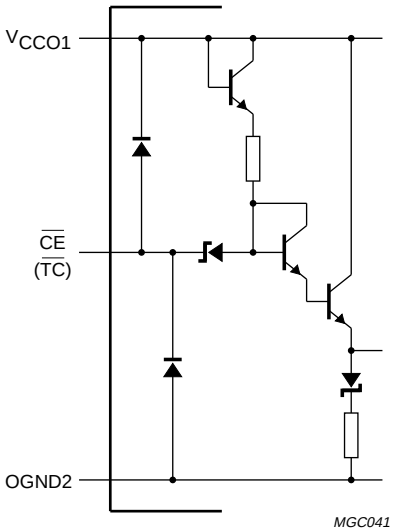


Fig.9 $\overline{CE}$ ($\overline{TC}$) 3-state input.

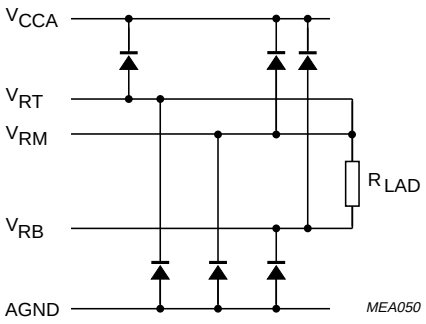


Fig.10 V_{RB}, V_{RM} and V_{RT}.

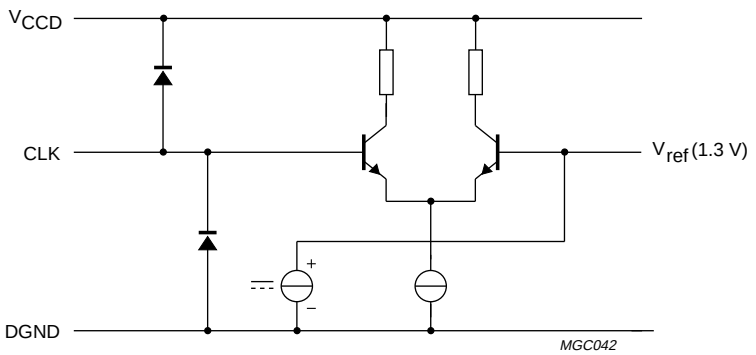
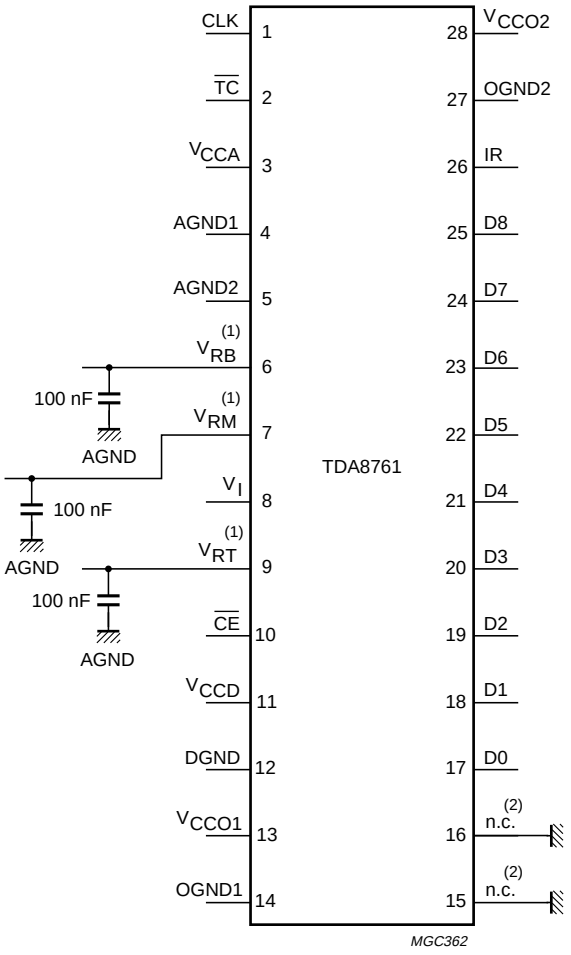


Fig.11 CLK input.

APPLICATION INFORMATION



The analog and digital supplies should be separated and decoupled.

The external voltage generator must be built such that a good supply voltage ripple rejection is achieved with respect to the LSB value. Eventually, the reference ladder voltages can be derived from a well regulated V_{CCA} supply through a resistor bridge and a decoupled capacitor.

For applications where the input signal must remain well centred around middle scale, V_{RM} must be decoupled and connected to analog input signal (pin 8) through a resistor. The values must be defined in accordance with the input signal frequency in order to avoid direct coupling into the ADC ladder (e.g. R = 5 kΩ and C = 100 nF).

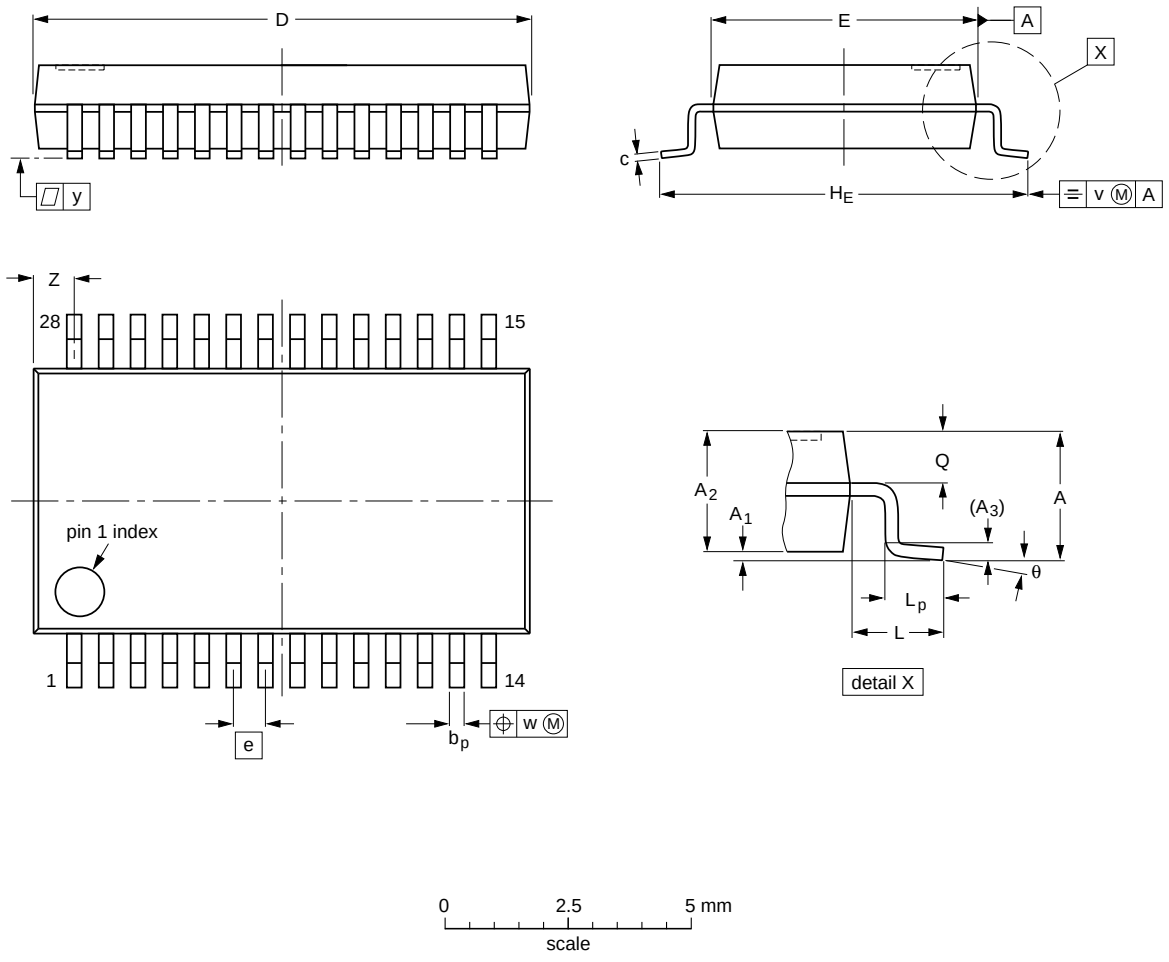
(1) V_{RB}, V_{RM} and V_{RT} are decoupled to AGND.

(2) Pins 15 and 16 should be connected to DGND in order to prevent noise influence.

Fig.12 Application diagram.

PACKAGE OUTLINE

SSOP28: plastic shrink small outline package; 28 leads; body width 5.3 mm **SOT341-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	2.0	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	10.4 10.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	1.1 0.7	8^o 0^o

Note

1. Plastic or metal protrusions of 0.20 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT341-1		MO-150AH				~~93-09-08~~ 95-02-04

SOLDERING

Plastic small outline packages

BY WAVE

During placement and before soldering, the component must be fixed with a droplet of adhesive. After curing the adhesive, the component can be soldered. The adhesive can be applied by screen printing, pin transfer or syringe dispensing.

Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder bath is 10 s, if allowed to cool to less than 150 °C within 6 s. Typical dwell time is 4 s at 250 °C.

A modified wave soldering technique is recommended using two solder waves (dual-wave), in which a turbulent wave with high upward pressure is followed by a smooth laminar wave. Using a mildly-activated flux eliminates the need for removal of corrosive residues in most applications.

BY SOLDER PASTE REFLOW

Reflow soldering requires the solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the substrate by screen printing, stencilling or pressure-syringe dispensing before device placement.

Several techniques exist for reflowing; for example, thermal conduction by heated belt, infrared, and vapour-phase reflow. Dwell times vary between 50 and 300 s according to method. Typical reflow temperatures range from 215 to 250 °C.

Preheating is necessary to dry the paste and evaporate the binding agent. Preheating duration: 45 min at 45 °C.

REPAIRING SOLDERED JOINTS (BY HAND-HELD SOLDERING IRON OR PULSE-HEATED SOLDER TOOL)

Fix the component by first soldering two, diagonally opposite, end pins. Apply the heating tool to the flat part of the pin only. Contact time must be limited to 10 s at up to 300 °C. When using proper tools, all other pins can be soldered in one operation within 2 to 5 s at between 270 and 320 °C. (Pulse-heated soldering is not recommended for SO packages.)

For pulse-heated solder tool (resistance) soldering of VSO packages, solder is applied to the substrate by dipping or by an extra thick tin/lead plating before package placement.

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

LIFE SUPPORT APPLICATIONS

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips for any damages resulting from such improper use or sale.

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Printed in The Netherlands

533061/1500/01/pp20 Date of release: 1995 Mar 20

Document order number: 9397 750 00112

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