

MEMORY

4 M × 32 BIT HYPER PAGE MODE DRAM MODULE

MB8504E032AA-60/-70

4 M × 32 BIT Hyper Page Mode DRAM Module, 5 V, 1-Bank

■ DESCRIPTION

The Fujitsu MB8504E032AA is a fully decoded, CMOS dynamic random access memory (DRAM) module consisting of eight MB8117405A devices. The MB8504E032AA is optimized for those applications requiring high speed, high performance and large memory storage. The operation and electrical characteristics of the MB8504E032AA are the same as the MB8117405A which features hyper page mode operation providing extended valid time for data output and higher speed random access of upto 2,048-bit of data within the same row than the fast page mode. For ease of memory expansion, the MB8504E032AA is offered in a 72-pad Single In-line Memory Module package (SIMM).

■ PRODUCT LINE & FEATURES

Parameter		MB8504E032AA-60	MB8504E032AA-70
RAS Access Time		60 ns max.	70 ns max.
Random Cycle Time		104 ns min.	124 ns min.
Address Access Time		30 ns max.	35 ns max.
CAS Access Time		15 ns max.	17 ns max.
Hyper Page Mode Cycle Time		25 ns min.	30 ns min.
Power Dissipation	Operating Mode	4620 mW max.	3960 mW max.
	Standby Mode	44 mW (CMOS) / 88 mW (TTL)	

- Organization : 4,194,304 words × 32 bits
- Memory : MB8117405A, 8 pcs
- 5.0V ± 10% Supply Voltage
- 2,048 Refresh Cycles / 32.8 ms
- Hyper page mode operation (EDO)

- Package and Ordering Information:
72-pin SIMM, order as
MB8504E032AA-xxSG
(SG = Gold Pad)
MB8504E032AA-xxSS
(SS = Gold Pad)

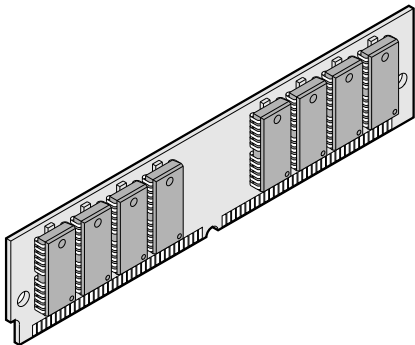
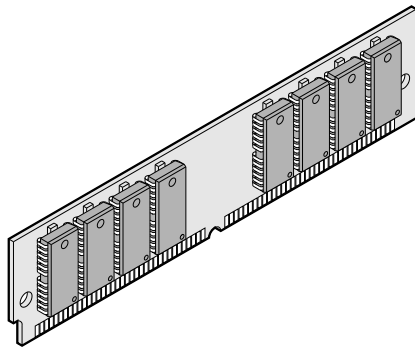
MB8504E032AA-60/-70

■ ABSOLUTE MAXIMUM RATINGS (See WARNING)

Parameter	Symbol	Value	Unit
Supply Voltage	V_{CC}	-0.5 to +7.0	V
Input Voltage	V_{IN}	-0.5 to +7.0	V
Output Voltage	V_{OUT}	-0.5 to +7.0	V
Short Circuit Output Current	I_{OUT}	± 50	mA
Power Dissipation	P_D	8	W
Storage Temperature	T_{STG}	-55 to +125	$^{\circ}C$

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

■ PACKAGE

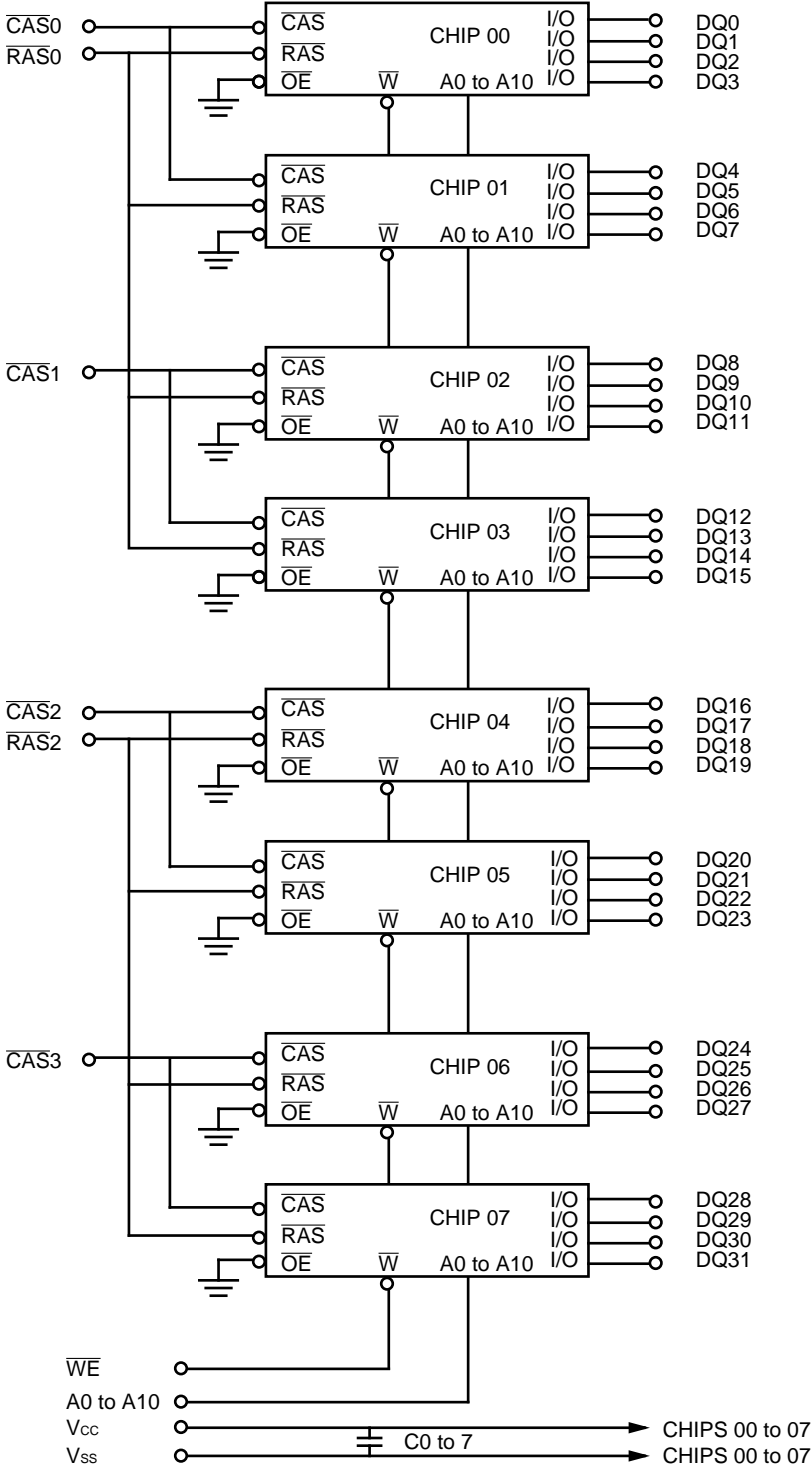


Plastic SIMM Package
(MSS-72P-P77)
(MSS-72P-P79)

DQ0	2	1	V_{SS}
DQ1	4	3	DQ16
DQ2	6	5	DQ17
DQ3	8	7	DQ18
	9	9	DQ19
V_{CC}	10	11	N.C.
A0	12	13	A1
A2	14	15	A3
A4	16	17	A5
A6	18	19	A10
DQ4	20	21	DQ20
DQ5	22	23	DQ21
DQ6	24	25	DQ22
DQ7	26	27	DQ23
A7	28	29	N.C.
V_{CC}	30	31	A8
A9	32	33	N.C.
RAS2	34	35	N.C.
N.C.	36		
N.C.	38	37	N.C.
N.C.	39		V_{SS}
CAS0	40	41	CAS2
CAS3	42	43	CAS1
RAS0	44	45	N.C.
N.C.	46	47	WE
N.C.	48	49	DQ8
DQ24	50	51	DQ9
DQ25	52	53	DQ10
DQ26	54	55	DQ11
DQ27	56	57	DQ12
DQ28	58	59	V_{CC}
DQ29	60	61	DQ13
DQ30	62	63	DQ14
DQ31	64	65	DQ15
N.C.	66	67	PD1
PD2	68	69	PD3
PD4	70	71	N.C.
V_{SS}	72		

Pin #	Symbol	-60	-70
67	PD1	V_{SS}	V_{SS}
68	PD2	N.C.	N.C.
69	PD3	N.C.	V_{SS}
70	PD4	N.C.	N.C.

FUNCTIONAL BLOCK DIAGRAM



MB8504E032AA-60/-70

■ RECOMMENDED OPERATING CONDITION

(Referenced to V_{SS})

Parameter	Symbol	Min.	Typ.	Max.	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	—	0	—	V
Input High Voltage, all inputs	V_{IH}	2.4	—	6.5	V
Input Low Voltage, all inputs*	V_{IL}	-0.3	—	0.8	V
Ambient Temperature	T_A	0	—	70	°C

* : Undershoots of up to -2.0 volts with a pulse width not exceeding 10 ns are acceptable

WARNING: Recommended operating conditions are normal operating ranges for the semiconductor device. All the device's electrical characteristics are warranted when operated within these ranges.

Always use semiconductor devices within the recommended operating conditions. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their FUJITSU representative beforehand.

MB8504E032AA-60/-70

■ DC CHARACTERISTICS

(At recommended operating conditions unless otherwise noted.)

Parameter	Notes	Symbol	Condition	Value		Unit
				Min.	Max.	
Output High Voltage	*1	V_{OH}	$I_{OH} = -5.0 \text{ mA}$	2.4	—	V
Output Low Voltage	*1	V_{OL}	$I_{OL} = 4.2 \text{ mA}$	—	0.4	V
Input Leakage Current	$\overline{\text{RAS}}$	$I_{I(L)}$	$0 \text{ V} \leq V_{IN} \leq V_{CC}$, $4.5 \text{ V} \leq V_{CC} \leq 5.5 \text{ V}$, $V_{SS} = 0 \text{ V}$, All other pins not under test = 0 V	-30	30	μA
	$\overline{\text{CAS}}$			-20	20	
	Address, $\overline{\text{WE}}$			-60	60	
Output Leakage Current		$I_{O(L)}$	$0 \text{ V} \leq V_{OUT} \leq 5.5 \text{ V}$, Data out disabled	-10	10	μA
Operating Current (Average power supply current)	*2	I_{CC1}	$\overline{\text{RAS}}$ & $\overline{\text{CAS}}$ cycling, $t_{RC} = \text{min}$	—	840	mA
				—	720	
Standby Current (Power supply current)	TTL Level	I_{CC2}	$\overline{\text{RAS}} = \overline{\text{CAS}} = V_{IH}$ $\overline{\text{RAS}} = \overline{\text{CAS}} \geq V_{CC} - 0.2 \text{ V}$	—	16	mA
	CMOS Level			—	8	
Refresh Current#1 (Average power supply current)	*2	I_{CC3}	$\overline{\text{CAS}} = V_{IH}$, $\overline{\text{RAS}} = \text{cycling}$, $t_{RC} = \text{min}$	—	840	mA
				—	720	
Hyper Page Mode Current	*2	I_{CC4}	$\overline{\text{RAS}} = V_{IL}$, $\overline{\text{CAS}} = \text{cycling}$, $t_{HPC} = \text{min}$	—	720	mA
				—	640	
Refresh Current#2 (Average power supply current)	*2	I_{CC5}	$\overline{\text{RAS}}$ cycling, $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$, $t_{RC} = \text{min}$	—	840	mA
				—	720	

Notes: *1. Referenced to V_{SS} .

*2. I_{CC} depends on the output load conditions and cycle rate. The specific values are obtained with the output open.

I_{CC} depends on the number of address change as $\overline{\text{RAS}} = V_{IL}$ and $\overline{\text{CAS}} = V_{IH}$, $V_{IL} > -0.3 \text{ V}$.

I_{CC1} , I_{CC3} , I_{CC4} and I_{CC5} are specified at one time of address change during $\overline{\text{RAS}} = V_{IL}$ and $\overline{\text{CAS}} = V_{IH}$.

I_{CC2} is specified during $\overline{\text{RAS}} = V_{IH}$ and $V_{IL} > -0.3 \text{ V}$.

■ CAPACITANCE ($T_A = 25^\circ\text{C}$, $f = 1 \text{ MHz}$, $V_{CC} = 5.0 \text{ V}$)

Parameter	Symbol	Typ.	Max.	Unit
Input Capacitance, A0 to A10	C_{IN1}	—	71	pF
Input Capacitance, $\overline{\text{RAS}}0$ and $\overline{\text{RAS}}2$	C_{IN2}	—	39	pF
Input Capacitance, $\overline{\text{CAS}}0$ to $\overline{\text{CAS}}3$	C_{IN3}	—	23	pF
Input Capacitance, $\overline{\text{WE}}$	C_{IN4}	—	66	pF
I/O Capacitance, (DQ0-31)	C_{DQ}	—	12	pF

MB8504E032AA-60/-70

■ AC CHARACTERISTICS

(At recommended operating conditions unless otherwise noted.) Notes 1, 2, 3

No.	Parameter	Notes	Symbol	MB8504E032AA-60		MB8504E032AA-70		Unit
				Min.	Max.	Min.	Max.	
1	Time Between Refresh		t _{REF}	—	32.8	—	32.8	ms
2	Random Read/Write Cycle Time		t _{RC}	104	—	124	—	ns
3	Access Time from $\overline{\text{RAS}}$	*4,7	t _{RAC}	—	60	—	70	ns
4	Access Time from $\overline{\text{CAS}}$	*5,7	t _{CAC}	—	15	—	17	ns
5	Column Address Access Time	*6,7	t _{AA}	—	30	—	35	ns
6	Output Hold Time		t _{OH}	3	—	3	—	ns
7	Output Hold Time from $\overline{\text{CAS}}$		t _{CHC}	5	—	5	—	ns
8	Output Buffer Turn On Delay Time		t _{ON}	0	—	0	—	ns
9	Output Buffer Turn Off Delay Time	*8	t _{OFF}	—	15	—	17	ns
10	Output Buffer Turn Off Delay Time from $\overline{\text{RAS}}$	*8	t _{OFR}	—	15	—	17	ns
11	Output Buffer Turn Off Delay Time from $\overline{\text{WE}}$	*8	t _{WEZ}	—	15	—	17	ns
12	Transition Time		t _T	1	50	1	50	ns
13	$\overline{\text{RAS}}$ Precharge Time		t _{RP}	40	—	50	—	ns
14	$\overline{\text{RAS}}$ Pulse Width		t _{RAS}	60	100000	70	100000	ns
15	$\overline{\text{RAS}}$ Hold Time		t _{RSH}	15	—	17	—	ns
16	$\overline{\text{CAS}}$ to $\overline{\text{RAS}}$ Precharge Time		t _{CRP}	5	—	5	—	ns
17	$\overline{\text{CAS}}$ to $\overline{\text{RAS}}$ Delay Time	*9,10	t _{RCD}	14	45	14	53	ns
18	$\overline{\text{CAS}}$ Pulse Width		t _{CAS}	10	—	13	—	ns
19	$\overline{\text{CAS}}$ Hold Time		t _{CSH}	40	—	50	—	ns
20	$\overline{\text{CAS}}$ Precharge Time (Normal)	*15	t _{CPN}	10	—	10	—	ns
21	Row Address Set Up Time		t _{ASR}	0	—	0	—	ns
22	Row Address Hold Time		t _{RAH}	10	—	10	—	ns
23	Column Address Set Up Time		t _{ASC}	0	—	0	—	ns
24	Column Address Hold Time		t _{CAH}	10	—	10	—	ns
25	Column Address Hold Time from $\overline{\text{RAS}}$		t _{AR}	24	—	24	—	ns
26	$\overline{\text{RAS}}$ to Column Address Delay Time	*11	t _{RAD}	12	30	12	35	ns
27	Column Address to $\overline{\text{RAS}}$ Lead Time		t _{RAL}	30	—	35	—	ns
28	Column Address to $\overline{\text{CAS}}$ Lead Time		t _{CAL}	23	—	28	—	ns
29	Read Command Set Up Time		t _{RCS}	0	—	0	—	ns
30	Read Command Hold Time Referenced to $\overline{\text{RAS}}$	*12	t _{RRH}	0	—	0	—	ns
31	Read Command Hold Time Referenced to $\overline{\text{CAS}}$	*12	t _{RCH}	0	—	0	—	ns

(Continued)

MB8504E032AA-60/-70

(Continued)

No.	Parameter	Notes	Symbol	MB8504E032AA-60		MB8504E032AA-70		Unit
				Min.	Max.	Min.	Max.	
32	Write Command Set Up Time	*13	t _{WCS}	0	—	0	—	ns
33	Write Command Hold Time		t _{WCH}	10	—	10	—	ns
34	Write Command Hold Time from $\overline{\text{RAS}}$		t _{WCR}	24	—	24	—	ns
35	$\overline{\text{WE}}$ Pulse Width		t _{WTP}	10	—	10	—	ns
36	Write Command to $\overline{\text{RAS}}$ Lead Time		t _{RWL}	15	—	17	—	ns
37	Write Command to $\overline{\text{CAS}}$ Lead Time		t _{CWL}	10	—	13	—	ns
38	DIN Set Up Time		t _{DS}	0	—	0	—	ns
39	DIN Hold Time		t _{DH}	10	—	10	—	ns
40	Date Hold Time from $\overline{\text{RAS}}$		t _{DHR}	24	—	24	—	ns
41	$\overline{\text{RAS}}$ Precharge Time to $\overline{\text{CAS}}$ Active Time (Refresh Cycles)		t _{RPC}	5	—	5	—	ns
42	$\overline{\text{CAS}}$ Set Up Time (C-B-R Refresh)		t _{CSR}	0	—	0	—	ns
43	$\overline{\text{CAS}}$ Hold Time (C-B-R Refresh)		t _{CHR}	10	—	12	—	ns
44	$\overline{\text{WE}}$ Set Up Time from $\overline{\text{RAS}}$	*16	t _{WSR}	0	—	0	—	ns
45	$\overline{\text{WE}}$ Hold Time from $\overline{\text{RAS}}$	*16	t _{WHR}	10	—	10	—	ns
46	$\overline{\text{RAS}}$ to Data In Delay Time		t _{RDD}	15	—	17	—	ns
47	$\overline{\text{CAS}}$ to Data In Delay Time		t _{CDD}	15	—	17	—	ns
48	DIN to $\overline{\text{CAS}}$ Delay Time		t _{DZC}	0	—	0	—	ns
49	$\overline{\text{WE}}$ Precharge Time		t _{WPZ}	8	—	8	—	ns
50	$\overline{\text{WE}}$ to Data In Delay Time		t _{WED}	15	—	17	—	ns
51	Hyper Page Mode $\overline{\text{RAS}}$ Pulse Width		t _{RASP}	—	100000	—	100000	ns
52	Hyper Page Mode Read/Write Cycle Time		t _{HPC}	25	—	30	—	ns
53	Access Time from $\overline{\text{CAS}}$ Precharge	*7,14	t _{CPA}	—	35	—	40	ns
54	Hyper Page Mode $\overline{\text{CAS}}$ Precharge Time		t _{CP}	10	—	10	—	ns
55	Hyper Page Mode $\overline{\text{RAS}}$ Hold Time from $\overline{\text{CAS}}$ Precharge		t _{RHCP}	35	—	40	—	ns

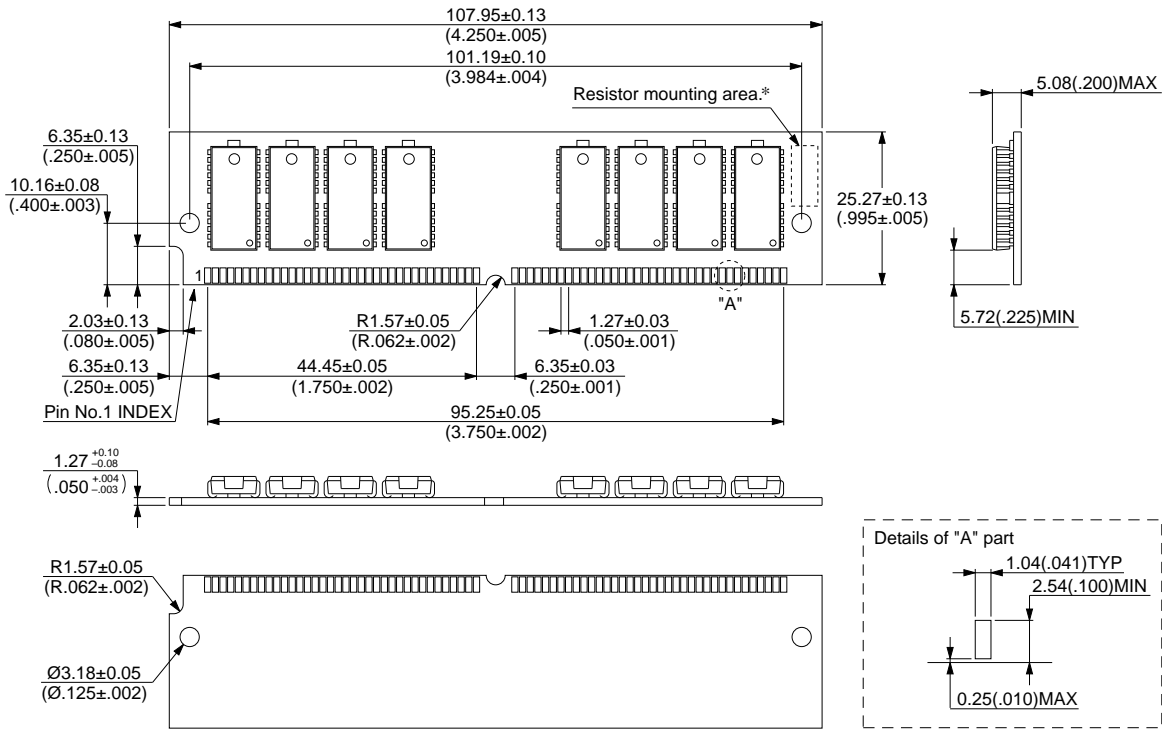
MB8504E032AA-60/-70

- Notes:**
- *1. An initial pause ($\overline{\text{RAS}} = \overline{\text{CAS}} = V_{\text{IH}}$) of 200 μs is required after power-up followed by any eight $\overline{\text{RAS}}$ -only cycles before proper device operation is achieved. If an internal refresh counter is used, a minimum of eight $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ initialization cycles are required instead of eight $\overline{\text{RAS}}$ cycles.
 - *2. AC characteristics assume $t_{\text{T}} = 5 \text{ ns}$.
 - *3. $V_{\text{IH}}(\text{min})$ and $V_{\text{IL}}(\text{max})$ are reference levels for measuring the timing of input signals. Transition times are measured between $V_{\text{IH}}(\text{min})$ and $V_{\text{IL}}(\text{max})$.
 - *4. Assumes that $t_{\text{RCD}} \leq t_{\text{RCD}}(\text{max})$, $t_{\text{RAD}} \leq t_{\text{RAD}}(\text{max})$. If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} will be increased by the amount that t_{RCD} exceeds the value shown.
 - *5. If $t_{\text{RCD}} \geq t_{\text{RCD}}(\text{max})$, $t_{\text{RAD}} \geq t_{\text{RAD}}(\text{max})$, and $t_{\text{ASC}} \geq t_{\text{AA}} - t_{\text{CAC}} - t_{\text{T}}$, access time is t_{CAC} .
 - *6. If $t_{\text{RAD}} \geq t_{\text{RAD}}(\text{max})$ and $t_{\text{ASC}} \geq t_{\text{AA}} - t_{\text{CAC}} - t_{\text{T}}$, access time is t_{AA} .
 - *7. Measured with a load equivalent to two TTL loads and 100 pF.
 - *8. t_{OFF} , t_{OFR} and t_{WEZ} are specified that output buffer change to high impedance state.
 - *9. Operation within the $t_{\text{RCD}}(\text{max})$ limit ensures that $t_{\text{RAC}}(\text{max})$ can be met. $t_{\text{RCD}}(\text{max})$ is specified as a reference point only; if t_{RCD} is greater than the specified $t_{\text{RCD}}(\text{max})$ limit, access time is controlled exclusively by t_{CAC} or t_{AA} .
 - *10. $t_{\text{RCD}}(\text{min}) = t_{\text{RAH}}(\text{min}) + 2 t_{\text{T}} + t_{\text{ASC}}(\text{min})$.
 - *11. Operation within the $t_{\text{RAD}}(\text{max})$ limit ensures that $t_{\text{RAC}}(\text{max})$ can be met. $t_{\text{RAD}}(\text{max})$ is specified as a reference point only; if t_{RAD} is greater than the specified $t_{\text{RAD}}(\text{max})$ limit, access time is controlled exclusively by t_{CAC} or t_{AA} .
 - *12. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.
 - *13. t_{WCS} is specified as a reference point only. If $t_{\text{WCS}} \geq t_{\text{WCS}}(\text{min})$ the data output pin will remain High-Z state through entire cycle.
 - *14. t_{CPA} is access time from the selection of a new column address (caused by changing $\overline{\text{CAS}}$ from "L" to "H"). Therefore, if t_{CP} become long, t_{CPA} also become longer than $t_{\text{CPA}}(\text{max})$.
 - *15. Assumes that $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh.
 - *16. Assumes that test mode function.
- *Source: See MB8117405A Data Sheet for details on the electricals.

MB8504E032AA-60/-70

■ PACKAGE DIMENSIONS

72-PAD PLASTIC SINGLE IN-LINE TYPE MODULE (CASE No.: MSS-72P-P77)

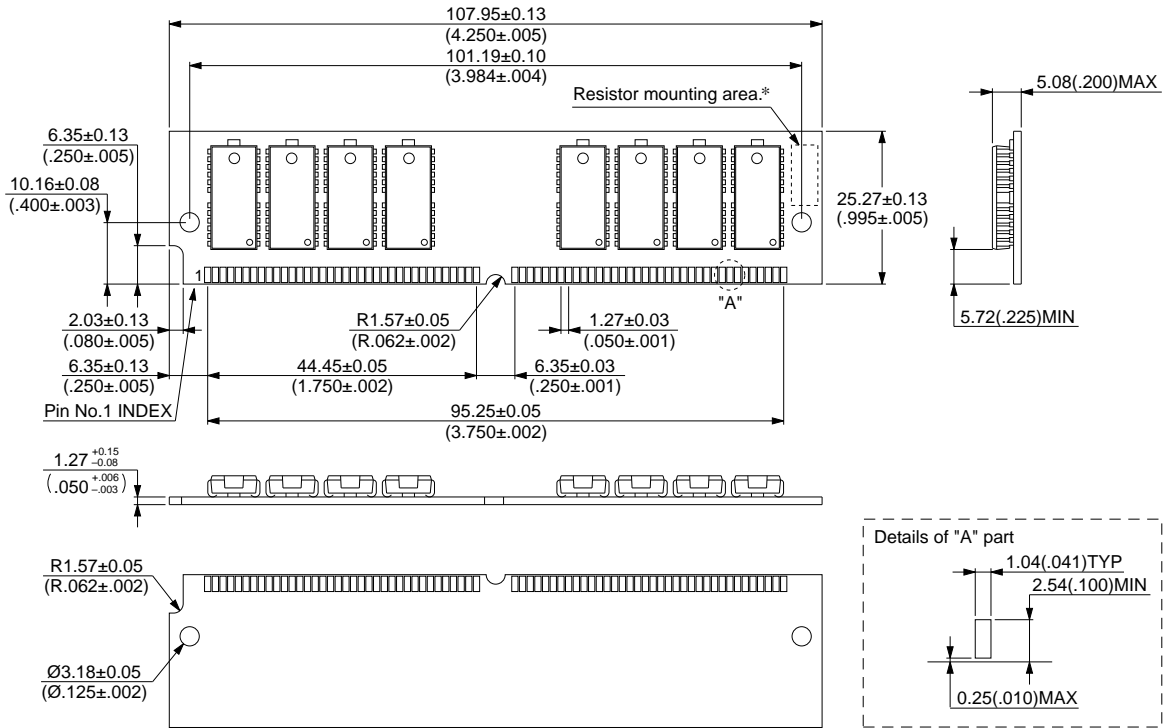


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Dimension in mm (inches)

MB8504E032AA-60/-70

72-PAD PLASTIC SINGLE IN-LINE TYPE MODULE (CASE No.: MSS-72P-P79)



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Dimension in mm (inches)

FUJITSU LIMITED

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