



***Z8 GP™ Microcontrollers***

## ***ZGP323H OTP MCU Family***

**Product Specification**

PS023803-0305



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## Revision History

Each instance in Table 1 reflects a change to this document from its previous revision. To see more detail, click the appropriate link in the table.

**Table 1. Revision History of this Document**

<b>Date</b>	<b>Revision Level</b>	<b>Section</b>	<b>Description</b>	<b>Page #</b>
December 2004	02		Changed low power consumption, STOP and HALT mode current values, deleted mask option note, clarified temperature ranges in Tables 6 and 8 and 10. Added new Tables 9 and 10. Also added Characterization data to Table 11 and changed Program/Erase Endurance value in Table 12.	1,2,10 11,12, 13,14, 15
			Removed Preliminary designation	All
March 2005	03		Minor change to Table 9 Electrical Characteristics. Added 20, 28 and 40-pin CDIP parts in the Ordering Section.	11,90



# Table of Contents

Revision History . . . . .	iii
Development Features . . . . .	1
General Description . . . . .	2
Pin Description . . . . .	4
Absolute Maximum Ratings . . . . .	10
Standard Test Conditions . . . . .	10
DC Characteristics . . . . .	11
AC Characteristics . . . . .	16
Pin Functions . . . . .	18
XTAL1 Crystal 1 (Time-Based Input) . . . . .	18
XTAL2 Crystal 2 (Time-Based Output) . . . . .	18
Port 0 (P07–P00) . . . . .	18
Port 1 (P17–P10) . . . . .	19
Port 2 (P27–P20) . . . . .	20
Port 3 (P37–P30) . . . . .	21
RESET (Input, Active Low) . . . . .	25
Functional Description . . . . .	25
Program Memory . . . . .	25
RAM . . . . .	25
Expanded Register File . . . . .	26
Register File . . . . .	30
Stack . . . . .	31
Timers . . . . .	32
Counter/Timer Functional Blocks . . . . .	40
Expanded Register File Control Registers (0D) . . . . .	66
Expanded Register File Control Registers (0F) . . . . .	71
Standard Control Registers . . . . .	75
Package Information . . . . .	81
Ordering Information . . . . .	90



# List of Figures

Figure 1.	Functional Block Diagram	3
Figure 2.	Counter/Timers Diagram	4
Figure 3.	20-Pin PDIP/SOIC/SSOP/CDIP* Pin Configuration	5
Figure 4.	28-Pin PDIP/SOIC/SSOP/CDIP* Pin Configuration	6
Figure 5.	40-Pin PDIP/CDIP* Pin Configuration	7
Figure 6.	48-Pin SSOP Pin Configuration	8
Figure 7.	Test Load Diagram	10
Figure 8.	AC Timing Diagram	16
Figure 9.	Port 0 Configuration	19
Figure 10.	Port 1 Configuration	20
Figure 11.	Port 2 Configuration	21
Figure 12.	Port 3 Configuration	22
Figure 13.	Port 3 Counter/Timer Output Configuration	24
Figure 14.	Program Memory Map (32K OTP)	26
Figure 15.	Expanded Register File Architecture	28
Figure 16.	Register Pointer	29
Figure 17.	Register Pointer—Detail	31
Figure 18.	Glitch Filter Circuitry	40
Figure 19.	Transmit Mode Flowchart	41
Figure 20.	8-Bit Counter/Timer Circuits	42
Figure 21.	T8_OUT in Single-Pass Mode	43
Figure 22.	T8_OUT in Modulo-N Mode	43
Figure 23.	Demodulation Mode Count Capture Flowchart	44
Figure 24.	Demodulation Mode Flowchart	45
Figure 25.	16-Bit Counter/Timer Circuits	46
Figure 26.	T16_OUT in Single-Pass Mode	47
Figure 27.	T16_OUT in Modulo-N Mode	47
Figure 28.	Ping-Pong Mode Diagram	49
Figure 29.	Output Circuit	49
Figure 30.	Interrupt Block Diagram	51
Figure 31.	Oscillator Configuration	53
Figure 32.	Port Configuration Register (PCON) (Write Only)	55
Figure 33.	STOP Mode Recovery Register	57



Figure 34. SCLK Circuit	58
Figure 35. Stop Mode Recovery Source	59
Figure 36. Stop Mode Recovery Register 2 ((0F)DH:D2–D4, D6 Write Only)	61
Figure 37. Watch-Dog Timer Mode Register (Write Only)	62
Figure 38. Resets and WDT	63
Figure 39. TC8 Control Register ((0D)00H: Read/Write Except Where Noted)	66
Figure 40. T8 and T16 Common Control Functions ((0D)01H: Read/Write)	67
Figure 41. T16 Control Register ((0D) 2H: Read/Write Except Where Noted)	69
Figure 42. T8/T16 Control Register (0D)03H: Read/Write (Except Where Noted)	70
Figure 43. Voltage Detection Register	71
Figure 44. Port Configuration Register (PCON)(0F)00H: Write Only	72
Figure 45. Stop Mode Recovery Register ((0F)0BH: D6–D0=Write Only, D7=Read Only)	73
Figure 46. Stop Mode Recovery Register 2 ((0F)0DH:D2–D4, D6 Write Only)	74
Figure 47. Watch-Dog Timer Register ((0F) 0FH: Write Only)	75
Figure 48. Port 2 Mode Register (F6H: Write Only)	75
Figure 49. Port 3 Mode Register (F7H: Write Only)	76
Figure 50. Port 0 and 1 Mode Register (F8H: Write Only)	77
Figure 51. Interrupt Priority Register (F9H: Write Only)	78
Figure 52. Interrupt Request Register (FAH: Read/Write)	79
Figure 53. Interrupt Mask Register (FBH: Read/Write)	79
Figure 54. Flag Register (FCH: Read/Write)	80
Figure 55. Register Pointer (FDH: Read/Write)	80
Figure 56. Stack Pointer High (FEH: Read/Write)	81
Figure 57. Stack Pointer Low (FFH: Read/Write)	81
Figure 58. 20-Pin CDIP Package	82
Figure 59. 20-Pin PDIP Package Diagram	82
Figure 60. 20-Pin SOIC Package Diagram	83
Figure 61. 20-Pin SSOP Package Diagram	84
Figure 62. 28-Pin SOIC Package Diagram	85
Figure 63. 28-Pin CDIP Package Diagram	86
Figure 64. 28-Pin PDIP Package Diagram	86
Figure 65. 28-Pin SSOP Package Diagram	87
Figure 66. 40-Pin PDIP Package Diagram	87
Figure 67. 40-Pin CDIP Package Diagram	88



Figure 68. 48-Pin SSOP Package Design ..... 89



## List of Tables

Table 1.	Revision History of this Document . . . . .	iii
Table 2.	Features . . . . .	1
Table 3.	Power Connections . . . . .	3
Table 4.	20-Pin PDIP/SOIC/SSOP/CDIP* Pin Identification . . . . .	5
Table 5.	28-Pin PDIP/SOIC/SSOP/CDIP* Pin Identification . . . . .	6
Table 6.	40- and 48-Pin Configuration . . . . .	8
Table 7.	Absolute Maximum Ratings . . . . .	10
Table 8.	Capacitance . . . . .	11
Table 9.	GP323HS DC Characteristics . . . . .	11
Table 10.	GP323HE DC Characteristics . . . . .	12
Table 11.	GP323HA DC Characteristics . . . . .	14
Table 12.	EPROM/OTP Characteristics . . . . .	15
Table 13.	AC Characteristics . . . . .	17
Table 14.	Port 3 Pin Function Summary. . . . .	23
Table 15.	CTR1(0D)01H T8 and T16 Common Functions. . . . .	35
Table 16.	Interrupt Types, Sources, and Vectors . . . . .	52
Table 17.	IRQ Register. . . . .	52
Table 18.	SMR2(F)0DH:Stop Mode Recovery Register 2* . . . . .	58
Table 19.	Stop Mode Recovery Source . . . . .	60
Table 20.	Watch-Dog Timer Time Select . . . . .	63
Table 21.	EPROM Selectable Options . . . . .	64





## Development Features

Table 2 lists the features of ZiLOG<sup>®</sup>'s ZGP323H members.

**Table 2. Features**

Device	OTP (KB)	RAM (Bytes)	I/O Lines	Voltage Range
ZGP323H OTP MCU Family	4, 8, 16, 32	237	32, 24 or 16	2.0V–5.5V

- Low power consumption—18mW (typical)
- T = Temperature  
S = Standard 0° to +70°C  
E = Extended -40° to +105°C  
A = Automotive -40° to +125°C
- Three standby modes:
  - STOP— (typical 1.8µA)
  - HALT— (typical 0.8mA)
  - Low voltage reset
- Special architecture to automate both generation and reception of complex pulses or signals:
  - One programmable 8-bit counter/timer with two capture registers and two load registers
  - One programmable 16-bit counter/timer with one 16-bit capture register pair and one 16-bit load register pair
  - Programmable input glitch filter for pulse reception
- Six priority interrupts
  - Three external
  - Two assigned to counter/timers
  - One low-voltage detection interrupt
- Low voltage detection and high voltage detection flags
- Programmable Watch-Dog Timer/Power-On Reset (WDT/POR) circuits
- Two independent comparators with programmable interrupt polarity
- Programmable EPROM options
  - Port 0: 0–3 pull-up transistors
  - Port 0: 4–7 pull-up transistors

- Port 1: 0–3 pull-up transistors
- Port 1: 4–7 pull-up transistors
- Port 2: 0–7 pull-up transistors
- EPROM Protection
- WDT enabled at POR

## General Description

The ZGP323H is an OTP-based member of the MCU family of infrared microcontrollers. With 237B of general-purpose RAM and up to 32KB of OTP, ZiLOG<sup>®</sup>'s CMOS microcontrollers offer fast-executing, efficient use of memory, sophisticated interrupts, input/output bit manipulation capabilities, automated pulse generation/reception, and internal key-scan pull-up transistors.

The ZGP323H architecture (Figure 1) is based on ZiLOG's 8-bit microcontroller core with an Expanded Register File allowing access to register-mapped peripherals, input/output (I/O) circuits, and powerful counter/timer circuitry. The Z8<sup>®</sup> offers a flexible I/O scheme, an efficient register and address space structure, and a number of ancillary features that are useful in many consumer, automotive, computer peripheral, and battery-operated hand-held applications.

There are three basic address spaces available to support a wide range of configurations: Program Memory, Register File and Expanded Register File. The register file is composed of 256 Bytes (B) of RAM. It includes 4 I/O port registers, 16 control and status registers, and 236 general-purpose registers. The Expanded Register File consists of two additional register groups (F and D).

To unburden the program from coping with such real-time problems as generating complex waveforms or receiving and demodulating complex waveform/pulses, the Z8 GP OTP offers a new intelligent counter/timer architecture with 8-bit and 16-bit counter/timers (see Figure 2). Also included are a large number of user-selectable modes and two on-board comparators to process analog signals with separate reference voltages.

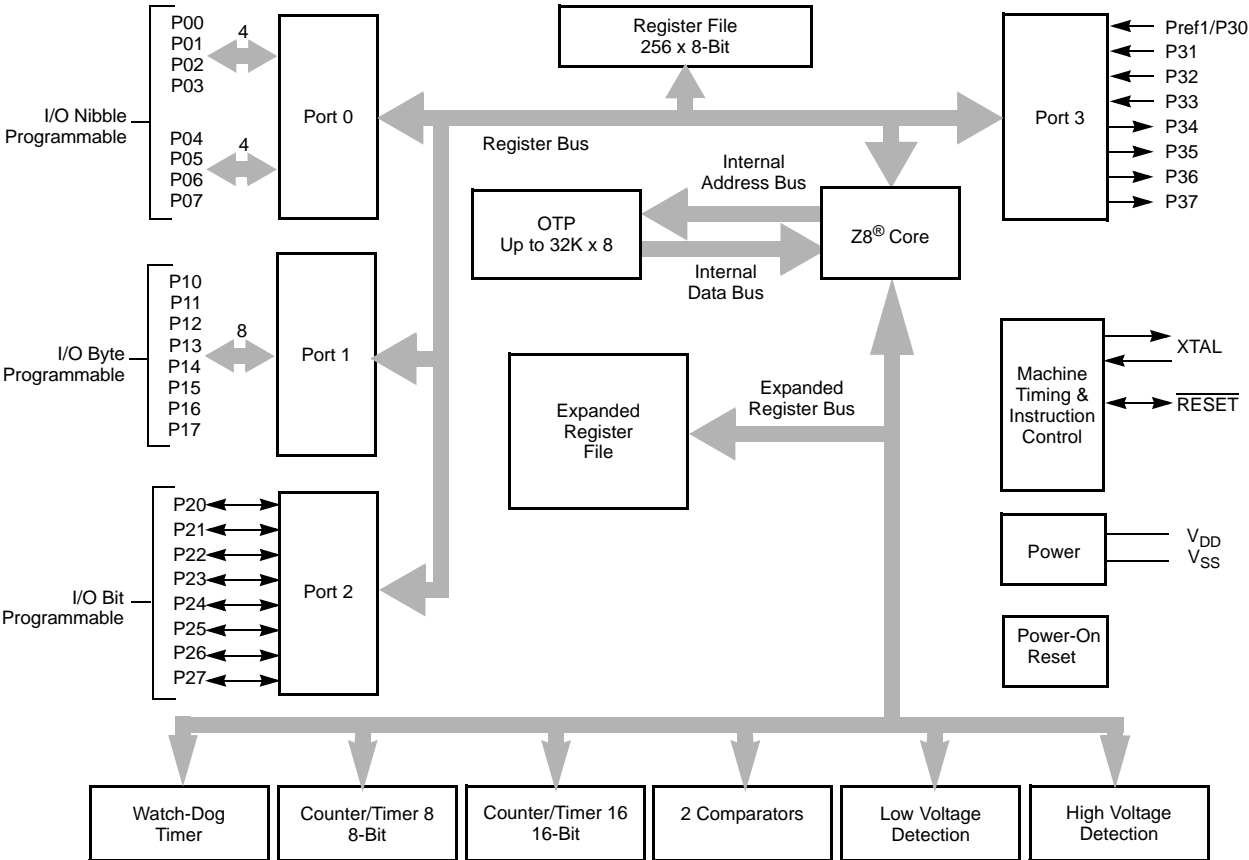
- **Note:** All signals with an overline, " $\bar{\quad}$ ", are active Low. For example,  $\overline{B/W}$ , in which WORD is active Low, and  $\overline{B/W}$ , in which BYTE is active Low.

Power connections use the conventional descriptions listed in Table 3.



**Table 3. Power Connections**

Connection	Circuit	Device
Power	V <sub>CC</sub>	V <sub>DD</sub>
Ground	GND	V <sub>SS</sub>



Note: Refer to the specific package for available pins.

**Figure 1. Functional Block Diagram**

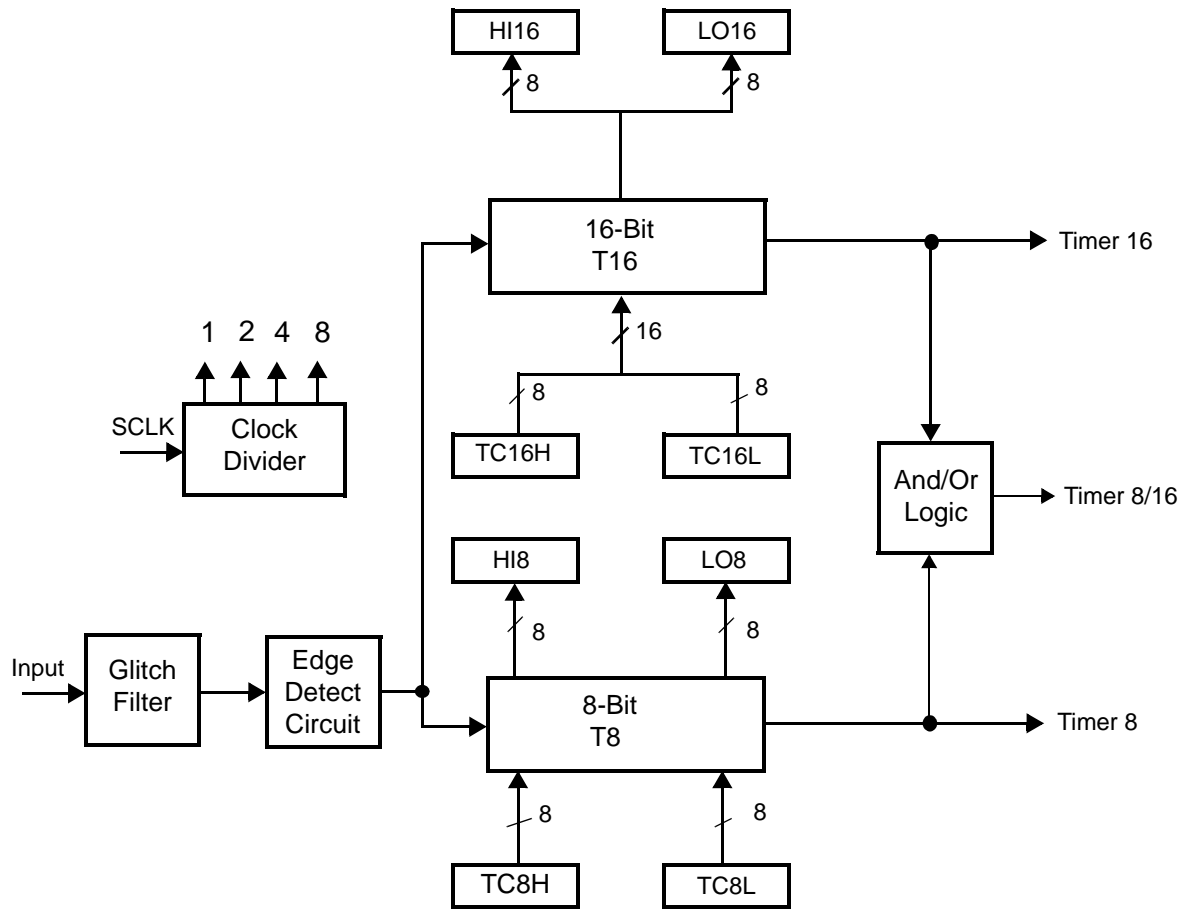


Figure 2. Counter/Timers Diagram

## Pin Description

The pin configuration for the 20-pin PDIP/SOIC/SSOP is illustrated in Figure 3 and described in Table 4. The pin configuration for the 28-pin PDIP/SOIC/SSOP are depicted in Figure 4 and described in Table 5. The pin configurations for the 40-pin PDIP and 48-pin SSOP versions are illustrated in Figure 5, Figure 6, and described in Table 6.

For customer engineering code development, a UV erasable windowed cerdip packaging is offered in 20-pin, 28-pin, and 40-pin configurations. ZiLOG does not recommend nor guarantee these packages for use in production.

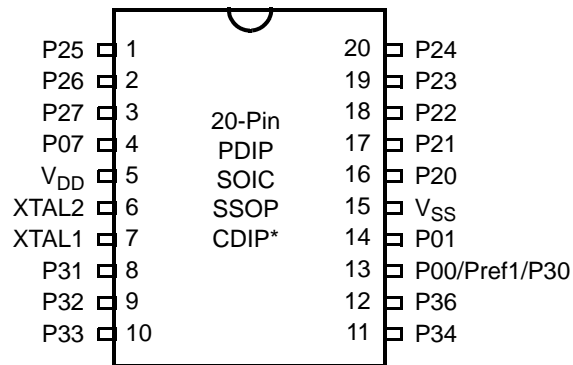


Figure 3. 20-Pin PDIP/SOIC/SSOP/CDIP\* Pin Configuration

Table 4. 20-Pin PDIP/SOIC/SSOP/CDIP\* Pin Identification

Pin #	Symbol	Function	Direction
1–3	P25–P27	Port 2, Bits 5,6,7	Input/Output
4	P07	Port 0, Bit 7	Input/Output
5	$V_{DD}$	Power Supply	
6	XTAL2	Crystal Oscillator Clock	Output
7	XTAL1	Crystal Oscillator Clock	Input
8–10	P31–P33	Port 3, Bits 1,2,3	Input
11,12	P34, P36	Port 3, Bits 4,6	Output
13	P00/Pref1/P30	Port 0, Bit 0/Analog reference input Port 3 Bit 0	Input/Output for P00 Input for Pref1/P30
14	P01	Port 0, Bit 1	Input/Output
15	$V_{SS}$	Ground	
16–20	P20–P24	Port 2, Bits 0,1,2,3,4	Input/Output

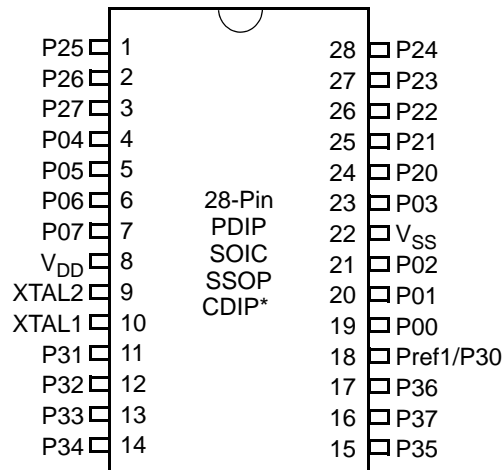


Figure 4. 28-Pin PDIP/SOIC/SSOP/CDIP\* Pin Configuration

Table 5. 28-Pin PDIP/SOIC/SSOP/CDIP\* Pin Identification

Pin	Symbol	Direction	Description
1-3	P25-P27	Input/Output	Port 2, Bits 5,6,7
4-7	P04-P07	Input/Output	Port 0, Bits 4,5,6,7
8	V <sub>DD</sub>		Power supply
9	XTAL2	Output	Crystal, oscillator clock
10	XTAL1	Input	Crystal, oscillator clock
11-13	P31-P33	Input	Port 3, Bits 1,2,3
14	P34	Output	Port 3, Bit 4
15	P35	Output	Port 3, Bit 5
16	P37	Output	Port 3, Bit 7
17	P36	Output	Port 3, Bit 6
18	Pref1/P30 Port 3 Bit 0	Input	Analog ref input; connect to V <sub>CC</sub> if not used Input for Pref1/P30
19-21	P00-P02	Input/Output	Port 0, Bits 0,1,2
22	V <sub>SS</sub>		Ground
23	P03	Input/Output	Port 0, Bit 3
24-28	P20-P24	Input/Output	Port 2, Bits 0-4

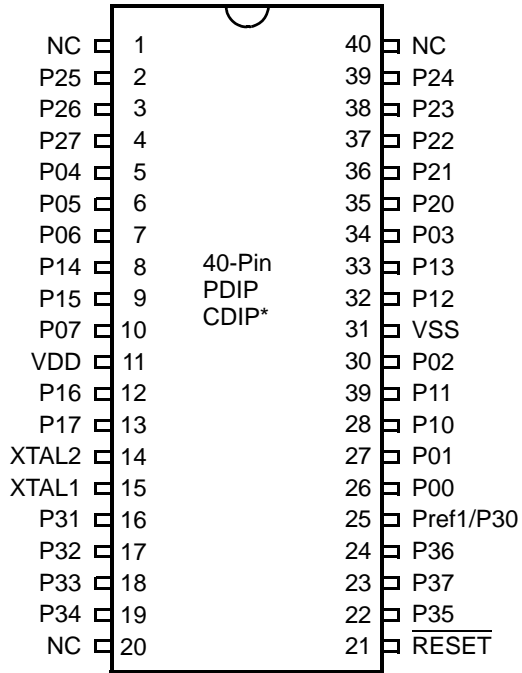


Figure 5. 40-Pin PDIP/CDIP\* Pin Configuration

► **Note:** \*Windowed Cerdip. These units are intended to be used for engineering code development only. ZiLOG does not recommend/guarantee this package for production use.

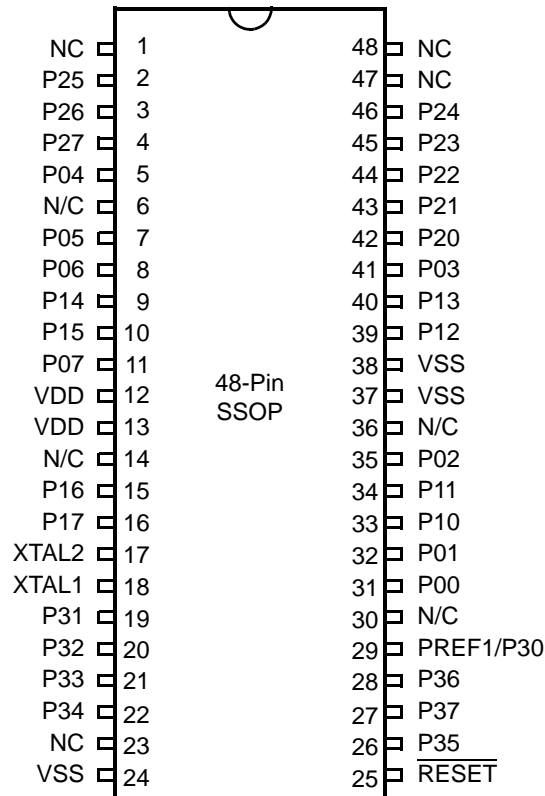


Figure 6. 48-Pin SSOP Pin Configuration

Table 6. 40- and 48-Pin Configuration

40-Pin PDIP #	48-Pin SSOP #	Symbol
26	31	P00
27	32	P01
30	35	P02
34	41	P03
5	5	P04
6	7	P05
7	8	P06
10	11	P07
28	33	P10
29	34	P11
32	39	P12





**Table 6. 40- and 48-Pin Configuration (Continued)**

40-Pin PDIP #	48-Pin SSOP #	Symbol
33	40	P13
8	9	P14
9	10	P15
12	15	P16
13	16	P17
35	42	P20
36	43	P21
37	44	P22
38	45	P23
39	46	P24
2	2	P25
3	3	P26
4	4	P27
16	19	P31
17	20	P32
18	21	P33
19	22	P34
22	26	P35
24	28	P36
23	27	P37
20	23	NC
40	47	NC
1	1	NC
21	25	RESET
15	18	XTAL1
14	17	XTAL2
11	12, 13	V <sub>DD</sub>
31	24, 37, 38	V <sub>SS</sub>
25	29	Pref1/P30
	48	NC
	6	NC
	14	NC
	30	NC
	36	NC

## Absolute Maximum Ratings

Stresses greater than those listed in Table 8 might cause permanent damage to the device. This rating is a stress rating only. Functional operation of the device at any condition above those indicated in the operational sections of these specifications is not implied. Exposure to absolute maximum rating conditions for an extended period might affect device reliability.

**Table 7. Absolute Maximum Ratings**

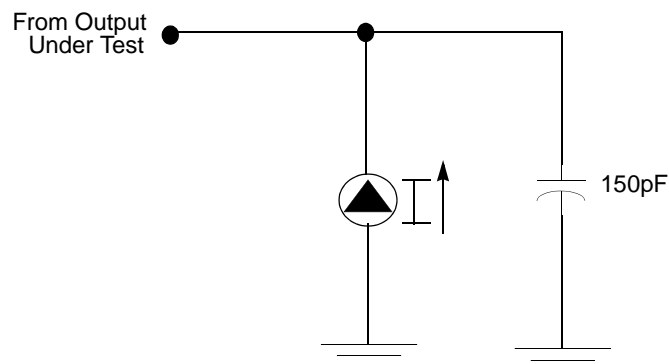
Parameter	Minimum	Maximum	Units	Notes
Ambient temperature under bias	-40	125	° C	1
Storage temperature	-65	+150	° C	
Voltage on any pin with respect to $V_{SS}$	-0.3	7.0	V	2
Voltage on $V_{DD}$ pin with respect to $V_{SS}$	-0.3	7.0	V	
Maximum current on input and/or inactive output pin	-5	+5	$\mu$ A	
Maximum output current from active output pin	-25	+25	mA	
Maximum current into $V_{DD}$ or out of $V_{SS}$		75	mA	

Notes:

1. See Ordering Information.
2. This voltage applies to all pins except the following:  $V_{DD}$ , P32, P33 and RESET.

## Standard Test Conditions

The characteristics listed in this product specification apply for standard test conditions as noted. All voltages are referenced to GND. Positive current flows into the referenced pin (see Figure 7).



**Figure 7. Test Load Diagram**

## Capacitance

Table 8 lists the capacitances.

**Table 8. Capacitance**

Parameter	Maximum
Input capacitance	12pF
Output capacitance	12pF
I/O capacitance	12pF

Note:  $T_A = 25^\circ\text{C}$ ,  $V_{CC} = \text{GND} = 0\text{V}$ ,  $f = 1.0\text{MHz}$ , unmeasured pins returned to GND

## DC Characteristics

**Table 9. GP323HS DC Characteristics**

Symbol	Parameter	$V_{CC}$	$T_A = 0^\circ\text{C to } +70^\circ\text{C}$			Units	Conditions	Notes
			Min	Typ(7)	Max			
$V_{CC}$	Supply Voltage		2.0		5.5	V	See Note 5	5
$V_{CH}$	Clock Input High Voltage	2.0-5.5	$0.8 V_{CC}$		$V_{CC}+0.3$	V	Driven by External Clock Generator	
$V_{CL}$	Clock Input Low Voltage	2.0-5.5	$V_{SS}-0.3$		0.4	V	Driven by External Clock Generator	
$V_{IH}$	Input High Voltage	2.0-5.5	$0.7 V_{CC}$		$V_{CC}+0.3$	V		
$V_{IL}$	Input Low Voltage	2.0-5.5	$V_{SS}-0.3$		$0.2 V_{CC}$	V		
$V_{OH1}$	Output High Voltage	2.0-5.5	$V_{CC}-0.4$			V	$I_{OH} = -0.5\text{mA}$	
$V_{OH2}$	Output High Voltage (P36, P37, P00, P01)	2.0-5.5	$V_{CC}-0.8$			V	$I_{OH} = -7\text{mA}$	
$V_{OL1}$	Output Low Voltage	2.0-5.5			0.4	V	$I_{OL} = 4.0\text{mA}$	
$V_{OL2}$	Output Low Voltage (P00, P01, P36, P37)	2.0-5.5			0.8	V	$I_{OL} = 10\text{mA}$	
$V_{OFFSET}$	Comparator Input Offset Voltage	2.0-5.5			25	mV		
$V_{REF}$	Comparator Reference Voltage	2.0-5.5	0		$V_{CC}$ 1.75	V		
$I_{IL}$	Input Leakage	2.0-5.5	-1		1	$\mu\text{A}$	$V_{IN} = 0\text{V}$ , $V_{CC}$ Pull-ups disabled	
$R_{PU}$	Pull-up Resistance	2.0V	225		675	$\text{K}\Omega$	$V_{IN} = 0\text{V}$ ; Pullups selected by mask option	
		3.6V	75		275	$\text{K}\Omega$		
		5.0V	40		160	$\text{K}\Omega$		

**Table 9. GP323HS DC Characteristics (Continued)**

Symbol	Parameter	V <sub>CC</sub>	T <sub>A</sub> =0°C to +70°C			Units	Conditions	Notes
			Min	Typ(7)	Max			
I <sub>OL</sub>	Output Leakage	2.0-5.5	-1		1	μA	V <sub>IN</sub> = 0V, V <sub>CC</sub>	
I <sub>CC</sub>	Supply Current	2.0V		1	3	mA	at 8.0 MHz	1, 2
		3.6V		5	10	mA	at 8.0 MHz	1, 2
		5.5V		10	15	mA	at 8.0 MHz	1, 2
I <sub>CC1</sub>	Standby Current (HALT Mode)	2.0V		0.5	1.6	mA	V <sub>IN</sub> = 0V, Clock at 8.0MHz	1, 2, 6
		3.6V		0.8	2.0	mA	V <sub>IN</sub> = 0V, Clock at 8.0MHz	1, 2, 6
		5.5V		1.3	3.2	mA	V <sub>IN</sub> = 0V, Clock at 8.0MHz	1, 2, 6
I <sub>CC2</sub>	Standby Current (Stop Mode)	2.0V		1.6	8	μA	V <sub>IN</sub> = 0 V, V <sub>CC</sub> WDT not Running	3
		3.6V		1.8	10	μA	V <sub>IN</sub> = 0 V, V <sub>CC</sub> WDT not Running	3
		5.5V		1.9	12	μA	V <sub>IN</sub> = 0 V, V <sub>CC</sub> WDT not Running	3
		2.0V		5	20	μA	V <sub>IN</sub> = 0 V, V <sub>CC</sub> WDT is Running	3
		3.6V		8	30	μA	V <sub>IN</sub> = 0 V, V <sub>CC</sub> WDT is Running	3
		5.5V		15	45	μA	V <sub>IN</sub> = 0 V, V <sub>CC</sub> WDT is Running	3
I <sub>LV</sub>	Standby Current (Low Voltage)			1.2	6	μA	Measured at 1.3V	4
V <sub>BO</sub>	V <sub>CC</sub> Low Voltage Protection			1.9	2.0	V	8MHz maximum Ext. CLK Freq.	
V <sub>LVD</sub>	V <sub>CC</sub> Low Voltage Detection			2.4		V		
V <sub>HVD</sub>	V <sub>CC</sub> High Voltage Detection			2.7		V		

**Notes:**

1. All outputs unloaded, inputs at rail.
2. CL1 = CL2 = 100 pF.
3. Oscillator stopped.
4. Oscillator stops when V<sub>CC</sub> falls below V<sub>BO</sub> limit.
5. It is strongly recommended to add a filter capacitor (minimum 0.1 μF), physically close to V<sub>CC</sub> and V<sub>SS</sub> pins if operating voltage fluctuations are anticipated, such as those resulting from driving an Infrared LED.
6. Comparator and Timers are on. Interrupt disabled.
7. Typical values shown are at 25 degrees C.

**Table 10. GP323HE DC Characteristics**

Symbol	Parameter	V <sub>CC</sub>	T <sub>A</sub> = -40°C to +105°C			Units	Conditions	Notes
			Min	Typ(7)	Max			
V <sub>CC</sub>	Supply Voltage		2.0		5.5	V	See Note 5	5
V <sub>CH</sub>	Clock Input High Voltage	2.0-5.5	0.8 V <sub>CC</sub>		V <sub>CC</sub> +0.3	V	Driven by External Clock Generator	
V <sub>CL</sub>	Clock Input Low Voltage	2.0-5.5	V <sub>SS</sub> -0.3		0.4	V	Driven by External Clock Generator	
V <sub>IH</sub>	Input High Voltage	2.0-5.5	0.7 V <sub>CC</sub>		V <sub>CC</sub> +0.3	V		
V <sub>IL</sub>	Input Low Voltage	2.0-5.5	V <sub>SS</sub> -0.3		0.2 V <sub>CC</sub>	V		
V <sub>OH1</sub>	Output High Voltage	2.0-5.5	V <sub>CC</sub> -0.4			V	I <sub>OH</sub> = -0.5mA	



Table 10. GP323HE DC Characteristics (Continued)

Symbol	Parameter	V <sub>CC</sub>	T <sub>A</sub> = -40°C to +105°C			Units	Conditions	Notes
			Min	Typ(7)	Max			
V <sub>OH2</sub>	Output High Voltage (P36, P37, P00, P01)	2.0-5.5	V <sub>CC</sub> -0.8			V	I <sub>OH</sub> = -7mA	
V <sub>OL1</sub>	Output Low Voltage	2.0-5.5			0.4	V	I <sub>OL</sub> = 4.0mA	
V <sub>OL2</sub>	Output Low Voltage (P00, P01, P36, P37)	2.0-5.5			0.8	V	I <sub>OL</sub> = 10mA	
V <sub>OFFSET</sub>	Comparator Input Offset Voltage	2.0-5.5			25	mV		
V <sub>REF</sub>	Comparator Reference Voltage	2.0-5.5	0		V <sub>DD</sub> -1.75	V		
I <sub>IL</sub>	Input Leakage	2.0-5.5	-1		1	μA	V <sub>IN</sub> = 0V, V <sub>CC</sub> Pull-ups disabled	
R <sub>PU</sub>	Pull-up Resistance	2.0V	200.0		700.0	KΩ	V <sub>IN</sub> = 0V; Pullups selected by mask option	
		3.6V	50.0		300.0	KΩ		
		5.0V	25.0		175.0	KΩ		
I <sub>OL</sub>	Output Leakage	2.0-5.5	-1		1	μA	V <sub>IN</sub> = 0V, V <sub>CC</sub>	
I <sub>CC</sub>	Supply Current	2.0V		1	3	mA	at 8.0 MHz	1, 2
		3.6V		5	10	mA	at 8.0 MHz	1, 2
		5.5V		10	15	mA	at 8.0 MHz	1, 2
I <sub>CC1</sub>	Standby Current (HALT Mode)	2.0V		0.5	1.6	mA	V <sub>IN</sub> = 0V, Clock at 8.0MHz	1, 2, 6
		3.6V		0.8	2.0	mA	V <sub>IN</sub> = 0V, Clock at 8.0MHz	1, 2, 6
		5.5V		1.3	3.2	mA	V <sub>IN</sub> = 0V, Clock at 8.0MHz	1, 2, 6
I <sub>CC2</sub>	Standby Current (Stop Mode)	2.0V		1.6	12	μA	V <sub>IN</sub> = 0 V, V <sub>CC</sub> WDT not Running	3
		3.6V		1.8	15	μA	V <sub>IN</sub> = 0 V, V <sub>CC</sub> WDT not Running	3
		5.5V		1.9	18	μA	V <sub>IN</sub> = 0 V, V <sub>CC</sub> WDT not Running	3
		2.0V		5	30	μA	V <sub>IN</sub> = 0 V, V <sub>CC</sub> WDT is Running	3
		3.6V		8	40	μA	V <sub>IN</sub> = 0 V, V <sub>CC</sub> WDT is Running	3
		5.5V		15	60	μA	V <sub>IN</sub> = 0 V, V <sub>CC</sub> WDT is Running	3
I <sub>LV</sub>	Standby Current (Low Voltage)			1.2	6	μA	Measured at 1.3V	4
V <sub>BO</sub>	V <sub>CC</sub> Low Voltage Protection			1.9	2.15	V	8MHz maximum Ext. CLK Freq.	
V <sub>LVD</sub>	V <sub>CC</sub> Low Voltage Detection			2.4		V		
V <sub>HVD</sub>	V <sub>CC</sub> High Voltage Detection			2.7		V		

**Notes:**

1. All outputs unloaded, inputs at rail.
2. CL1 = CL2 = 100 pF.
3. Oscillator stopped.
4. Oscillator stops when V<sub>CC</sub> falls below V<sub>BO</sub> limit.
5. It is strongly recommended to add a filter capacitor (minimum 0.1 μF), physically close to V<sub>CC</sub> and V<sub>SS</sub> pins if operating voltage fluctuations are anticipated, such as those resulting from driving an Infrared LED.
6. Comparator and Timers are on. Interrupt disabled.
7. Typical values shown are at 25 degrees C.

Table 11. GP323HA DC Characteristics

T <sub>A</sub> = -40°C to +125°C								
Symbol	Parameter	V <sub>CC</sub>	Min	Typ(7)	Max	Units	Conditions	Notes
V <sub>CC</sub>	Supply Voltage		2.0		5.5	V	See Note 5	5
V <sub>CH</sub>	Clock Input High Voltage	2.0-5.5	0.8 V <sub>CC</sub>		V <sub>CC</sub> +0.3	V	Driven by External Clock Generator	
V <sub>CL</sub>	Clock Input Low Voltage	2.0-5.5	V <sub>SS</sub> -0.3		0.4	V	Driven by External Clock Generator	
V <sub>IH</sub>	Input High Voltage	2.0-5.5	0.7 V <sub>CC</sub>		V <sub>CC</sub> +0.3	V		
V <sub>IL</sub>	Input Low Voltage	2.0-5.5	V <sub>SS</sub> -0.3		0.2 V <sub>CC</sub>	V		
V <sub>OH1</sub>	Output High Voltage	2.0-5.5	V <sub>CC</sub> -0.4			V	I <sub>OH</sub> = -0.5mA	
V <sub>OH2</sub>	Output High Voltage (P36, P37, P00, P01)	2.0-5.5	V <sub>CC</sub> -0.8			V	I <sub>OH</sub> = -7mA	
V <sub>OL1</sub>	Output Low Voltage	2.0-5.5			0.4	V	I <sub>OL</sub> = 4.0mA	
V <sub>OL2</sub>	Output Low Voltage (P00, P01, P36, P37)	2.0-5.5			0.8	V	I <sub>OL</sub> = 10mA	
V <sub>OFFSET</sub>	Comparator Input Offset Voltage	2.0-5.5			25	mV		
V <sub>REF</sub>	Comparator Reference Voltage	2.0-5.5	0		V <sub>DD</sub> -1.75	V		
I <sub>IL</sub>	Input Leakage	2.0-5.5	-1		1	μA	V <sub>IN</sub> = 0V, V <sub>CC</sub> Pull-ups disabled	
R <sub>PU</sub>	Pull-up Resistance	2.0V	200		700	KΩ	V <sub>IN</sub> = 0V; Pullups selected by mask option	
		3.6V	50		300	KΩ		
		5.0V	25		175	KΩ		
I <sub>OL</sub>	Output Leakage	2.0-5.5	-1		1	μA	V <sub>IN</sub> = 0V, V <sub>CC</sub>	
I <sub>CC</sub>	Supply Current	2.0V		1	3	mA	at 8.0 MHz	1, 2
		3.6V		5	10	mA	at 8.0 MHz	1, 2
		5.5V		10	15	mA	at 8.0 MHz	1, 2
I <sub>CC1</sub>	Standby Current (HALT Mode)	2.0V		0.5	1.6	mA	V <sub>IN</sub> = 0V, Clock at 8.0MHz	1, 2, 6
		3.6V		0.8	2.0	mA	V <sub>IN</sub> = 0V, Clock at 8.0MHz	1, 2, 6
		5.5V		1.3	3.2	mA	V <sub>IN</sub> = 0V, Clock at 8.0MHz	1, 2, 6
I <sub>CC2</sub>	Standby Current (Stop Mode)	2.0V		1.6	15	μA	V <sub>IN</sub> = 0 V, V <sub>CC</sub> WDT not Running	3
		3.6V		1.8	20	μA	V <sub>IN</sub> = 0 V, V <sub>CC</sub> WDT not Running	3
		5.5V		1.9	25	μA	V <sub>IN</sub> = 0 V, V <sub>CC</sub> WDT not Running	3
		2.0V		5	30	μA	V <sub>IN</sub> = 0 V, V <sub>CC</sub> WDT is Running	3
		3.6V		8	40	μA	V <sub>IN</sub> = 0 V, V <sub>CC</sub> WDT is Running	3
		5.5V		15	60	μA	V <sub>IN</sub> = 0 V, V <sub>CC</sub> WDT is Running	3
I <sub>LV</sub>	Standby Current (Low Voltage)			1.2	6	μA	Measured at 1.3V	4
V <sub>BO</sub>	V <sub>CC</sub> Low Voltage Protection			1.9	2.15	V	8MHz maximum Ext. CLK Freq.	
V <sub>LVD</sub>	V <sub>CC</sub> Low Voltage Detection			2.4		V		



**Table 11. GP323HA DC Characteristics (Continued)**

Symbol	Parameter	V <sub>CC</sub>	T <sub>A</sub> = -40°C to +125°C			Units	Conditions	Notes
			Min	Typ(7)	Max			
V <sub>HVD</sub>	V <sub>CC</sub> High Voltage Detection			2.7		V		

**Notes:**

1. All outputs unloaded, inputs at rail.
2. CL1 = CL2 = 100 pF.
3. Oscillator stopped.
4. Oscillator stops when V<sub>CC</sub> falls below V<sub>BO</sub> limit.
5. It is strongly recommended to add a filter capacitor (minimum 0.1 μF), physically close to V<sub>CC</sub> and V<sub>SS</sub> pins if operating voltage fluctuations are anticipated, such as those resulting from driving an Infrared LED.
6. Comparator and Timers are on. Interrupt disabled.
7. Typical values shown are at 25 degrees C.

**Table 12. EPROM/OTP Characteristics**

Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
	Erase Time	15			Minutes	1,3
	Data Retention @ use years		10		Years	2
	Program/Erase Endurance	100			Cycles	1

**Notes:**

1. For windowed cerdip package only.
2. Standard: 0°C to 70°C; Extended: -40°C to +105°C; Automotive: -40°C to +125°C. Determined using the Arrhenius model, which is an industry standard for estimating data retention of floating gate technologies:

$$AF = \exp[(Ea/k) * (1/T_{use} - 1/T_{stress})]$$

Where:

Ea is the intrinsic activation energy (eV; typ. 0.8)

k is Boltzman's constant (8.67 x 10<sup>-5</sup> eV/°K)

°K = -273.16°C

T<sub>use</sub> = Use Temperature in °K

T<sub>stress</sub> = Stress Temperature in °K

3. At a stable UV Lamp output of 20mW/CM<sup>2</sup>

# AC Characteristics

Figure 8 and Table 13 describe the Alternating Current (AC) characteristics.

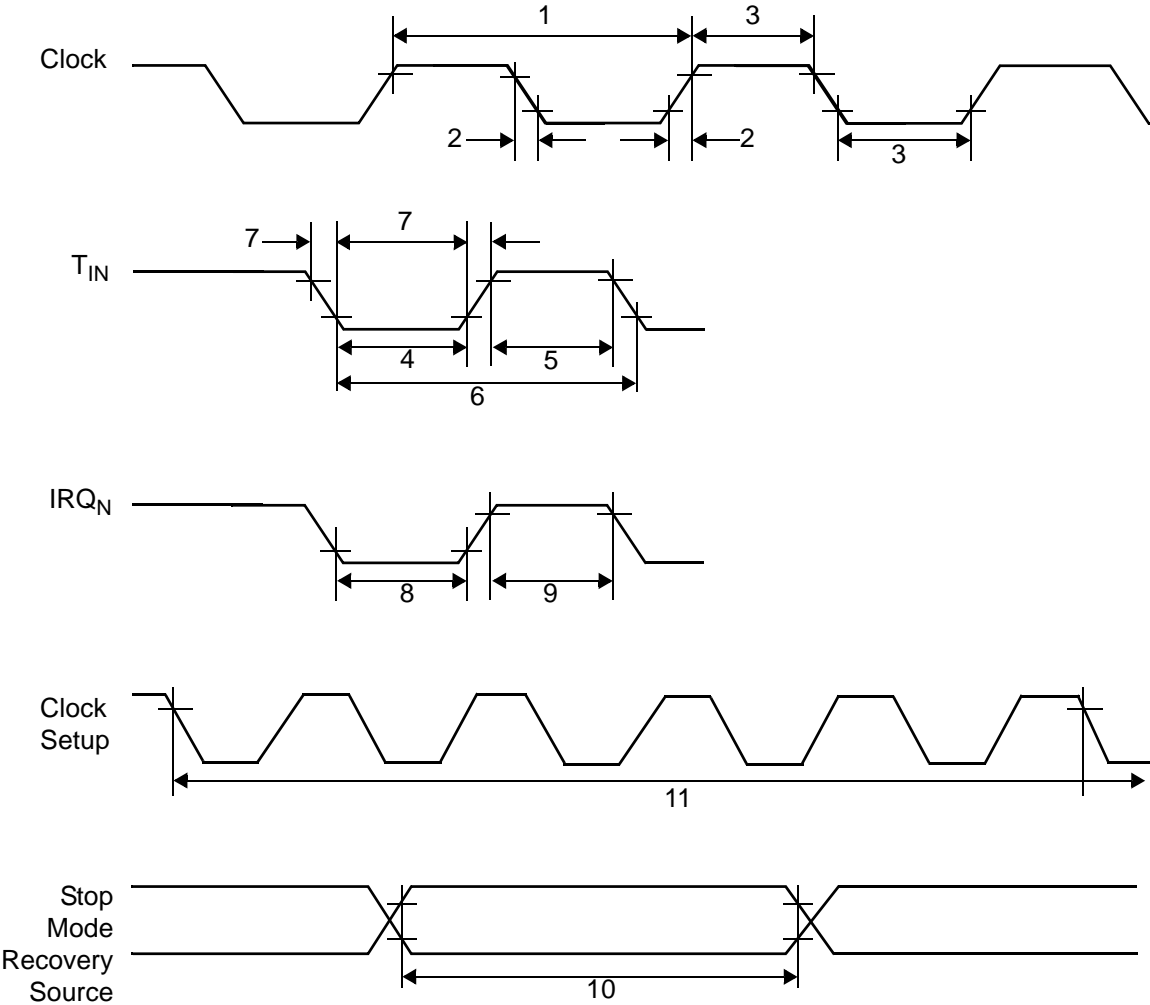


Figure 8. AC Timing Diagram





Table 13. AC Characteristics

No	Symbol	Parameter	V <sub>CC</sub>	T <sub>A</sub> =0°C to +70°C (S) -40°C to +105°C (E) -40°C to +125°C (A) 8.0MHz		Units	Notes	Watch-Dog Timer Mode Register (D1, D0)
				Minimum	Maximum			
1	T <sub>pC</sub>	Input Clock Period	2.0–5.5	121	DC	ns	1	
2	TrC, TfC	Clock Input Rise and Fall Times	2.0–5.5		25	ns	1	
3	T <sub>wC</sub>	Input Clock Width	2.0–5.5	37		ns	1	
4	T <sub>wTinL</sub>	Timer Input Low Width	2.0 5.5	100 70		ns	1	
5	T <sub>wTinH</sub>	Timer Input High Width	2.0–5.5	3T <sub>pC</sub>			1	
6	T <sub>pTin</sub>	Timer Input Period	2.0–5.5	8T <sub>pC</sub>			1	
7	TrTin, TfTin	Timer Input Rise and Fall Timers	2.0–5.5		100	ns	1	
8	T <sub>wIL</sub>	Interrupt Request Low Time	2.0 5.5	100 70		ns	1, 2	
9	T <sub>wIH</sub>	Interrupt Request Input High Time	2.0–5.5	5T <sub>pC</sub>			1, 2	
10	T <sub>wsm</sub>	Stop-Mode Recovery Width Spec	2.0–5.5	12 5T <sub>pC</sub>		ns	3 4	
11	T <sub>ost</sub>	Oscillator Start-Up Time	2.0–5.5		5T <sub>pC</sub>		4	
12	T <sub>wdt</sub>	Watch-Dog Timer Delay Time	2.0–5.5 2.0–5.5 2.0–5.5 2.0–5.5	5 10 20 80		ms ms ms ms	0, 0 0, 1 1, 0 1, 1	
13	T <sub>POR</sub>	Power-On Reset	2.0–5.5	2.5	10	ms		

Notes:

1. Timing Reference uses 0.9 V<sub>CC</sub> for a logic 1 and 0.1 V<sub>CC</sub> for a logic 0.
2. Interrupt request through Port 3 (P33–P31).
3. SMR – D5 = 1.
4. SMR – D5 = 0.

## Pin Functions

### XTAL1 Crystal 1 (Time-Based Input)

This pin connects a parallel-resonant crystal or ceramic resonator to the on-chip oscillator input. Additionally, an optional external single-phase clock can be coded to the on-chip oscillator input.

### XTAL2 Crystal 2 (Time-Based Output)

This pin connects a parallel-resonant crystal or ceramic resonant to the on-chip oscillator output.

### Port 0 (P07–P00)

Port 0 is an 8-bit, bidirectional, CMOS-compatible port. These eight I/O lines are configured under software control as a nibble I/O port. The output drivers are push-pull or open-drain controlled by bit D2 in the PCON register.

If one or both nibbles are needed for I/O operation, they must be configured by writing to the Port 0 mode register. After a hardware reset, Port 0 is configured as an input port.

An optional pull-up transistor is available as a mask option on all Port 0 bits with nibble select.

- **Notes:** Internal pull-ups are disabled on any given pin or group of port pins when programmed into output mode.

The Port 0 direction is reset to its default state following an SMR.

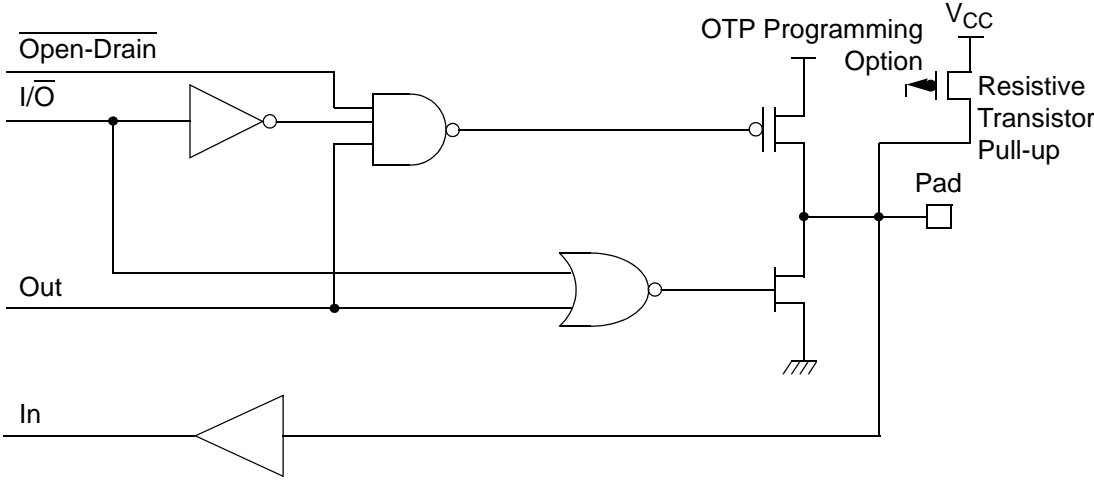
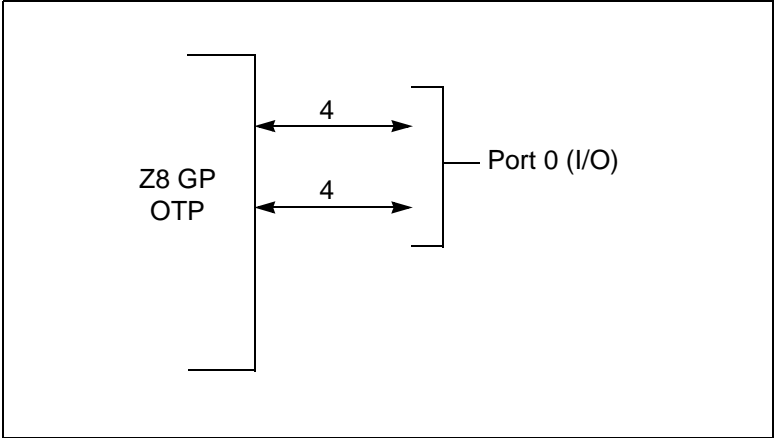


Figure 9. Port 0 Configuration

**Port 1 (P17–P10)**

Port 1 (see Figure 10) Port 1 can be configured for standard port input or output mode. After POR, Port 1 is configured as an input port. The output drivers are either push-pull or open-drain and are controlled by bit D1 in the PCON register.

► **Note:** The Port 1 direction is reset to its default state following an SMR.

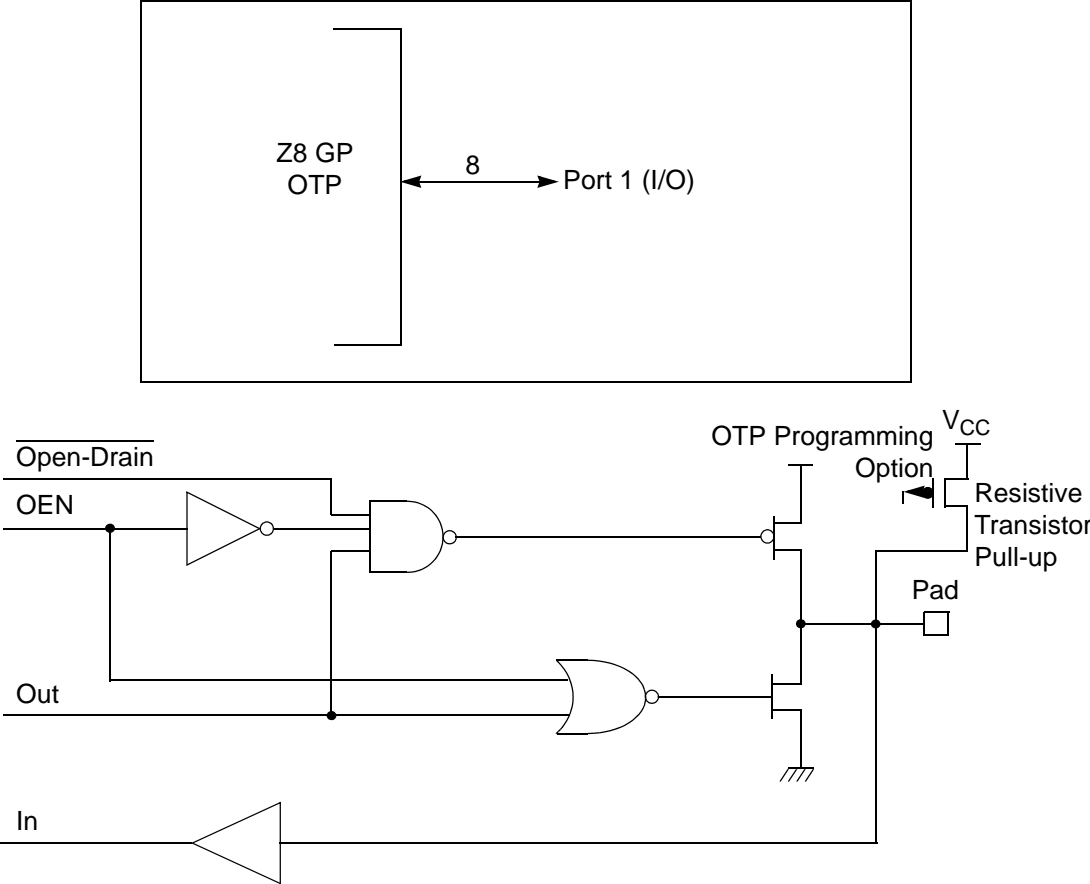


Figure 10. Port 1 Configuration

**Port 2 (P27–P20)**

Port 2 is an 8-bit, bidirectional, CMOS-compatible I/O port (see Figure 11). These eight I/O lines can be independently configured under software control as inputs or outputs. Port 2 is always available for I/O operation. A mask option is available to connect eight pull-up transistors on this port. Bits programmed as outputs are globally programmed as either push-pull or open-drain. The POR resets with the eight bits of Port 2 configured as inputs.

Port 2 also has an 8-bit input OR and AND gate, which can be used to wake up the part. P20 can be programmed to access the edge-detection circuitry in demodulation mode.

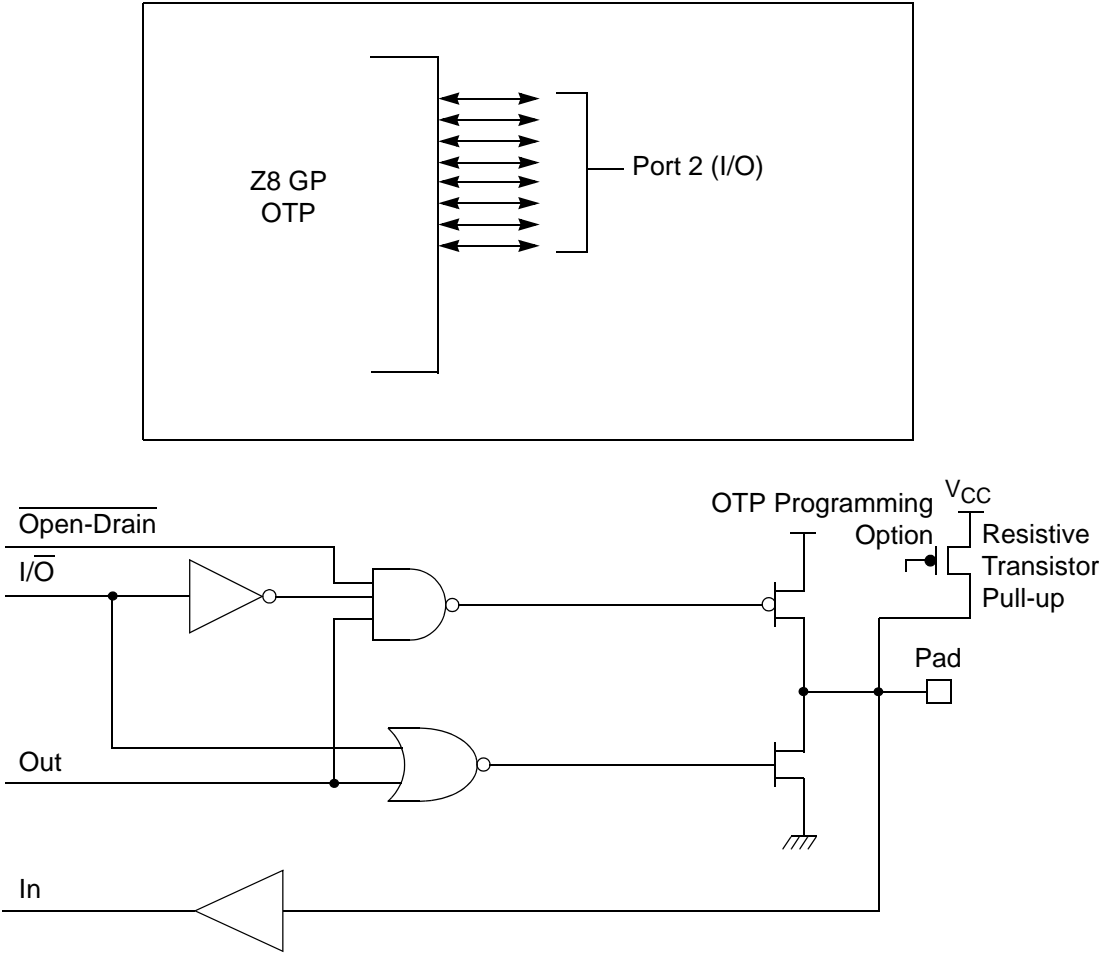
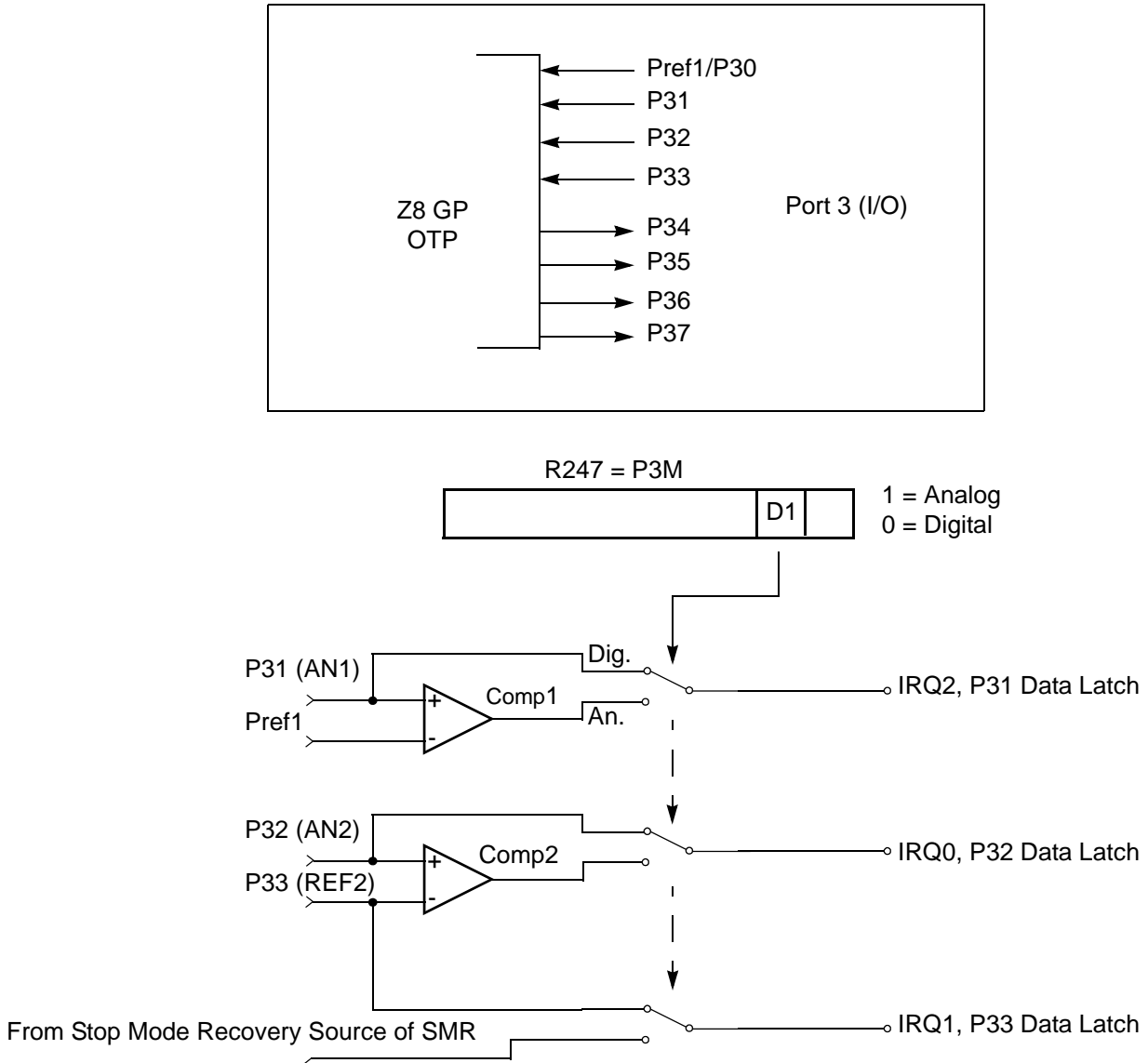


Figure 11. Port 2 Configuration

**Port 3 (P37–P30)**

Port 3 is a 8-bit, CMOS-compatible fixed I/O port (see Figure 12). Port 3 consists of four fixed input (P33–P30) and four fixed output (P37–P34), which can be configured under software control for interrupt and as output from the counter/timers. P30, P31, P32, and P33 are standard CMOS inputs; P34, P35, P36, and P37 are push-pull outputs.



**Figure 12. Port 3 Configuration**

Two on-board comparators process analog signals on P31 and P32, with reference to the voltage on Pref1 and P33. The analog function is enabled by programming the Port 3 Mode Register (bit 1). P31 and P32 are programmable as rising, falling, or both edge triggered interrupts (IRQ register bits 6 and 7). Pref1 and P33 are the comparator reference voltage inputs. Access to the Counter Timer edge-detection circuit is through P31 or P20 (see “T8 and T16 Common Functions—



CTR1(0D)01H” on page 35). Other edge detect and IRQ modes are described in Table 14.

- ▶ **Note:** Comparators are powered down by entering Stop Mode. For P31–P33 to be used in a Stop Mode Recovery (SMR) source, these inputs must be placed into digital mode.

**Table 14. Port 3 Pin Function Summary**

Pin	I/O	Counter/Timers	Comparator	Interrupt
Pref1/P30	IN		RF1	
P31	IN	IN	AN1	IRQ2
P32	IN		AN2	IRQ0
P33	IN		RF2	IRQ1
P34	OUT	T8	AO1	
P35	OUT	T16		
P36	OUT	T8/16		
P37	OUT		AO2	
P20	I/O	IN		

Port 3 also provides output for each of the counter/timers and the AND/OR Logic (see Figure 13). Control is performed by programming bits D5–D4 of CTR1, bit 0 of CTR0, and bit 0 of CTR2.

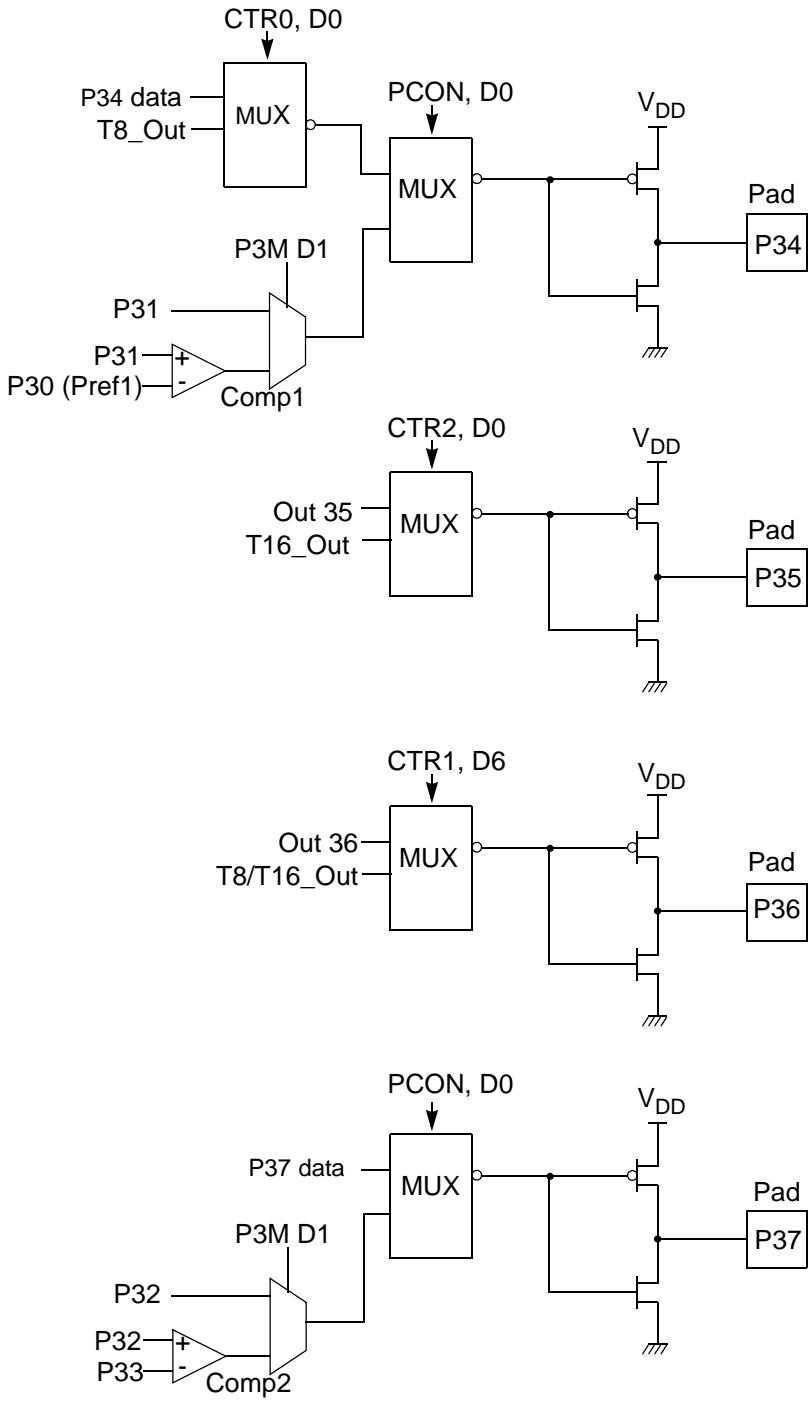


Figure 13. Port 3 Counter/Timer Output Configuration





### Comparator Inputs

In analog mode, P31 and P32 have a comparator front end. The comparator reference is supplied to P33 and Pref1. In this mode, the P33 internal data latch and its corresponding IRQ1 are diverted to the SMR sources (excluding P31, P32, and P33) as indicated in Figure 12 on page 22. In digital mode, P33 is used as D3 of the Port 3 input register, which then generates IRQ1.

- ▶ **Note:** Comparators are powered down by entering Stop Mode. For P31–P33 to be used in a Stop Mode Recovery source, these inputs must be placed into digital mode.

### Comparator Outputs

These channels can be programmed to be output on P34 and P37 through the PCON register.

## RESET (Input, Active Low)

Reset initializes the MCU and is accomplished either through Power-On, Watch-Dog Timer, Stop Mode Recovery, Low-Voltage detection, or external reset. During Power-On Reset and Watch-Dog Timer Reset, the internally generated reset drives the reset pin Low for the POR time. Any devices driving the external reset line must be open-drain to avoid damage from a possible conflict during reset conditions. Pull-up is provided internally.

When the Z8 GP asserts (Low) the RESET pin, the internal pull-up is disabled. The Z8 GP does not assert the RESET pin when under VBO.

- ▶ **Note:** The external Reset does not initiate an exit from STOP mode.

## Functional Description

This device incorporates special functions to enhance the Z8<sup>®</sup> functionality in consumer and battery-operated applications.

### Program Memory

This device addresses up to 32KB of OTP memory. The first 12 Bytes are reserved for interrupt vectors. These locations contain the six 16-bit vectors that correspond to the six available interrupts.

### RAM

This device features 256B of RAM. See Figure 14.

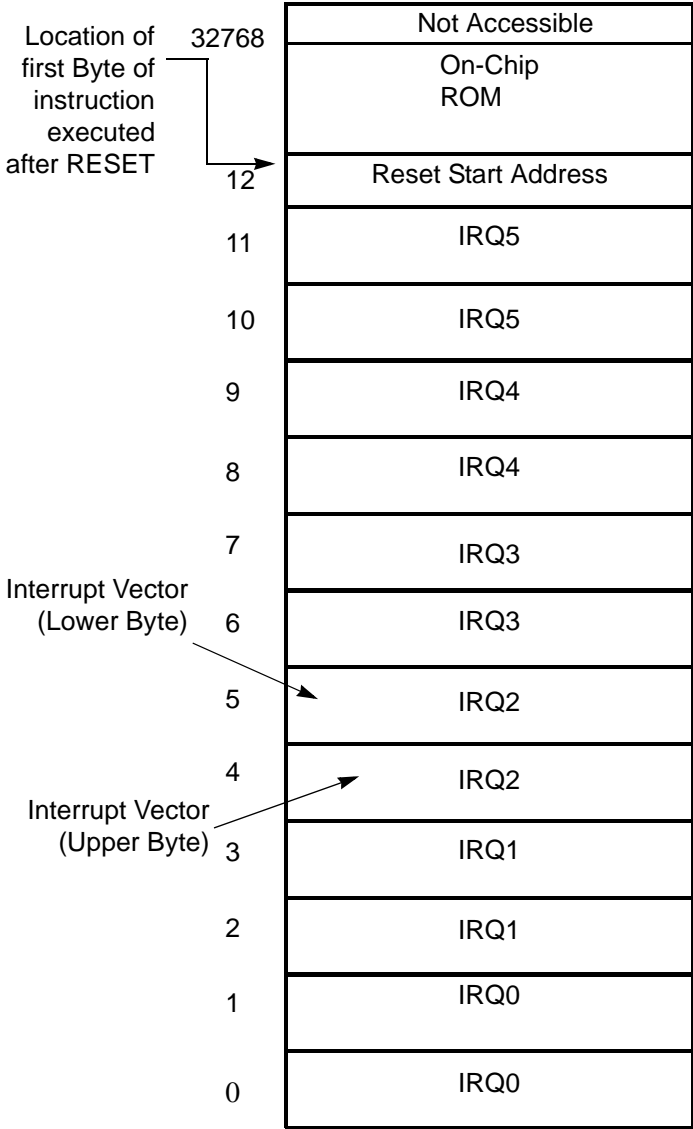


Figure 14. Program Memory Map (32K OTP)

### Expanded Register File

The register file has been expanded to allow for additional system control registers and for mapping of additional peripheral devices into the register address area. The Z8<sup>®</sup> register address space (R0 through R15) has been implemented as 16 banks, with 16 registers per bank. These register groups are known as the



ERF (Expanded Register File). Bits 7–4 of register RP select the working register group. Bits 3–0 of register RP select the expanded register file bank.

- ▶ **Note:** An expanded register bank is also referred to as an expanded register group (see Figure 15).





The upper nibble of the register pointer (see Figure 16) selects which working register group, of 16 bytes in the register file, is accessed out of the possible 256. The lower nibble selects the expanded register file bank and, in the case of the Z8 GP family, banks 0, F, and D are implemented. A 0H in the lower nibble allows the normal register file (bank 0) to be addressed. Any other value from 1H to FH exchanges the lower 16 registers to an expanded register bank.

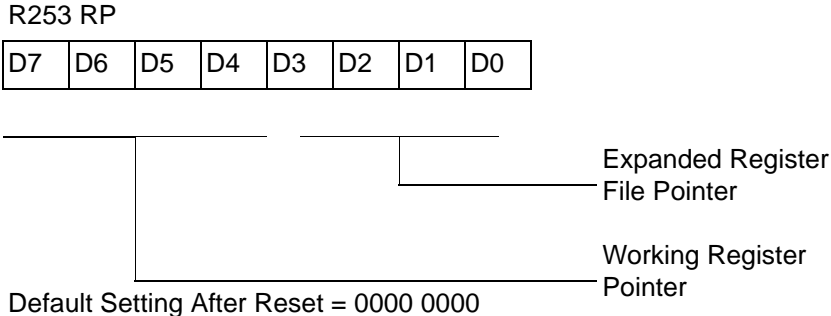


Figure 16. Register Pointer

Example: Z8 GP: (See Figure 15 on page 28)

R253 RP = 00h  
R0 = Port 0  
R1 = Port 1  
R2 = Port 2  
R3 = Port 3

But if:

R253 RP = 0Dh  
R0 = CTR0  
R1 = CTR1  
R2 = CTR2  
R3 = Reserved

The counter/timers are mapped into ERF group D. Access is easily performed using the following:

```

LD          RP, #0Dh          ; Select ERF D
for access to bank D

                                ; (working
register group 0)
LD          R0, #xx          ; load CTR0
LD          1, #xx          ; load CTR1
LD          R1, 2            ; CTR2→CTR1

LD          RP, #0Dh          ; Select ERF D
for access to bank D

                                ; (working
register group 0)
LD          RP, #7Dh          ; Select
expanded register bank D and working ; register
group 7 of bank 0 for access.
LD          71h, 2           ; CTRL2→register 71h
; CTRL2→register 71h
LD          R1, 2            ; CTRL2→register 71h
; CTRL2→register 71h

```

## Register File

The register file (bank 0) consists of 4 I/O port registers, 237 general-purpose registers, 16 control and status registers (R0–R3, R4–R239, and R240–R255, respectively), and two expanded registers groups in Banks D (see Table 15) and F. Instructions can access registers directly or indirectly through an 8-bit address field, thereby allowing a short, 4-bit register address to use the Register Pointer (Figure 17). In the 4-bit mode, the register file is divided into 16 working register groups, each occupying 16 continuous locations. The Register Pointer addresses the starting location of the active working register group.

- ▶ **Note:** Working register group E0–EF can only be accessed through working registers and indirect addressing modes.

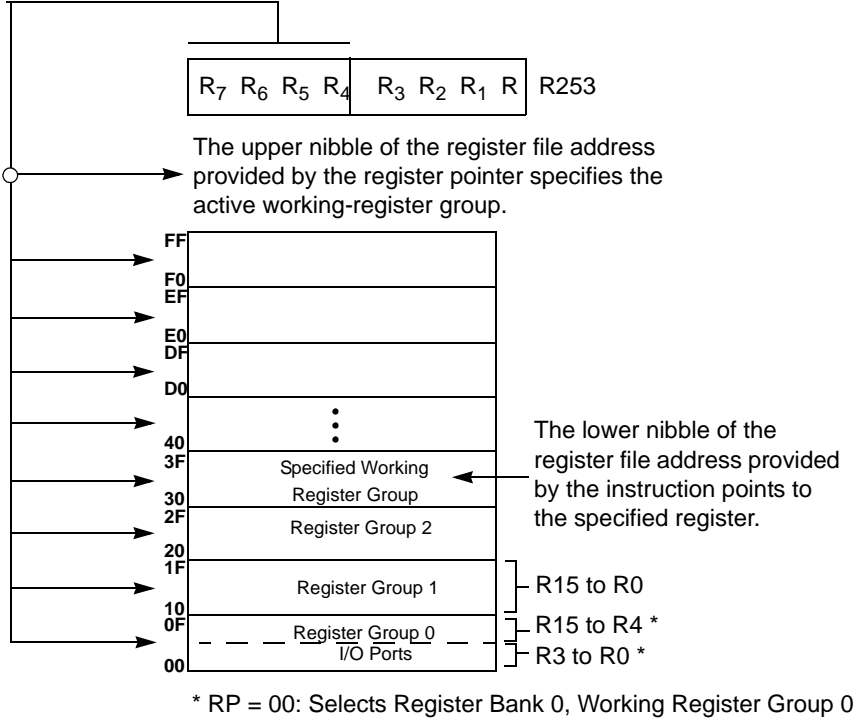


Figure 17. Register Pointer—Detail

**Stack**

The internal register file is used for the stack. An 8-bit Stack Pointer SPL (R255) is used for the internal stack that resides in the general-purpose registers (R4–R239). SPH (R254) can be used as a general-purpose register.



## Timers

### T8\_Capture\_HI—HI8(D)0BH

This register holds the captured data from the output of the 8-bit Counter/Timer0. Typically, this register holds the number of counts when the input signal is 1.

Field	Bit Position		Description
T8_Capture_HI	[7:0]	R/W	Captured Data - No Effect

### T8\_Capture\_LO—L08(D)0AH

This register holds the captured data from the output of the 8-bit Counter/Timer0. Typically, this register holds the number of counts when the input signal is 0.

Field	Bit Position		Description
T8_Capture_LO	[7:0]	R/W	Captured Data - No Effect

### T16\_Capture\_HI—HI16(D)09H

This register holds the captured data from the output of the 16-bit Counter/Timer16. This register holds the MS-Byte of the data.

Field	Bit Position		Description
T16_Capture_HI	[7:0]	R/W	Captured Data - No Effect

### T16\_Capture\_LO—L016(D)08H

This register holds the captured data from the output of the 16-bit Counter/Timer16. This register holds the LS-Byte of the data.

Field	Bit Position		Description
T16_Capture_LO	[7:0]	R/W	Captured Data - No Effect

### Counter/Timer2 MS-Byte Hold Register—TC16H(D)07H

Field	Bit Position		Description
T16_Data_HI	[7:0]	R/W	Data





### Counter/Timer2 LS-Byte Hold Register—TC16L(D)06H

Field	Bit Position		Description
T16_Data_LO	[7:0]	R/W	Data

### Counter/Timer8 High Hold Register—TC8H(D)05H

Field	Bit Position		Description
T8_Level_HI	[7:0]	R/W	Data

### Counter/Timer8 Low Hold Register—TC8L(D)04H

Field	Bit Position		Description
T8_Level_LO	[7:0]	R/W	Data

### CTR0 Counter/Timer8 Control Register—CTR0(D)00H

Table 15 lists and briefly describes the fields for this register.

**Table 15. CTR0(D)00H Counter/Timer8 Control Register**

Field	Bit Position		Value	Description
T8_Enable	7-----	R/W	0*	Counter Disabled
			1	Counter Enabled
			0	Stop Counter
			1	Enable Counter
Single/Modulo-N	-6-----	R/W	0*	Modulo-N
			1	Single Pass
Time_Out	--5-----	R/W	0**	No Counter Time-Out
			1	Counter Time-Out Occurred
			0	No Effect
			1	Reset Flag to 0
T8_Clock	---43---	R/W	0 0**	SCLK
			0 1	SCLK/2
			1 0	SCLK/4
			1 1	SCLK/8
Capture_INT_Mask	----2--	R/W	0**	Disable Data Capture Interrupt
			1	Enable Data Capture Interrupt



**Table 15. CTR0(D)00H Counter/Timer8 Control Register (Continued)**

Field	Bit Position		Value	Description
Counter_INT_Mask	-----1-	R/W	0**	Disable Time-Out Interrupt
			1	Enable Time-Out Interrupt
P34_Out	-----0	R/W	0*	P34 as Port Output
			1	T8 Output on P34

**Note:**

\*Indicates the value upon Power-On Reset.

\*\*Indicates the value upon Power-On Reset. Not reset with a Stop Mode recovery.

**T8 Enable**

This field enables T8 when set (written) to 1.

**Single/Modulo-N**

When set to 0 (Modulo-N), the counter reloads the initial value when the terminal count is reached. When set to 1 (single-pass), the counter stops when the terminal count is reached.

**Timeout**

This bit is set when T8 times out (terminal count reached). To reset this bit, write a 1 to its location.



**Caution:** Writing a 1 is the only way to reset the Terminal Count status condition. Reset this bit before using/enabling the counter/timers.

The first clock of T8 might not have complete clock width and can occur any time when enabled.



**Note:** Take care when using the OR or AND commands to manipulate CTR0, bit 5 and CTR1, bits 0 and 1 (Demodulation Mode). These instructions use a Read-Modify-Write sequence in which the current status from the CTR0 and CTR1 registers is ORed or ANDed with the designated value and then written back into the registers.

**T8 Clock**

This bit defines the frequency of the input signal to T8.



### Capture\_INT\_Mask

Set this bit to allow an interrupt when data is captured into either LO8 or HI8 upon a positive or negative edge detection in demodulation mode.

### Counter\_INT\_Mask

Set this bit to allow an interrupt when T8 has a timeout.

### P34\_Out

This bit defines whether P34 is used as a normal output pin or the T8 output.

### T8 and T16 Common Functions—CTR1(0D)01H

This register controls the functions in common with the T8 and T16.

Table 16 lists and briefly describes the fields for this register.

**Table 16. CTR1(0D)01H T8 and T16 Common Functions**

Field	Bit Position		Value	Description
Mode	7-----	R/W	0*	Transmit Mode Demodulation Mode
P36_Out/ Demodulator_Input	-6-----	R/W	0* 1 0* 1	Transmit Mode Port Output T8/T16 Output Demodulation Mode P31 P20
T8/T16_Logic/ Edge_Detect	--54----	R/W	00** 01 10 11 00** 01 10 11	Transmit Mode AND OR NOR NAND Demodulation Mode Falling Edge Rising Edge Both Edges Reserved



**Table 16. CTR1(0D)01H T8 and T16 Common Functions (Continued)**

Field	Bit Position		Value	Description
Transmit_Submode/ Glitch_Filter	----32--	R/W	00*	Transmit Mode
			01	Normal Operation
		R	10	Ping-Pong Mode
			11	T16_Out = 0
		W	00*	T16_Out = 1
			01	Demodulation Mode
		R	10	No Filter
			11	4 SCLK Cycle
				8 SCLK Cycle
				Reserved
Initial_T8_Out/ Rising Edge	-----1-	R/W	0*	Transmit Mode
			1	T8_OUT is 0 Initially
		R	0*	T8_OUT is 1 Initially
			1	Demodulation Mode
		W	0	No Rising Edge
			1	Rising Edge Detected
		R	0	No Effect
			1	Reset Flag to 0
Initial_T16_Out/ Falling_Edge	-----0	R/W	0*	Transmit Mode
			1	T16_OUT is 0 Initially
		R	0*	T16_OUT is 1 Initially
			1	Demodulation Mode
		W	0	No Falling Edge
			1	Falling Edge Detected
		R	0	No Effect
			1	Reset Flag to 0

**Note:**

\*Default at Power-On Reset

\*Default at Power-On Reset. Not reset with Stop Mode recovery.

**Mode**

If the result is 0, the counter/timers are in TRANSMIT mode; otherwise, they are in DEMODULATION mode.

**P36\_Out/Demodulator\_Input**

In TRANSMIT Mode, this bit defines whether P36 is used as a normal output pin or the combined output of T8 and T16.

In DEMODULATION Mode, this bit defines whether the input signal to the Counter/Timers is from P20 or P31.

If the input signal is from Port 31, a capture event may also generate an IRQ2 interrupt. To prevent generating an IRQ2, either disable the IRQ2 interrupt by clearing its IMR bit D2 or use P20 as the input.

### T8/T16\_Logic/Edge \_Detect

In TRANSMIT Mode, this field defines how the outputs of T8 and T16 are combined (AND, OR, NOR, NAND).

In DEMODULATION Mode, this field defines which edge should be detected by the edge detector.

### Transmit\_Submode/Glitch Filter

In Transmit Mode, this field defines whether T8 and T16 are in the PING-PONG mode or in independent normal operation mode. Setting this field to “NORMAL OPERATION Mode” terminates the “PING-PONG Mode” operation. When set to 10, T16 is immediately forced to a 0; a setting of 11 forces T16 to output a 1.

In DEMODULATION Mode, this field defines the width of the glitch that must be filtered out.

### Initial\_T8\_Out/Rising\_Edge

In TRANSMIT Mode, if 0, the output of T8 is set to 0 when it starts to count. If 1, the output of T8 is set to 1 when it starts to count. When the counter is not enabled and this bit is set to 1 or 0, T8\_OUT is set to the opposite state of this bit. This ensures that when the clock is enabled, a transition occurs to the initial state set by CTR1, D1.

In DEMODULATION Mode, this bit is set to 1 when a rising edge is detected in the input signal. In order to reset the mode, a 1 should be written to this location.

### Initial\_T16 Out/Falling \_Edge

In TRANSMIT Mode, if it is 0, the output of T16 is set to 0 when it starts to count. If it is 1, the output of T16 is set to 1 when it starts to count. This bit is effective only in Normal or PING-PONG Mode (CTR1, D3; D2). When the counter is not enabled and this bit is set, T16\_OUT is set to the opposite state of this bit. This ensures that when the clock is enabled, a transition occurs to the initial state set by CTR1, D0.

In DEMODULATION Mode, this bit is set to 1 when a falling edge is detected in the input signal. In order to reset it, a 1 should be written to this location.

- **Note:** Modifying CTR1 (D1 or D0) while the counters are enabled causes unpredictable output from T8/T16\_OUT.

### CTR2 Counter/Timer 16 Control Register—CTR2(D)02H

Table 17 lists and briefly describes the fields for this register.



**Table 17. CTR2(D)02H: Counter/Timer16 Control Register**

Field	Bit Position		Value	Description	
T16_Enable	7-----	R	0*	Counter Disabled	
			1	Counter Enabled	
		W	0	Stop Counter	
			1	Enable Counter	
Single/Modulo-N	-6-----	R/W	0*	Transmit Mode	
			1	Modulo-N	
				Single Pass	
			0	Demodulation Mode	
Time_Out	--5-----	R	0*	T16 Recognizes Edge	
			1	T16 Does Not Recognize Edge	
			W	0	No Counter Timeout
				1	Counter Timeout Occurred
T16_Clock	---43---	R/W	00**	No Effect	
			01	Reset Flag to 0	
			10	SCLK	
			11	SCLK/2	
Capture_INT_Mask	-----2--	R/W	0**	SCLK/4	
			1	SCLK/8	
Counter_INT_Mask	-----1-	R/W	0*	Disable Data Capture Int.	
				1	Enable Data Capture Int.
P35_Out	-----0	R/W	0*	Disable Timeout Int.	
				1	Enable Timeout Int.

**Note:**

\*Indicates the value upon Power-On Reset.

\*\*Indicates the value upon Power-On Reset. Not reset with a Stop Mode recovery.

**T16\_Enable**

This field enables T16 when set to 1.

**Single/Modulo-N**

In TRANSMIT Mode, when set to 0, the counter reloads the initial value when it reaches the terminal count. When set to 1, the counter stops when the terminal count is reached.



In Demodulation Mode, when set to 0, T16 captures and reloads on detection of all the edges. When set to 1, T16 captures and detects on the first edge but ignores the subsequent edges. For details, see the description of T16 Demodulation Mode on page 47.

#### Time\_Out

This bit is set when T16 times out (terminal count reached). To reset the bit, write a 1 to this location.

#### T16\_Clock

This bit defines the frequency of the input signal to Counter/Timer16.

#### Capture\_INT\_Mask

This bit is set to allow an interrupt when data is captured into LO16 and HI16.

#### Counter\_INT\_Mask

Set this bit to allow an interrupt when T16 times out.

#### P35\_Out

This bit defines whether P35 is used as a normal output pin or T16 output.

### CTR3 T8/T16 Control Register—CTR3(D)03H

Table 18 lists and briefly describes the fields for this register. This register allows the T<sub>8</sub> and T<sub>16</sub> counters to be synchronized.

**Table 18. CTR3 (D)03H: T8/T16 Control Register**

Field	Bit Position		Value	Description
T <sub>16</sub> Enable	7-----	R	0*	Counter Disabled
		R	1	Counter Enabled
		W	0	Stop Counter
		W	1	Enable Counter
T <sub>8</sub> Enable	-6-----	R	0*	Counter Disabled
		R	1	Counter Enabled
		W	0	Stop Counter
		W	1	Enable Counter
Sync Mode	--5-----	R/W	0**	Disable Sync Mode
			1	Enable Sync Mode

**Table 18. CTR3 (D)03H: T8/T16 Control Register (Continued)**

Field	Bit Position		Value	Description
Reserved	---43210	R	1	Always reads 11111
		W	x	No Effect

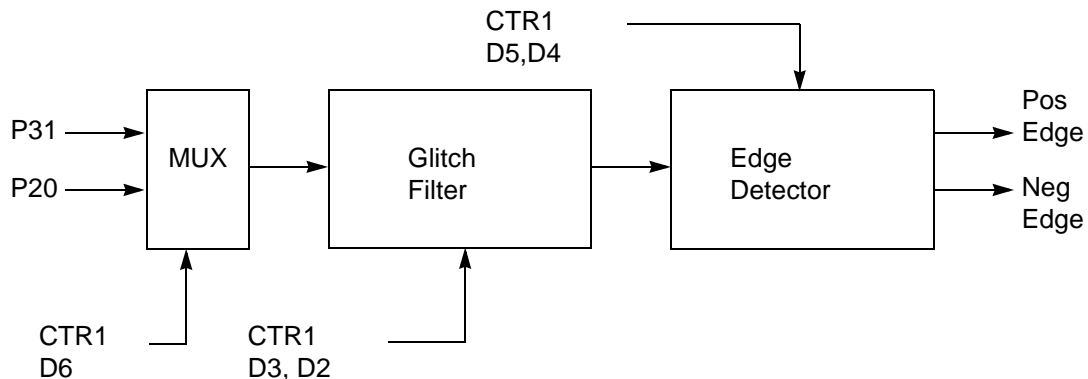
\*Indicates the value upon Power-On Reset.

\*\*Indicates the value upon Power-On Reset. Not reset with a Stop Mode recovery.

## Counter/Timer Functional Blocks

### Input Circuit

The edge detector monitors the input signal on P31 or P20. Based on CTR1 D5–D4, a pulse is generated at the Pos Edge or Neg Edge line when an edge is detected. Glitches in the input signal that have a width less than specified (CTR1 D3, D2) are filtered out (see Figure 18).



**Figure 18. Glitch Filter Circuitry**

### T8 Transmit Mode

Before T8 is enabled, the output of T8 depends on CTR1, D1. If it is 0, T8\_OUT is 1; if it is 1, T8\_OUT is 0. See Figure 19.



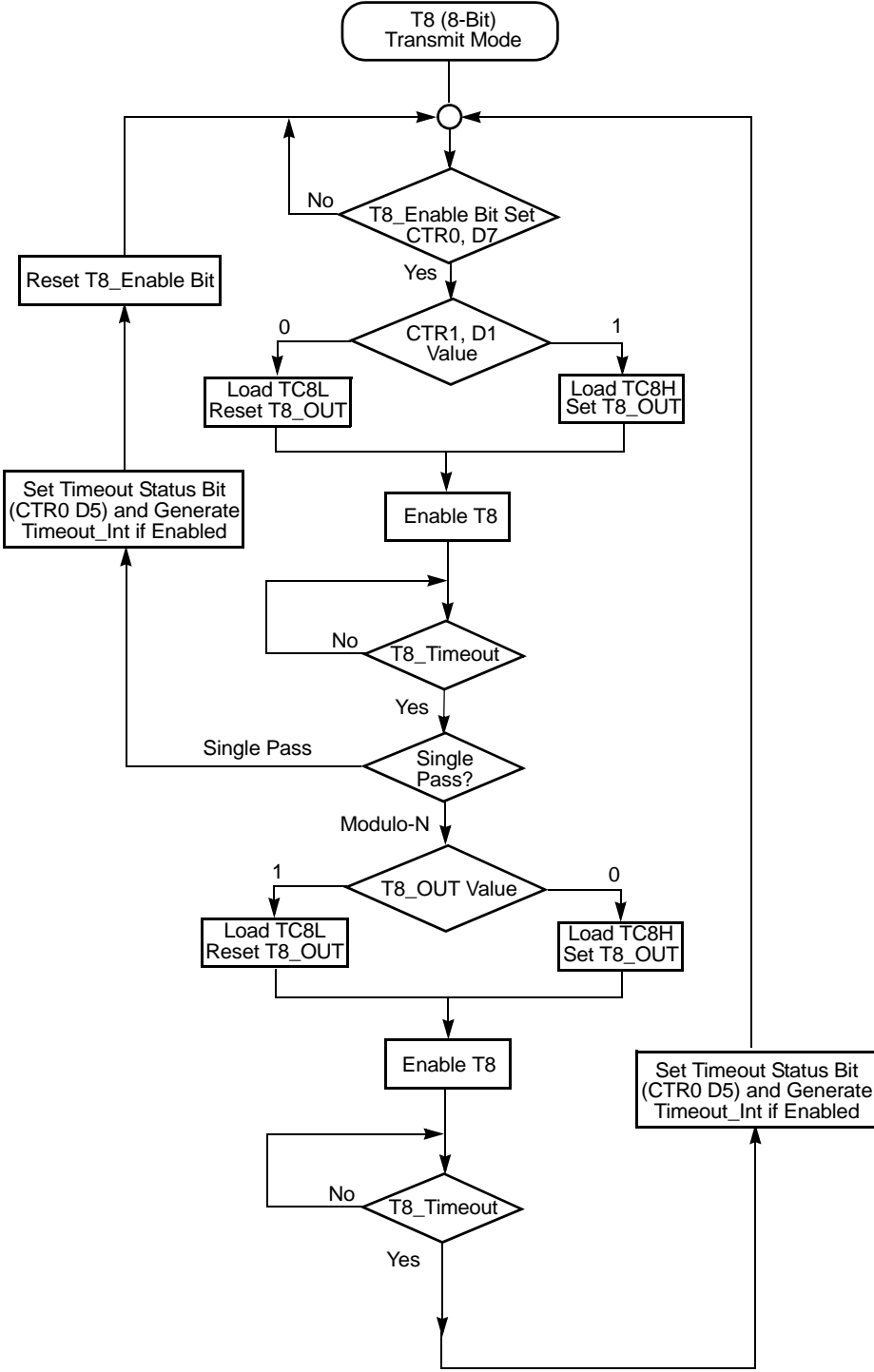


Figure 19. Transmit Mode Flowchart

When T8 is enabled, the output T8\_OUT switches to the initial value (CTR1, D1). If the initial value (CTR1, D1) is 0, TC8L is loaded; otherwise, TC8H is loaded into the counter. In SINGLE-PASS Mode (CTR0, D6), T8 counts down to 0 and stops, T8\_OUT toggles, the timeout status bit (CTR0, D5) is set, and a timeout interrupt can be generated if it is enabled (CTR0, D1). In Modulo-N Mode, upon reaching terminal count, T8\_OUT is toggled, but no interrupt is generated. From that point, T8 loads a new count (if the T8\_OUT level now is 0), TC8L is loaded; if it is 1, TC8H is loaded. T8 counts down to 0, toggles T8\_OUT, and sets the timeout status bit (CTR0, D5), thereby generating an interrupt if enabled (CTR0, D1). One cycle is thus completed. T8 then loads from TC8H or TC8L according to the T8\_OUT level and repeats the cycle. See Figure 20.

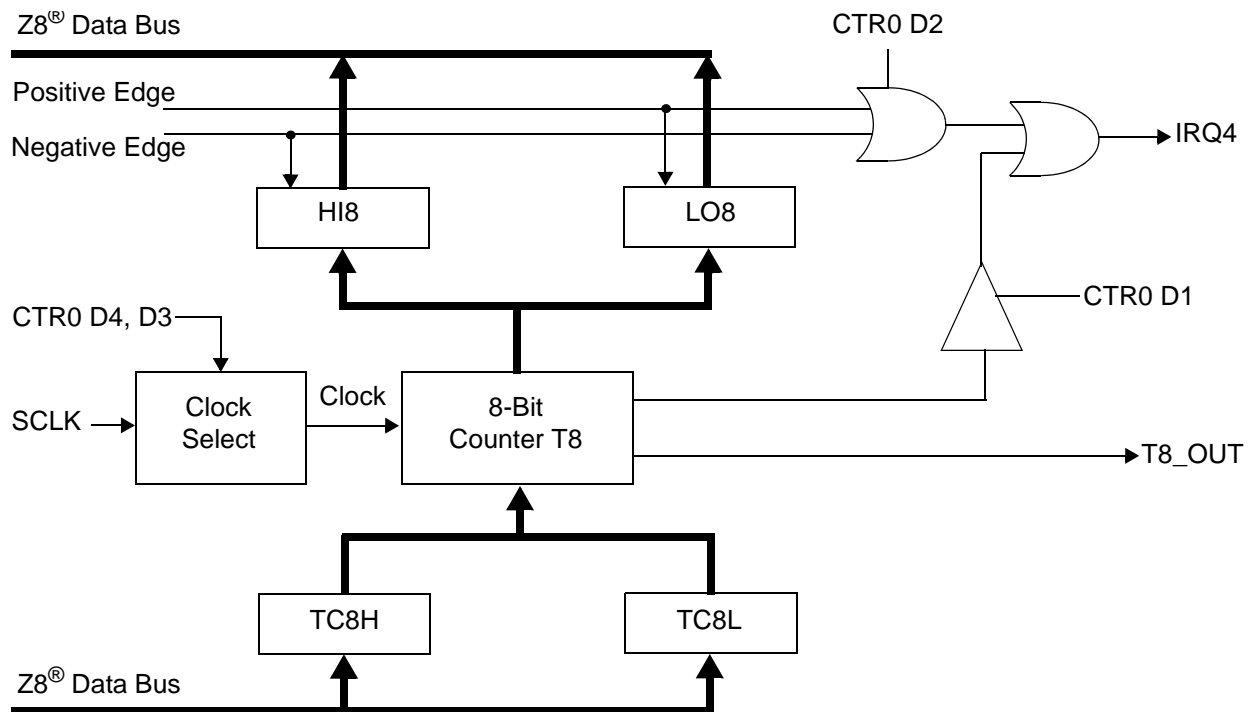


Figure 20. 8-Bit Counter/Timer Circuits

You can modify the values in TC8H or TC8L at any time. The new values take effect when they are loaded.



**Caution:** To ensure known operation do not write these registers at the time the values are to be loaded into the counter/timer. An initial count of 1 is not allowed (a non-function occurs). An initial count of 0 causes TC8 to count from 0 to FFH to FEH.

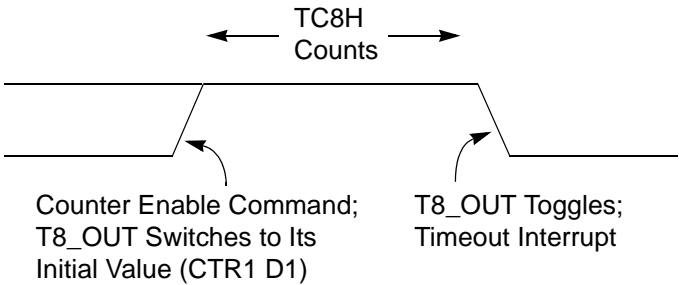
► **Note:** The letter *h* denotes hexadecimal values.

Transition from 0 to FF<sub>h</sub> is not a timeout condition.

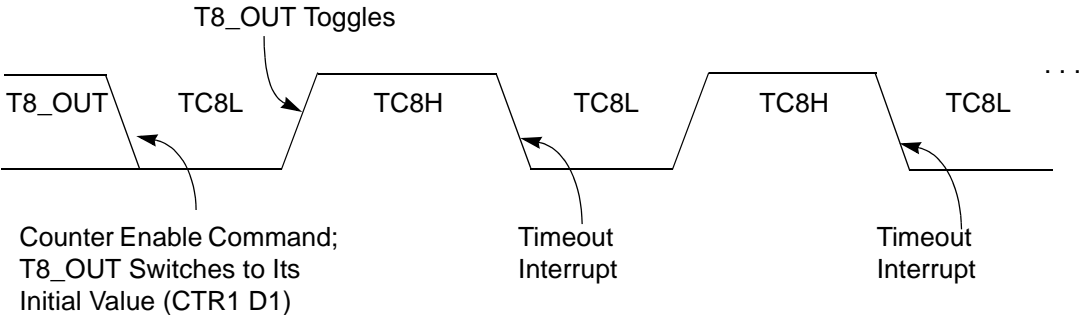


**Caution:** Using the same instructions for stopping the counter/timers and setting the status bits is not recommended.

Two successive commands are necessary. First, the counter/timers must be stopped. Second, the status bits must be reset. These commands are required because it takes one counter/timer clock interval for the initiated event to actually occur. See Figure 21 and Figure 22.



**Figure 21. T8\_OUT in Single-Pass Mode**



**Figure 22. T8\_OUT in Modulo-N Mode**

**T8 Demodulation Mode**

The user must program TC8L and TC8H to FF<sub>h</sub>. After T8 is enabled, when the first edge (rising, falling, or both depending on CTR1, D5; D4) is detected, it starts to count down. When a subsequent edge (rising, falling, or both depending on CTR1, D5; D4) is detected during counting, the current value of T8 is complemented and put into one of the capture registers. If it is a positive edge, data is put

into LO8; if it is a negative edge, data is put into HI8. From that point, one of the edge detect status bits (CTR1, D1; D0) is set, and an interrupt can be generated if enabled (CTR0, D2). Meanwhile, T8 is loaded with FFh and starts counting again. If T8 reaches 0, the timeout status bit (CTR0, D5) is set, and an interrupt can be generated if enabled (CTR0, D1). T8 then continues counting from FFh (see Figure 23 and Figure 24).

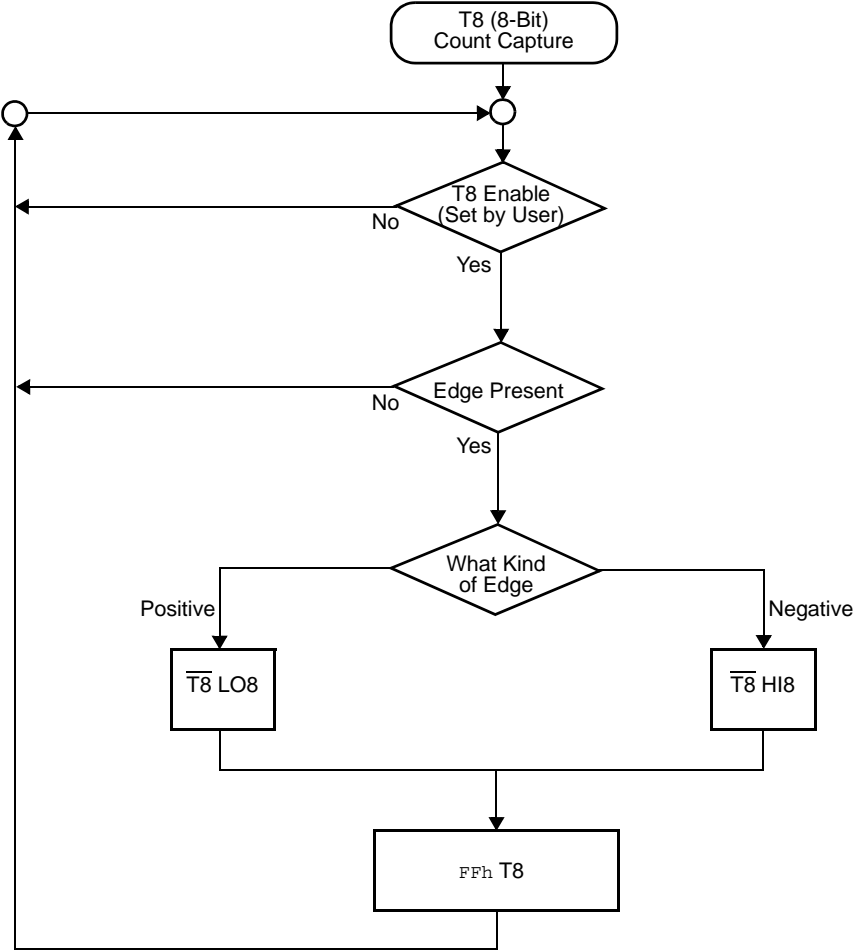


Figure 23. Demodulation Mode Count Capture Flowchart

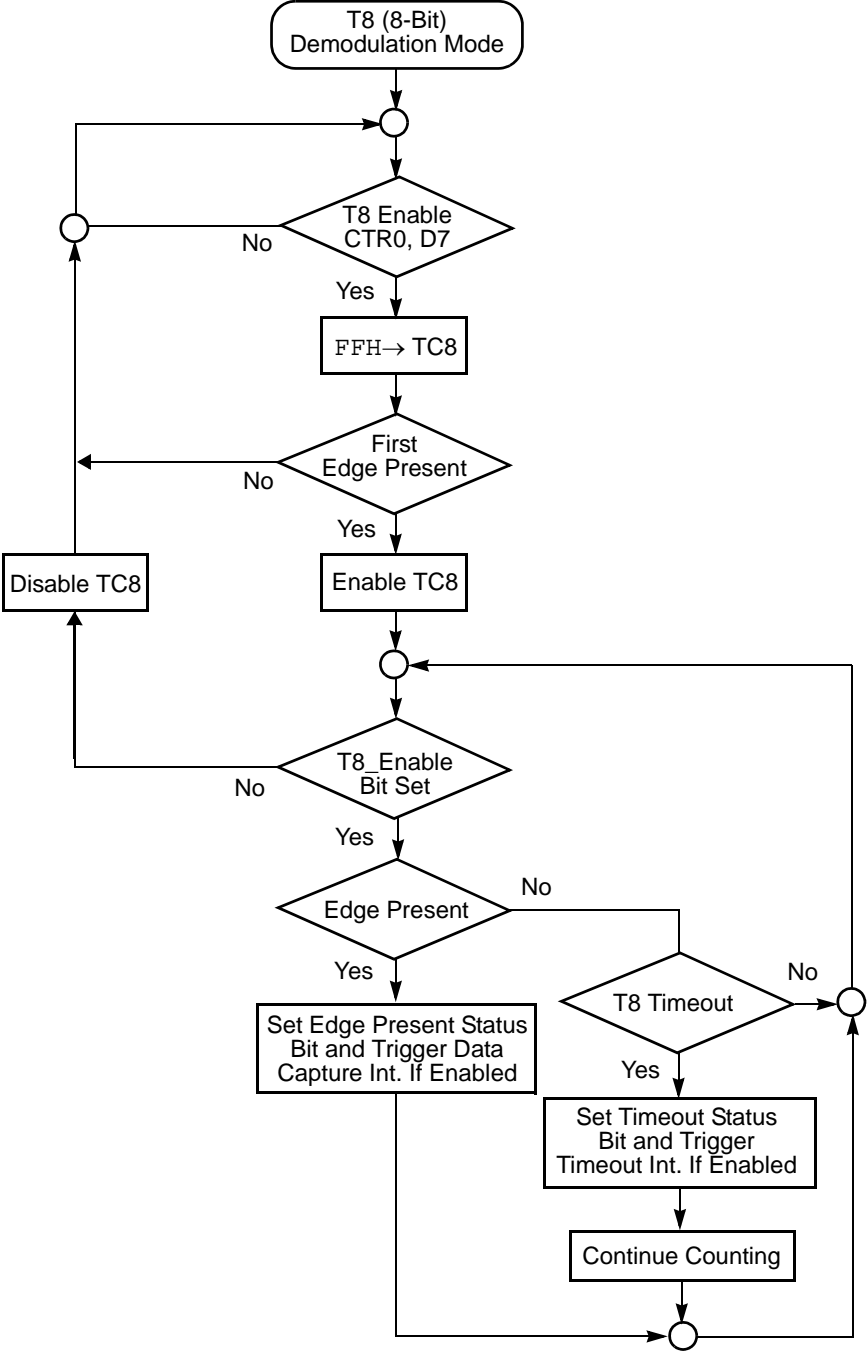


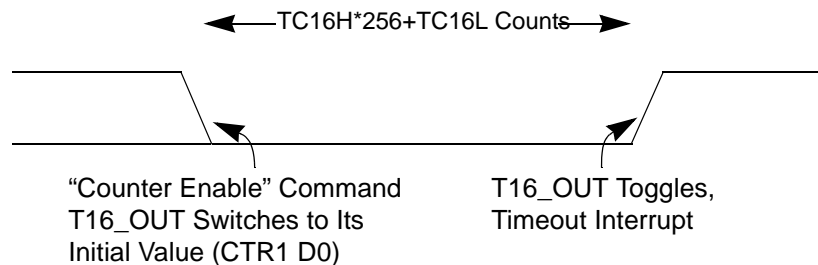
Figure 24. Demodulation Mode Flowchart



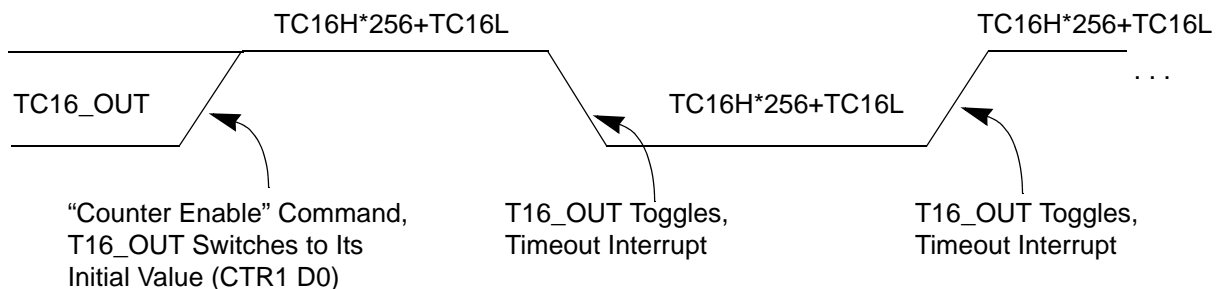


**Caution:**

Do not load these registers at the time the values are to be loaded into the counter/timer to ensure known operation. An initial count of 1 is not allowed. An initial count of 0 causes T16 to count from 0 to FFFFH to FFFE<sub>H</sub>. Transition from 0 to FFFF<sub>H</sub> is not a timeout condition.



**Figure 26. T16\_OUT in Single-Pass Mode**



**Figure 27. T16\_OUT in Modulo-N Mode**

**T16 DEMODULATION Mode**

The user must program TC16L and TC16H to FF<sub>H</sub>. After T16 is enabled, and the first edge (rising, falling, or both depending on CTR1 D5; D4) is detected, T16 captures HI16 and LO16, reloads, and begins counting.

**If D6 of CTR2 Is 0**

When a subsequent edge (rising, falling, or both depending on CTR1, D5; D4) is detected during counting, the current count in T16 is complemented and put into HI16 and LO16. When data is captured, one of the edge detect status bits (CTR1, D1; D0) is set, and an interrupt is generated if enabled (CTR2, D2). T16 is loaded with FFFF<sub>H</sub> and starts again.

This T16 mode is generally used to measure space time, the length of time between bursts of carrier signal (marks).

### If D6 of CTR2 Is 1

T16 ignores the subsequent edges in the input signal and continues counting down. A timeout of T8 causes T16 to capture its current value and generate an interrupt if enabled (CTR2, D2). In this case, T16 does not reload and continues counting. If the D6 bit of CTR2 is toggled (by writing a 0 then a 1 to it), T16 captures and reloads on the next edge (rising, falling, or both depending on CTR1, D5; D4), continuing to ignore subsequent edges.

This T16 mode generally measures mark time, the length of an active carrier signal burst.

If T16 reaches 0, T16 continues counting from `FFFFh`. Meanwhile, a status bit (CTR2 D5) is set, and an interrupt timeout can be generated if enabled (CTR2 D1).

### Ping-Pong Mode

This operation mode is only valid in TRANSMIT Mode. T8 and T16 must be programmed in Single-Pass mode (CTR0, D6; CTR2, D6), and Ping-Pong mode must be programmed in CTR1, D3; D2. The user can begin the operation by enabling either T8 or T16 (CTR0, D7 or CTR2, D7). For example, if T8 is enabled, T8\_OUT is set to this initial value (CTR1, D1). According to T8\_OUT's level, TC8H or TC8L is loaded into T8. After the terminal count is reached, T8 is disabled, and T16 is enabled. T16\_OUT then switches to its initial value (CTR1, D0), data from TC16H and TC16L is loaded, and T16 starts to count. After T16 reaches the terminal count, it stops, T8 is enabled again, repeating the entire cycle. Interrupts can be allowed when T8 or T16 reaches terminal control (CTR0, D1; CTR2, D1). To stop the ping-pong operation, write 00 to bits D3 and D2 of CTR1. See Figure 28.

- **Note:** Enabling ping-pong operation while the counter/timers are running might cause intermittent counter/timer function. Disable the counter/timers and reset the status flags before instituting this operation.



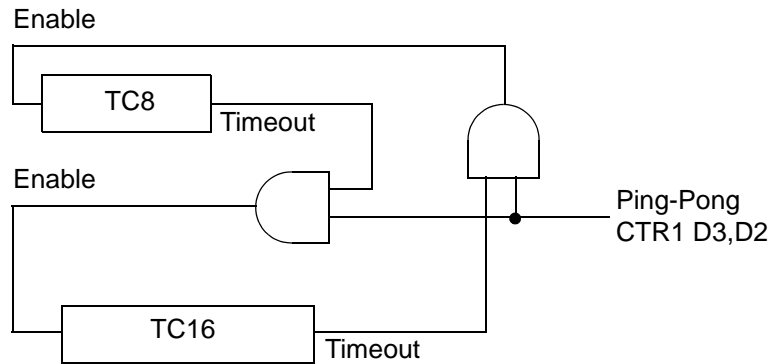


Figure 28. Ping-Pong Mode Diagram

### Initiating PING-PONG Mode

First, make sure both counter/timers are not running. Set T8 into Single-Pass mode (CTR0, D6), set T16 into SINGLE-PASS mode (CTR2, D6), and set the Ping-Pong mode (CTR1, D2; D3). These instructions can be in random order. Finally, start PING-PONG mode by enabling either T8 (CTR0, D7) or T16 (CTR2, D7). See Figure 29.

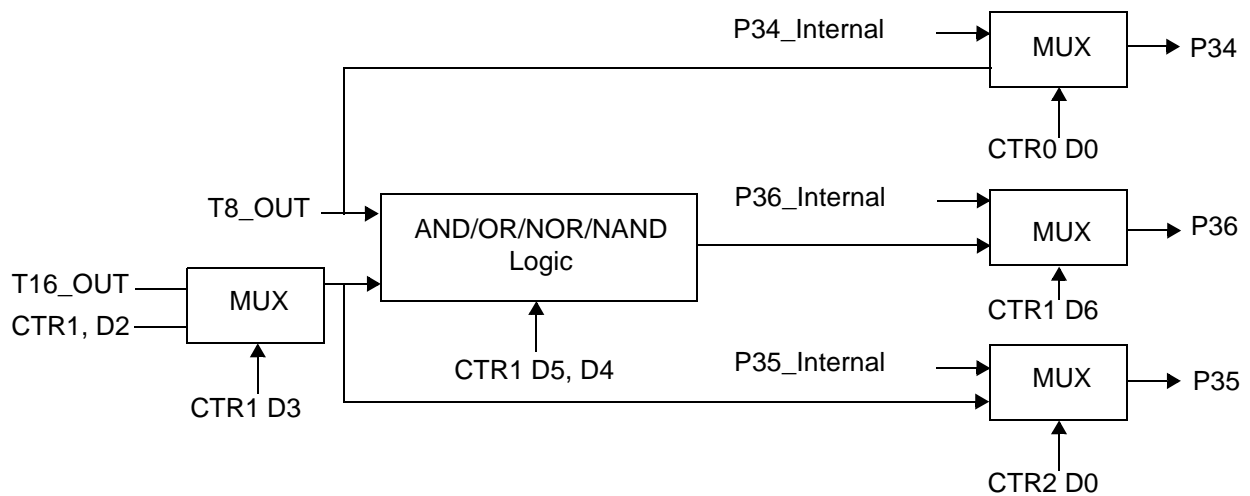


Figure 29. Output Circuit

The initial value of T8 or T16 must not be 1. Stopping the timer and restarting the timer reloads the initial value to avoid an unknown previous value.



### During PING-PONG Mode

The enable bits of T8 and T16 (CTR0, D7; CTR2, D7) are set and cleared alternately by hardware. The timeout bits (CTR0, D5; CTR2, D5) are set every time the counter/timers reach the terminal count.

### Interrupts

The ZGP323H features six different interrupts (Table 19). The interrupts are maskable and prioritized (Figure 30). The six sources are divided as follows: three sources are claimed by Port 3 lines P33–P31, two by the counter/timers (Table 19) and one for low voltage detection. The Interrupt Mask Register (globally or individually) enables or disables the six interrupt requests.

The source for IRQ is determined by bit 1 of the Port 3 mode register (P3M). When in digital mode, Pin P33 is the source. When in analog mode the output of the Stop mode recovery source logic is used as the source for the interrupt. See Figure 35, Stop Mode Recovery Source, on page 59.

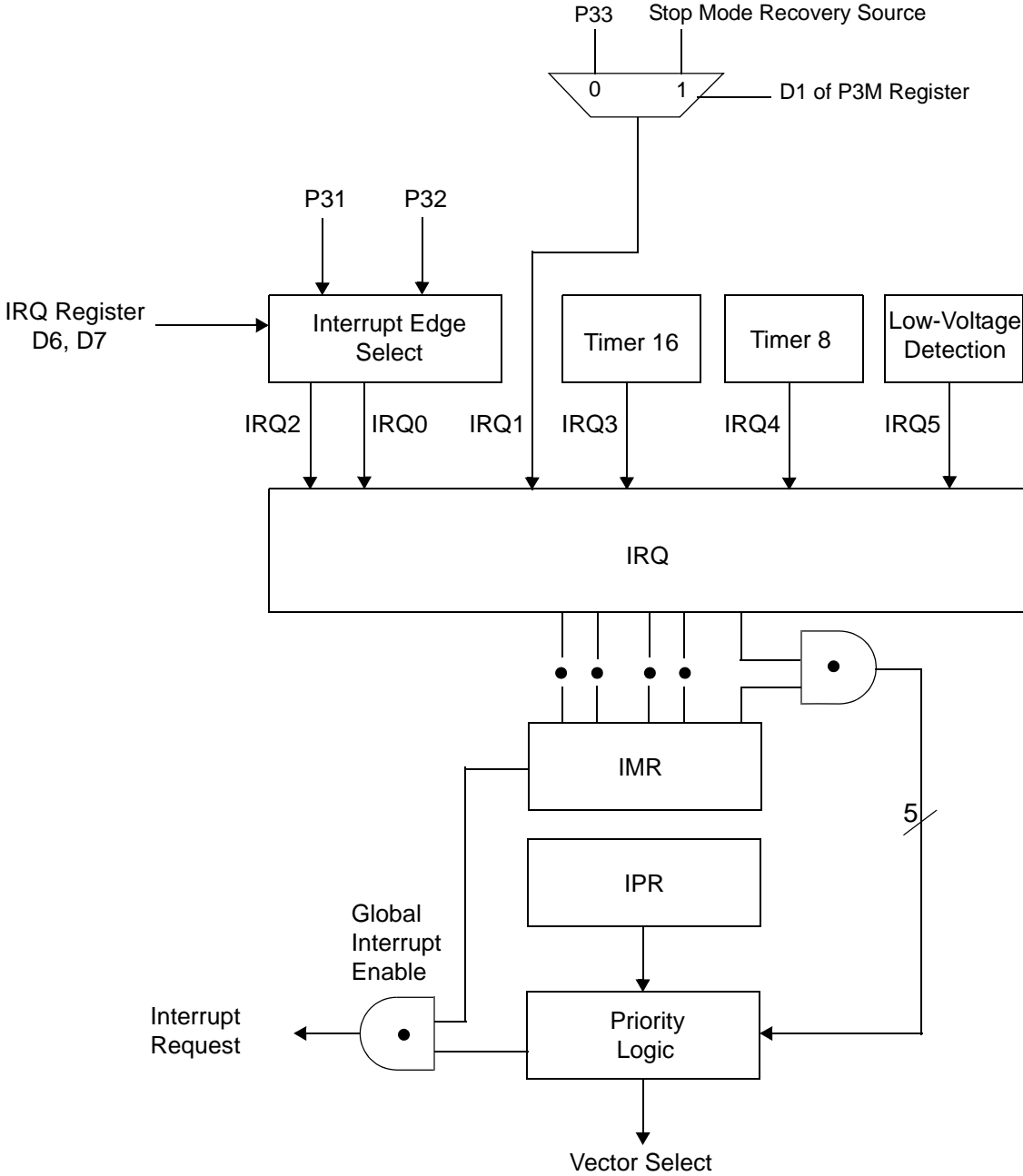


Figure 30. Interrupt Block Diagram



**Table 19. Interrupt Types, Sources, and Vectors**

Name	Source	Vector Location	Comments
IRQ0	P32	0,1	External (P32), Rising, Falling Edge Triggered
IRQ1	P33	2,3	External (P33), Falling Edge Triggered
IRQ2	P31, T <sub>IN</sub>	4,5	External (P31), Rising, Falling Edge Triggered
IRQ3	T16	6,7	Internal
IRQ4	T8	8,9	Internal
IRQ5	LVD	10,11	Internal

When more than one interrupt is pending, priorities are resolved by a programmable priority encoder controlled by the Interrupt Priority Register. An interrupt machine cycle activates when an interrupt request is granted. As a result, all subsequent interrupts are disabled, and the Program Counter and Status Flags are saved. The cycle then branches to the program memory vector location reserved for that interrupt. All ZGP323H interrupts are vectored through locations in the program memory. This memory location and the next byte contain the 16-bit address of the interrupt service routine for that particular interrupt request. To accommodate polled interrupt systems, interrupt inputs are masked, and the Interrupt Request register is polled to determine which of the interrupt requests require service.

An interrupt resulting from AN1 is mapped into IRQ2, and an interrupt from AN2 is mapped into IRQ0. Interrupts IRQ2 and IRQ0 can be rising, falling, or both edge triggered. These interrupts are programmable by the user. The software can poll to identify the state of the pin.

Programming bits for the Interrupt Edge Select are located in the IRQ Register (R250), bits D7 and D6. The configuration is indicated in Table 20.

**Table 20. IRQ Register**

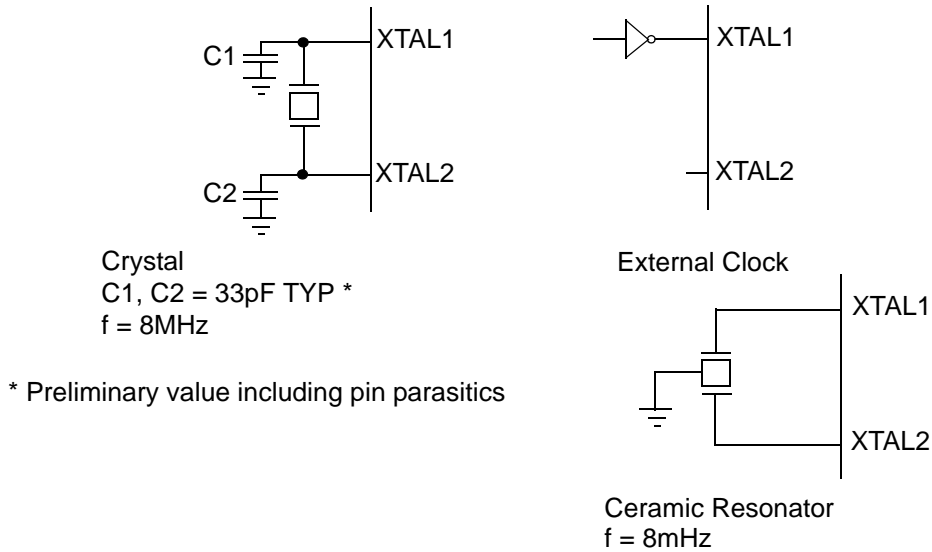
IRQ		Interrupt Edge	
D7	D6	IRQ2 (P31)	IRQ0 (P32)
0	0	F	F
0	1	F	R
1	0	R	F
1	1	R/F	R/F

**Note:** F = Falling Edge; R = Rising Edge

### Clock

The device's on-chip oscillator has a high-gain, parallel-resonant amplifier, for connection to a crystal or ceramic resonator, or any suitable external clock source (XTAL1 = Input, XTAL2 = Output). The crystal must be AT cut, 1 MHz to 8 MHz maximum, with a series resistance (RS) less than or equal to 100  $\Omega$ . The on-chip oscillator can be driven with a suitable external clock source.

The crystal must be connected across XTAL1 and XTAL2 using the recommended capacitors (capacitance greater than or equal to 22 pF) from each pin to ground.



**Figure 31. Oscillator Configuration**



### Power-On Reset

A timer circuit clocked by a dedicated on-board RC-oscillator is used for the Power-On Reset (POR) timer function. The POR time allows  $V_{DD}$  and the oscillator circuit to stabilize before instruction execution begins.

The POR timer circuit is a one-shot timer triggered by one of three conditions:

- Power Fail to Power OK status, including Waking up from  $V_{BO}$  Standby
- Stop-Mode Recovery (if D5 of SMR = 1)
- WDT Timeout

The POR timer is 2.5 ms minimum. Bit 5 of the Stop-Mode Register determines whether the POR timer is bypassed after Stop-Mode Recovery (typical for external clock).

### HALT Mode

This instruction turns off the internal CPU clock, but not the XTAL oscillation. The counter/timers and external interrupts IRQ0, IRQ1, IRQ2, IRQ3, IRQ4, and IRQ5 remain active. The devices are recovered by interrupts, either externally or internally generated. An interrupt request must be executed (enabled) to exit HALT Mode. After the interrupt service routine, the program continues from the instruction after HALT Mode.

### STOP Mode

This instruction turns off the internal clock and external crystal oscillation, reducing the standby current to 10  $\mu$ A or less. STOP Mode is terminated only by a reset, such as WDT timeout, POR, SMR or external reset. This condition causes the processor to restart the application program at address 000CH. To enter STOP (or HALT) mode, first flush the instruction pipeline to avoid suspending execution in mid-instruction. Execute a NOP (Opcode = FFH) immediately before the appropriate sleep instruction, as follows:

```

FF          NOP          ; clear the pipeline
6F          Stop        ; enter Stop Mode
    
```

or

```

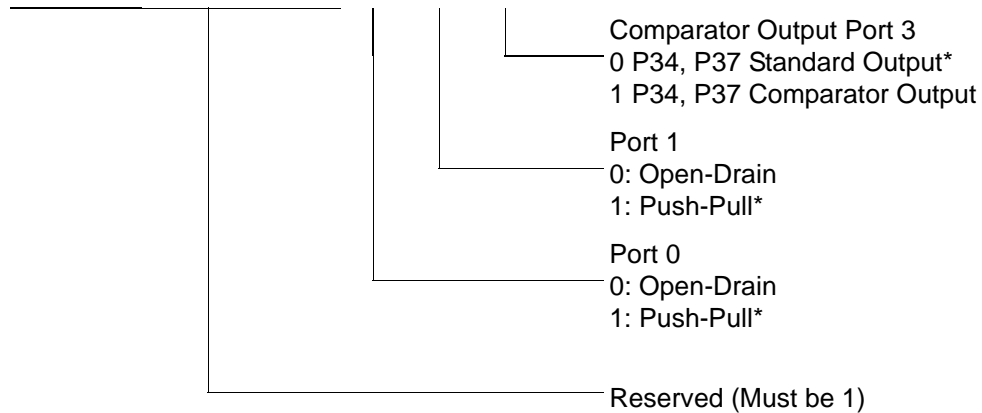
FF          NOP          ; clear the pipeline
7F          HALT        ; enter HALT Mode
    
```

### Port Configuration Register

The Port Configuration (PCON) register (Figure 32) configures the comparator output on Port 3. It is located in the expanded register 2 at Bank F, location 00.

PCON(FH)00H

D7	D6	D5	D4	D3	D2	D1	D0
----	----	----	----	----	----	----	----



\* Default setting after reset

**Figure 32. Port Configuration Register (PCON) (Write Only)**

#### Comparator Output Port 3 (D0)

Bit 0 controls the comparator used in Port 3. A 1 in this location brings the comparator outputs to P34 and P37, and a 0 releases the Port to its standard I/O configuration.

#### Port 1 Output Mode (D1)

Bit 1 controls the output mode of port 1. A 1 in this location sets the output to push-pull, and a 0 sets the output to open-drain.



### Port 0 Output Mode (D2)

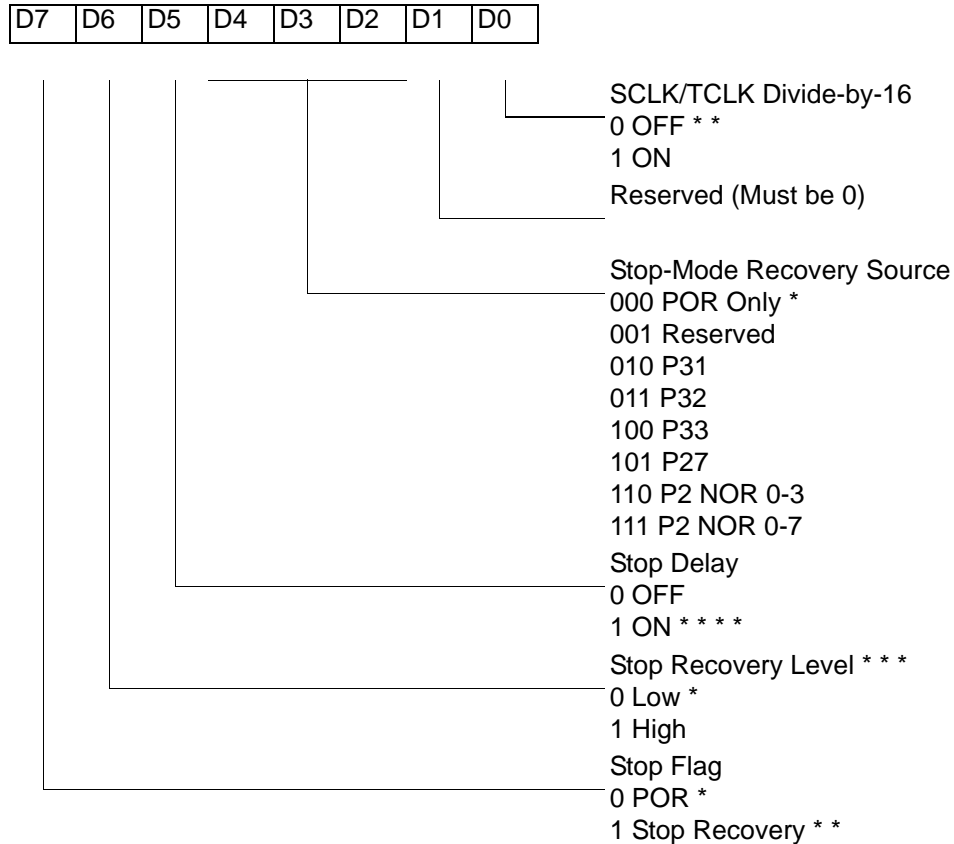
Bit 2 controls the output mode of port 0. A 1 in this location sets the output to push-pull, and a 0 sets the output to open-drain.

### Stop-Mode Recovery Register (SMR)

This register selects the clock divide value and determines the mode of Stop Mode Recovery (Figure 33). All bits are write only except bit 7, which is read only. Bit 7 is a flag bit that is hardware set on the condition of Stop recovery and reset by a power-on cycle. Bit 6 controls whether a low level or a high level at the XOR-gate input (Figure 35 on page 59) is required from the recovery source. Bit 5 controls the reset delay after recovery. Bits D2, D3, and D4 of the SMR register specify the source of the Stop Mode Recovery signal. Bit D0 determines if SCLK/TCLK are divided by 16 or not. The SMR is located in Bank F of the Expanded Register Group at address 0BH.



SMR(0F)0BH



- \* Default after Power On Reset or Watch-Dog Reset
- \*\* Default setting after Reset and Stop Mode Recovery
- \*\*\* At the XOR gate input
- \*\*\*\* Default setting after reset. Must be 1 if using a crystal or resonator clock source.

**Figure 33. STOP Mode Recovery Register**

**SCLK/TCLK Divide-by-16 Select (D0)**

D0 of the SMR controls a divide-by-16 prescaler of SCLK/TCLK (Figure 34). This control selectively reduces device power consumption during normal processor execution (SCLK control) and/or Halt Mode (where TCLK sources interrupt logic). After Stop Mode Recovery, this bit is set to a 0.

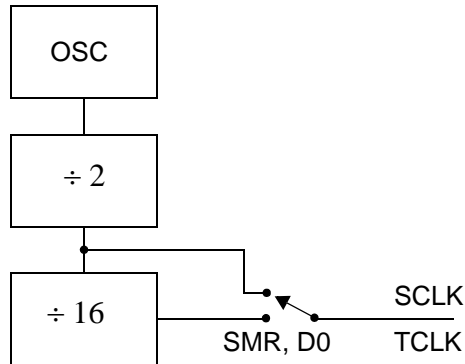


Figure 34. SCLK Circuit

### Stop-Mode Recovery Source (D2, D3, and D4)

These three bits of the SMR specify the wake-up source of the Stop recovery (Figure 35 and Table 22).

### Stop-Mode Recovery Register 2—SMR2(F)0DH

Table 21 lists and briefly describes the fields for this register.

Table 21. SMR2(F)0DH:Stop Mode Recovery Register 2\*

Field	Bit Position	Value	Description
Reserved	7-----	0	Reserved (Must be 0)
Recovery Level	-6-----	W 0 <sup>†</sup>	Low
		1	High
Reserved	--5-----	0	Reserved (Must be 0)
Source	---432--	W 000 <sup>†</sup>	A. POR Only
		001	B. NAND of P23–P20
		010	C. NAND of P27–P20
		011	D. NOR of P33–P31
		100	E. NAND of P33–P31
		101	F. NOR of P33–P31, P00, P07
		110	G. NAND of P33–P31, P00, P07
		111	H. NAND of P33–P31, P22–P20
Reserved	-----10	00	Reserved (Must be 0)

**Notes:**

\* Port pins configured as outputs are ignored as a SMR recovery source.

<sup>†</sup> Indicates the value upon Power-On Reset

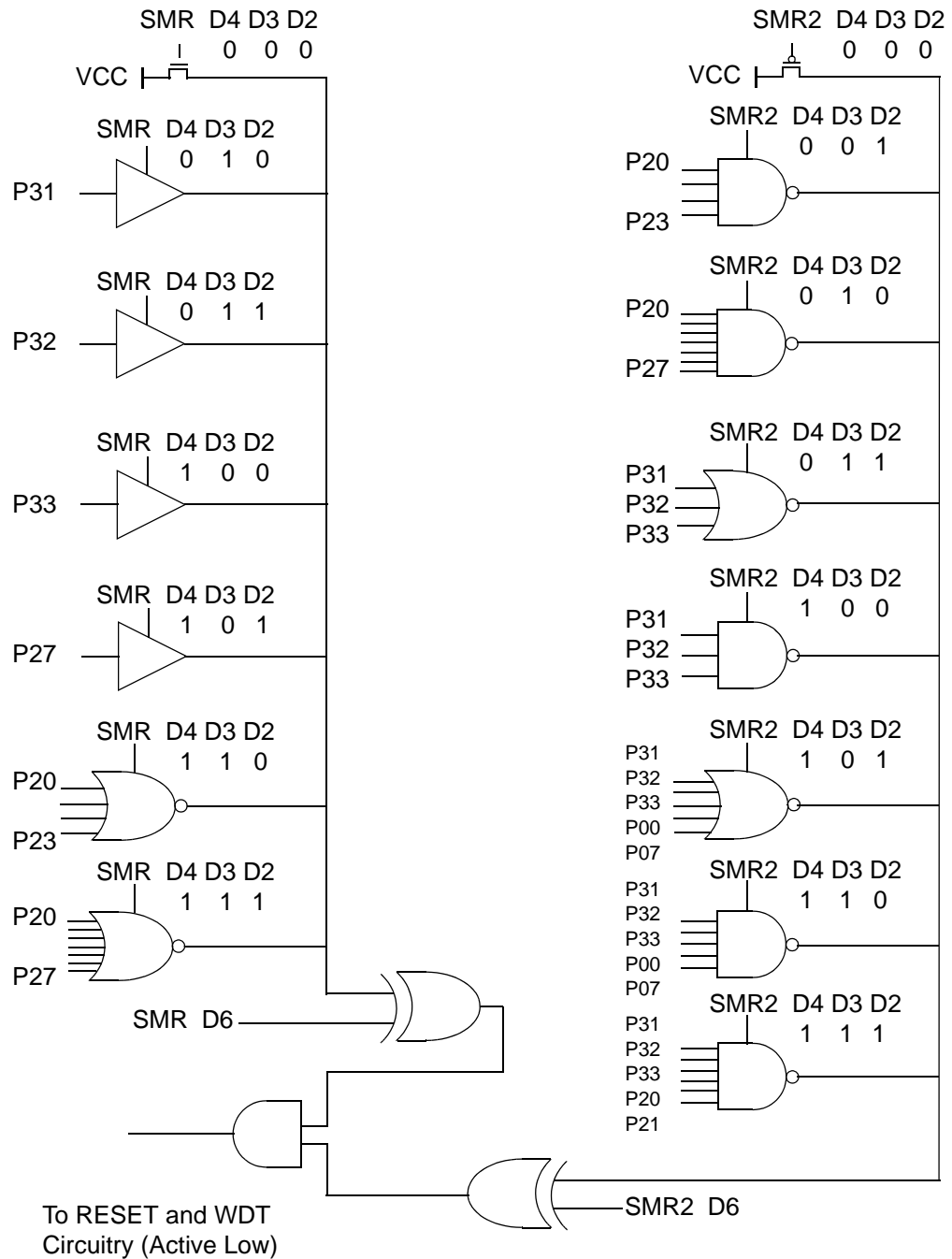


Figure 35. Stop Mode Recovery Source

**Table 22. Stop Mode Recovery Source**

SMR:432			Operation
D4	D3	D2	Description of Action
0	0	0	POR and/or external reset recovery
0	0	1	Reserved
0	1	0	P31 transition
0	1	1	P32 transition
1	0	0	P33 transition
1	0	1	P27 transition
1	1	0	Logical NOR of P20 through P23
1	1	1	Logical NOR of P20 through P27

- **Note:** Any Port 2 bit defined as an output drives the corresponding input to the default state. This condition allows the remaining inputs to control the AND/OR function. Refer to SMR2 register on page 61 for other recover sources.

#### Stop Mode Recovery Delay Select (D5)

This bit, if Low, disables the  $T_{POR}$  delay after Stop Mode Recovery. The default configuration of this bit is 1. If the “fast” wake up is selected, the Stop Mode Recovery source must be kept active for at least 5  $T_{pC}$ .

- **Note:** This bit must be set to 1 if using a crystal or resonator clock source. The  $T_{POR}$  delay allows the clock source to stabilize before executing instructions.

#### Stop Mode Recovery Edge Select (D6)

A 1 in this bit position indicates that a High level on any one of the recovery sources wakes the device from Stop Mode. A 0 indicates Low level recovery. The default is 0 on POR.

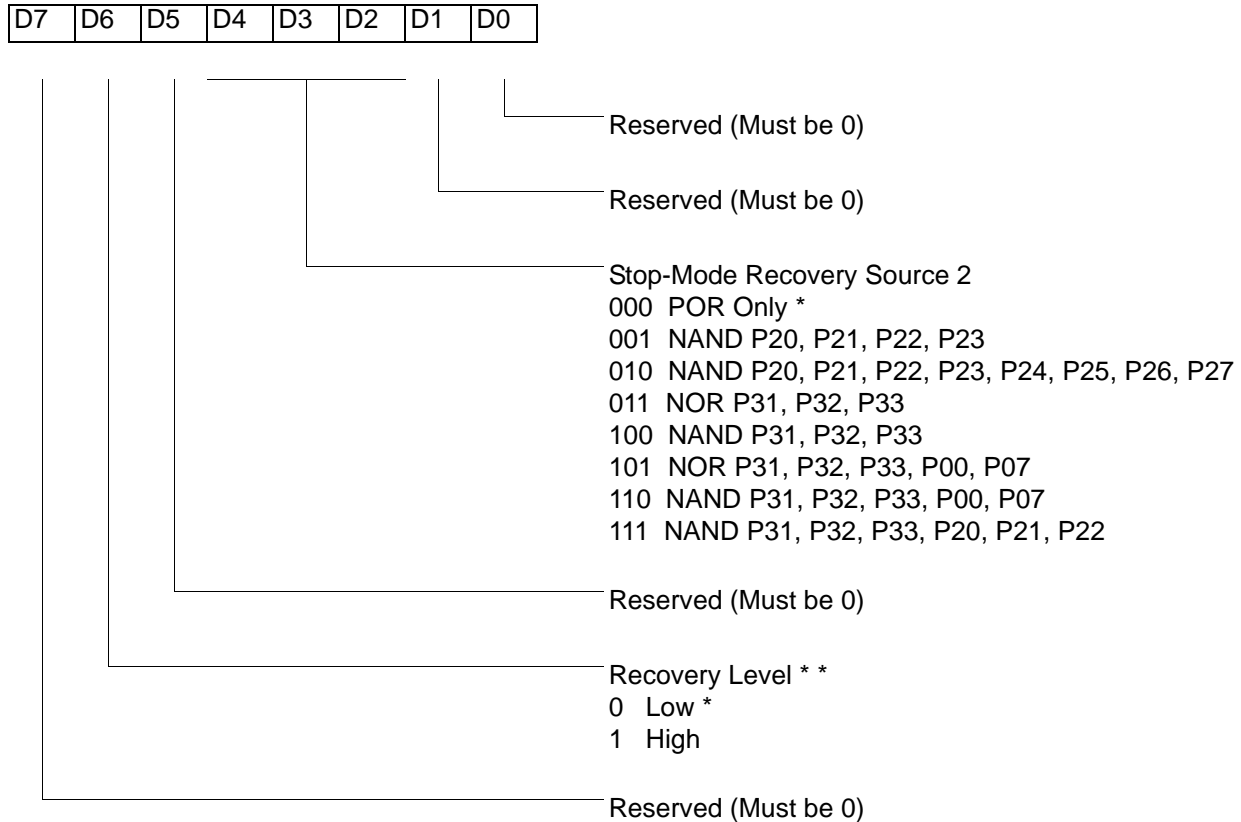
#### Cold or Warm Start (D7)

This bit is read only. It is set to 1 when the device is recovered from Stop Mode. The bit is set to 0 when the device reset is other than Stop Mode Recovery (SMR).

### Stop Mode Recovery Register 2 (SMR2)

This register determines the mode of Stop Mode Recovery for SMR2 (Figure 36).

SMR2(0F)DH



Note: If used in conjunction with SMR, either of the two specified events causes a Stop-Mode Recovery.

\* Default setting after reset

\*\* At the XOR gate input

**Figure 36. Stop Mode Recovery Register 2 ((0F)DH:D2–D4, D6 Write Only)**

If SMR2 is used in conjunction with SMR, either of the specified events causes a Stop Mode Recovery.

► **Note:** Port pins configured as outputs are ignored as an SMR or SMR2 recovery source. For example, if the NAND or P23–P20 is selected as the recovery source and P20 is configured as an output, the remaining SMR pins (P23–P21) form the NAND equation.

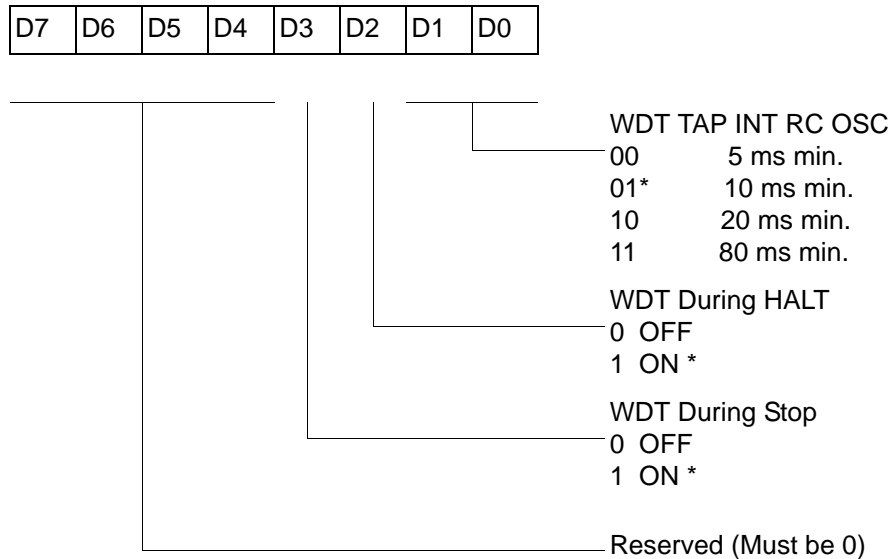


**Watch-Dog Timer Mode Register (WDTMR)**

The Watch-Dog Timer (WDT) is a retriggerable one-shot timer that resets the Z8<sup>®</sup> CPU if it reaches its terminal count. The WDT must initially be enabled by executing the WDT instruction. On subsequent executions of the WDT instruction, the WDT is refreshed. The WDT circuit is driven by an on-board RC-oscillator. The WDT instruction affects the Zero (Z), Sign (S), and Overflow (V) flags.

The POR clock source the internal RC-oscillator. Bits 0 and 1 of the WDT register control a tap circuit that determines the minimum timeout period. Bit 2 determines whether the WDT is active during HALT, and Bit 3 determines WDT activity during Stop. Bits 4 through 7 are reserved (Figure 37). This register is accessible only during the first 60 processor cycles (120 XTAL clocks) from the execution of the first instruction after Power-On-Reset, Watch-Dog Reset, or a Stop-Mode Recovery (Figure 36). After this point, the register cannot be modified by any means (intentional or otherwise). The WDTMR cannot be read. The register is located in Bank F of the Expanded Register Group at address location 0Fh. It is organized as shown in Figure 37.

WDTMR(0F)0Fh



\* Default setting after reset

**Figure 37. Watch-Dog Timer Mode Register (Write Only)**

**WDT Time Select (D0, D1)**

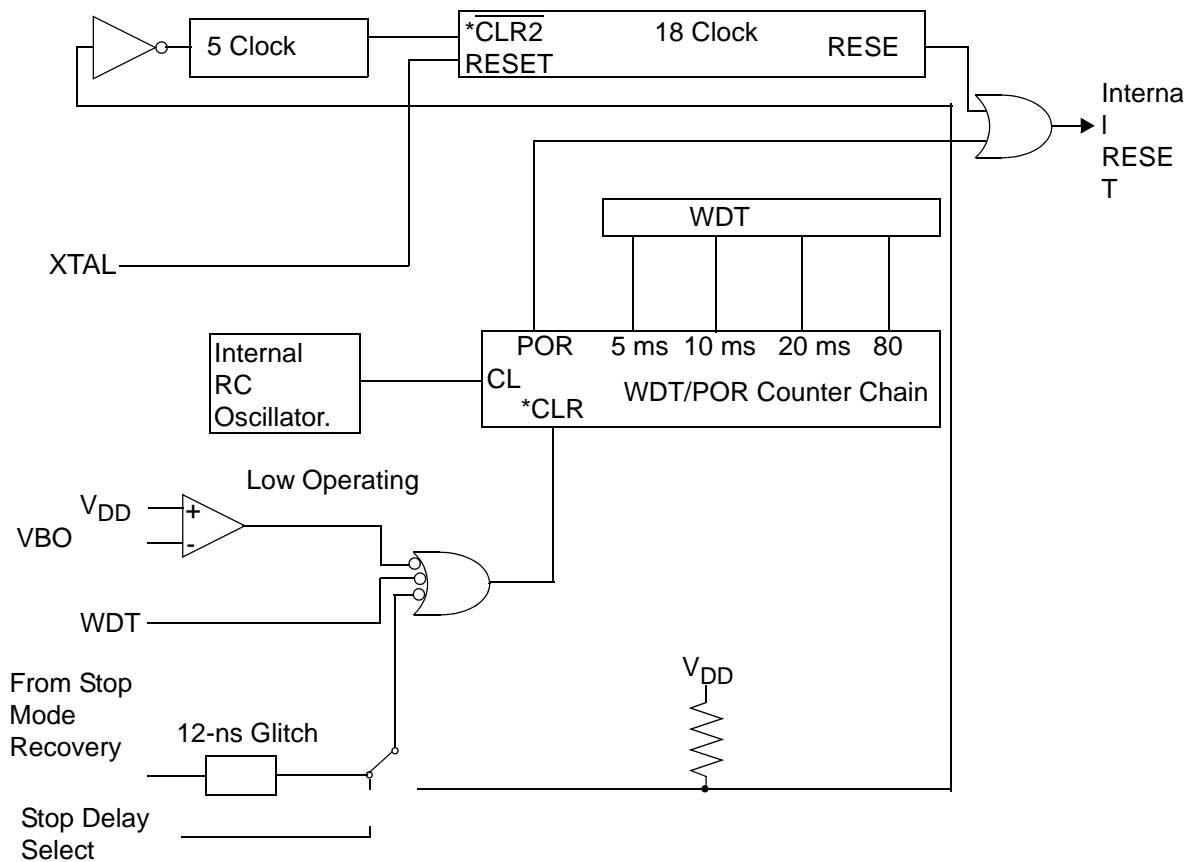
This bit selects the WDT time period. It is configured as indicated in Table 23.

**Table 23. Watch-Dog Timer Time Select**

D1	D0	Timeout of Internal RC-Oscillator
0	0	5ms min.
0	1	10ms min.
1	0	20ms min.
1	1	80ms min.

**WDTMR During Halt (D2)**

This bit determines whether or not the WDT is active during HALT Mode. A 1 indicates active during HALT. The default is 1. See Figure 38.



\* CLR1 and  $\overline{\text{CLR2}}$  enable the WDT/POR and 18 Clock Reset timers respectively upon a Low-to-

**Figure 38. Resets and WDT**



### WDTMR During STOP (D3)

This bit determines whether or not the WDT is active during STOP Mode. Because the XTAL clock is stopped during STOP Mode, the on-board RC has to be selected as the clock source to the WDT/POR counter. A 1 indicates active during Stop. The default is 1.

### EPROM Selectable Options

There are seven EPROM Selectable Options to choose from based on ROM code requirements. These options are listed in Table 24.

**Table 24. EPROM Selectable Options**

Port 00–03 Pull-Ups	On/Off
Port 04–07 Pull-Ups	On/Off
Port 10–13 Pull-Ups	On/Off
Port 14–17 Pull-Ups	On/Off
Port 20–27 Pull-Ups	On/Off
EPROM Protection	On/Off
Watch-Dog Timer at Power-On Reset	On/Off

### Voltage Brown-Out/Standby

An on-chip Voltage Comparator checks that the  $V_{DD}$  is at the required level for correct operation of the device. Reset is globally driven when  $V_{DD}$  falls below  $V_{BO}$ . A small drop in  $V_{DD}$  causes the XTAL1 and XTAL2 circuitry to stop the crystal or resonator clock. If the  $V_{DD}$  is allowed to stay above  $V_{RAM}$ , the RAM content is preserved. When the power level is returned to above  $V_{BO}$ , the device performs a POR and functions normally.



### Low-Voltage Detection Register—LVD(D)0Ch

- **Note:** Voltage detection does not work at Stop mode. It must be disabled during Stop mode in order to reduce current.

Field	Bit Position			Description
LVD	76543---			Reserved No Effect
	----2--	R	1 0*	HVD flag set HVD flag reset
	-----1-	R	1 0*	LVD flag set LVD flag reset
	-----0	R/W	1 0*	Enable VD Disable VD

\*Default after POR

- **Note:** Do not modify register P01M while checking a low-voltage condition. Switching noise of both ports 0 and 1 together might trigger the LVD flag.

### Voltage Detection and Flags

The Voltage Detection register (LVD, register 0CH at the expanded register bank 0Dh) offers an option of monitoring the  $V_{CC}$  voltage. The Voltage Detection is enabled when bit 0 of LVD register is set. Once Voltage Detection is enabled, the  $V_{CC}$  level is monitored in real time. The flags in the LVD register valid 20 $\mu$ S after Voltage Detection is enabled. The HVD flag (bit 2 of the LVD register) is set only if  $V_{CC}$  is higher than  $V_{HVD}$ . The LVD flag (bit 1 of the LVD register) is set only if  $V_{CC}$  is lower than the  $V_{LVD}$ . When Voltage Detection is enabled, the LVD flag also triggers IRQ5. The IRQ bit 5 latches the low voltage condition until it is cleared by instructions or reset. The IRQ5 interrupt is served if it is enabled in the IMR register. Otherwise, bit 5 of IRQ register is latched as a flag only.

- **Notes:** If it is necessary to receive an LVD interrupt upon power-up at an operating voltage lower than the low battery detect threshold, enable interrupts using the Enable Interrupt instruction (EI) prior to enabling the voltage detection.

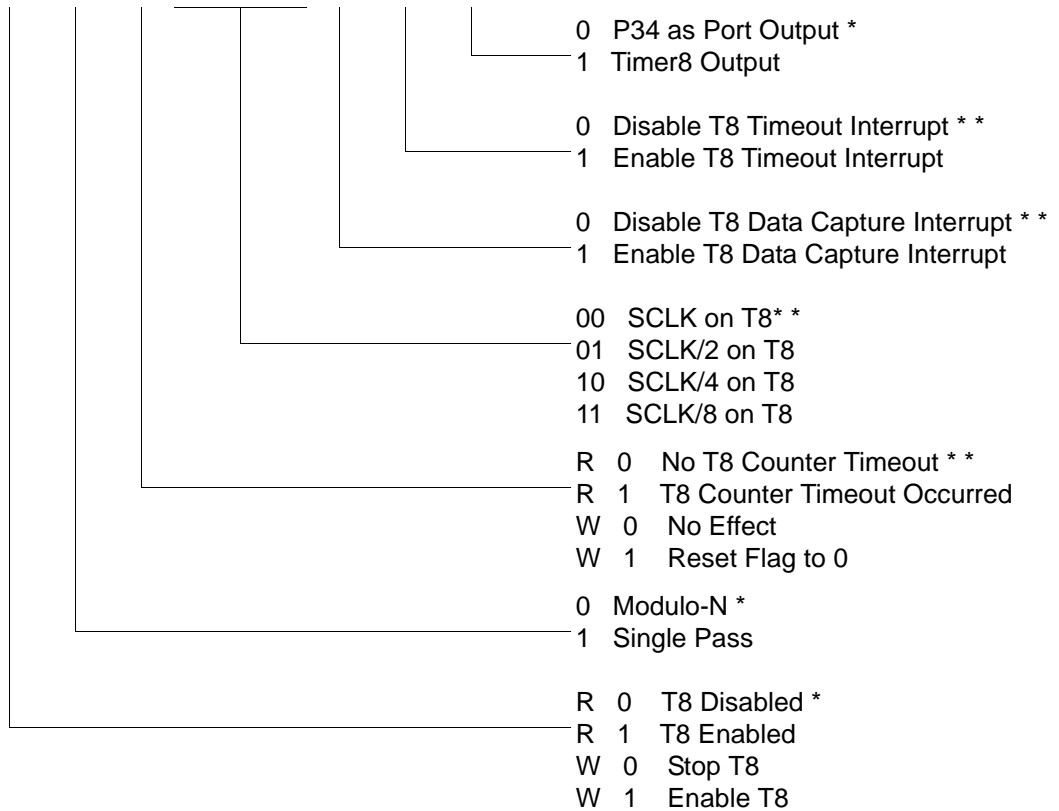


## Expanded Register File Control Registers (0D)

The expanded register file control registers (0D) are depicted in Figure 39 through Figure 43.

CTR0(0D)00H

D7	D6	D5	D4	D3	D2	D1	D0
----	----	----	----	----	----	----	----



\* Default setting after reset.

\*\* Default setting after Reset.. Not reset with a Stop-Mode recovery.

Figure 39. TC8 Control Register ((0D)00H: Read/Write Except Where Noted)



CTR1(0D)01H

D7	D6	D5	D4	D3	D2	D1	D0
----	----	----	----	----	----	----	----

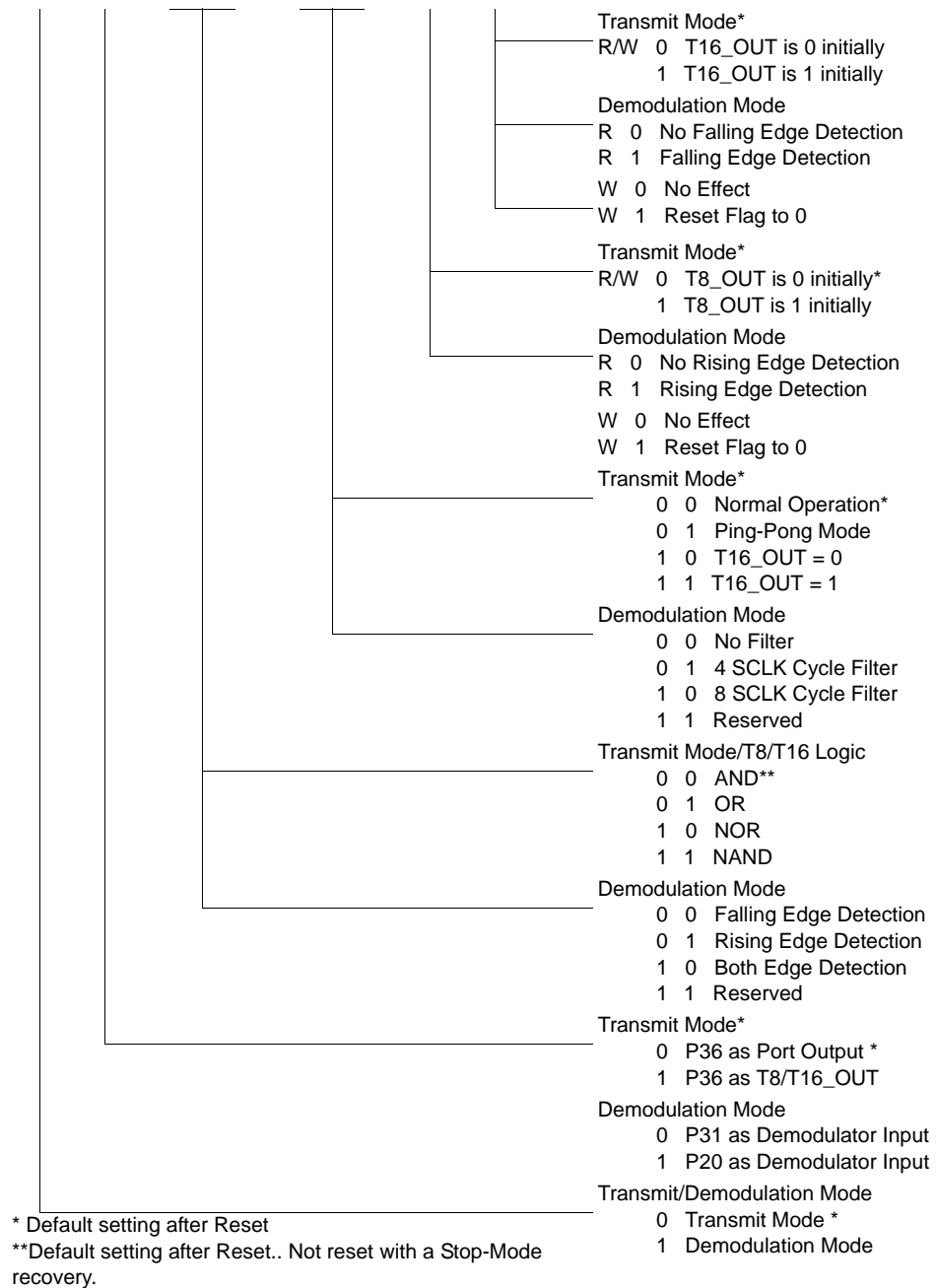


Figure 40. T8 and T16 Common Control Functions ((0D)01H: Read/Write)



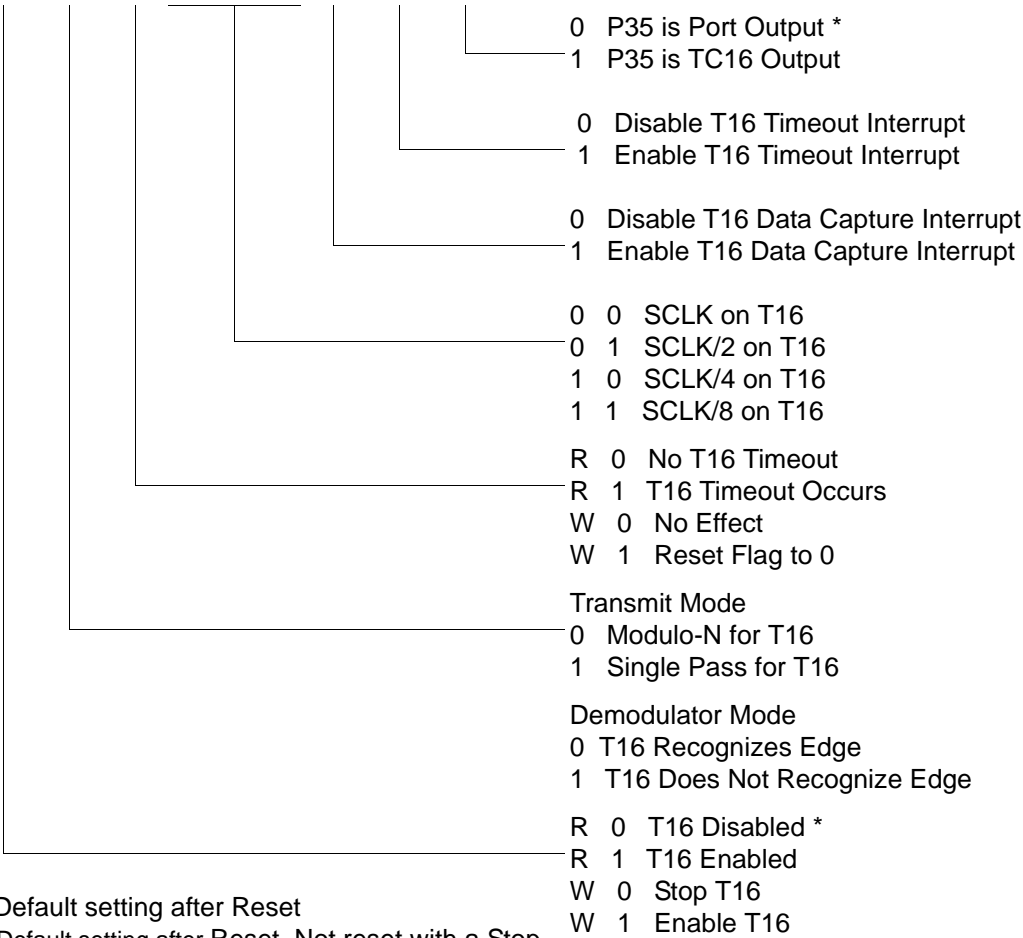
- ▶ **Notes:** Take care in differentiating the Transmit Mode from Demodulation Mode. Depending on which of these two modes is operating, the CTR1 bit has different functions.

Changing from one mode to another cannot be performed without disabling the counter/timers.



CTR2(0D)02H

D7	D6	D5	D4	D3	D2	D1	D0
----	----	----	----	----	----	----	----

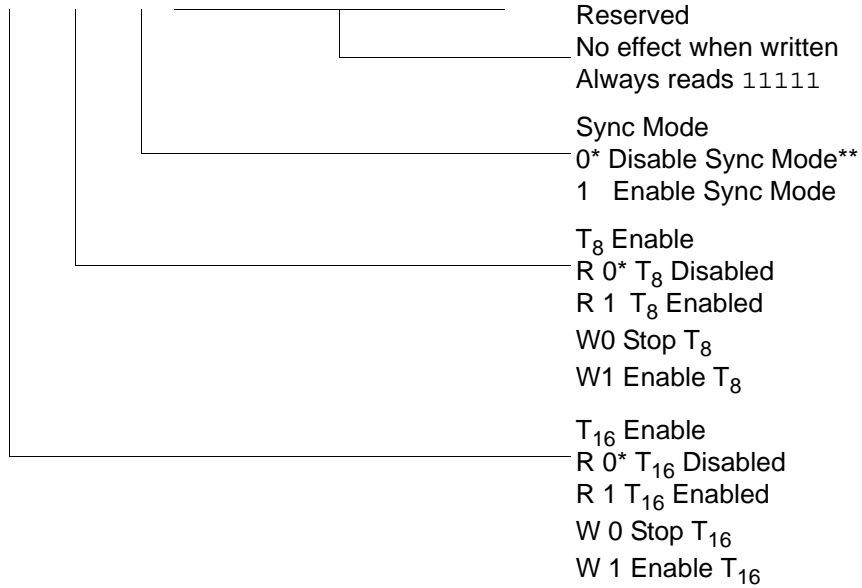


\* Default setting after Reset  
 \*\*Default setting after Reset. Not reset with a Stop-Mode recovery.

Figure 41. T16 Control Register ((0D) 2H: Read/Write Except Where Noted)

CTR3(0D)03H

D7	D6	D5	D4	D3	D2	D1	D0
----	----	----	----	----	----	----	----



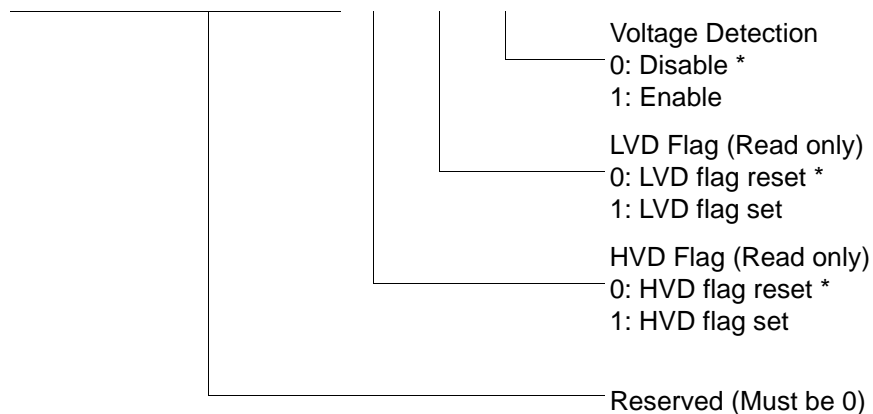
\* Default setting after reset.

\*\* Default setting after reset. Not reset with a Stop Mode recovery.

**Figure 42. T8/T16 Control Register (0D)03H: Read/Write (Except Where Noted)**

LVD(0D)0CH

D7	D6	D5	D4	D3	D2	D1	D0
----	----	----	----	----	----	----	----



\* Default setting after reset.

**Figure 43. Voltage Detection Register**

- **Note:** Do not modify register P01M while checking a low-voltage condition. Switching noise of both ports 0 and 1 together might trigger the LVD flag.

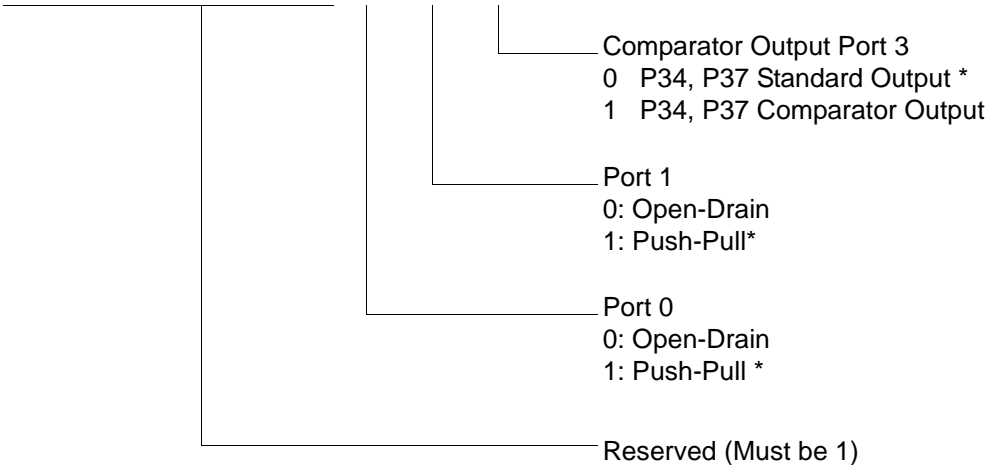
## Expanded Register File Control Registers (0F)

The expanded register file control registers (0F) are depicted in Figures 44 through Figure 57.



PCON(0F)00H

D7	D6	D5	D4	D3	D2	D1	D0
----	----	----	----	----	----	----	----



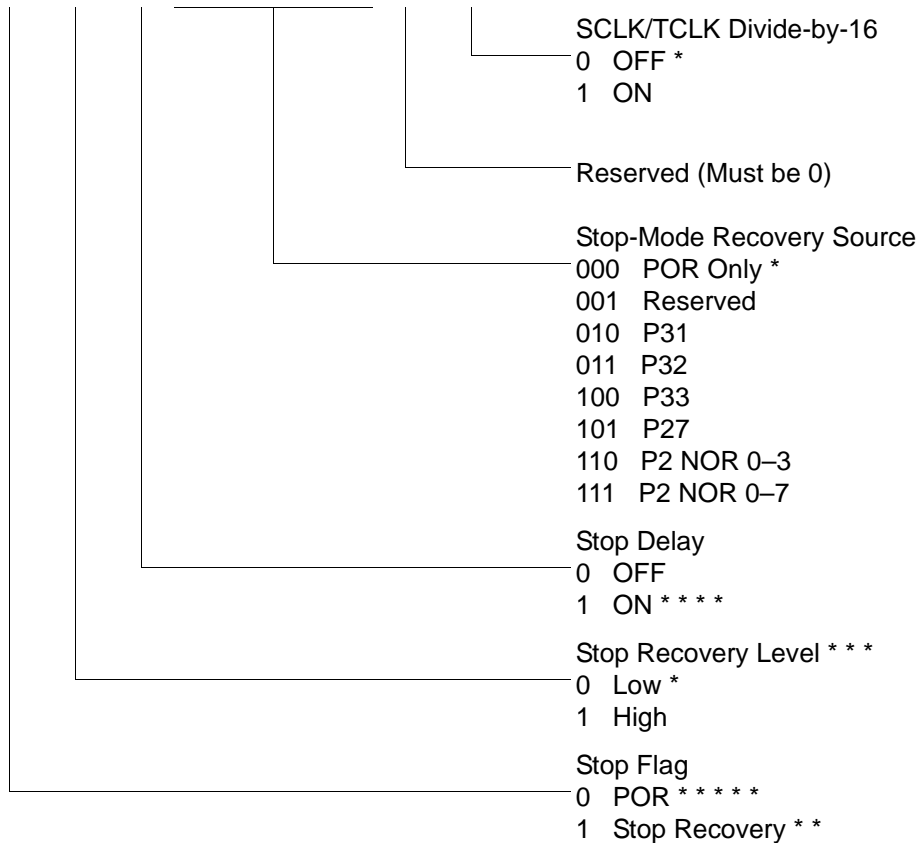
\* Default setting after reset

Figure 44. Port Configuration Register (PCON)(0F)00H: Write Only



SMR(0F)0BH

D7	D6	D5	D4	D3	D2	D1	D0
----	----	----	----	----	----	----	----

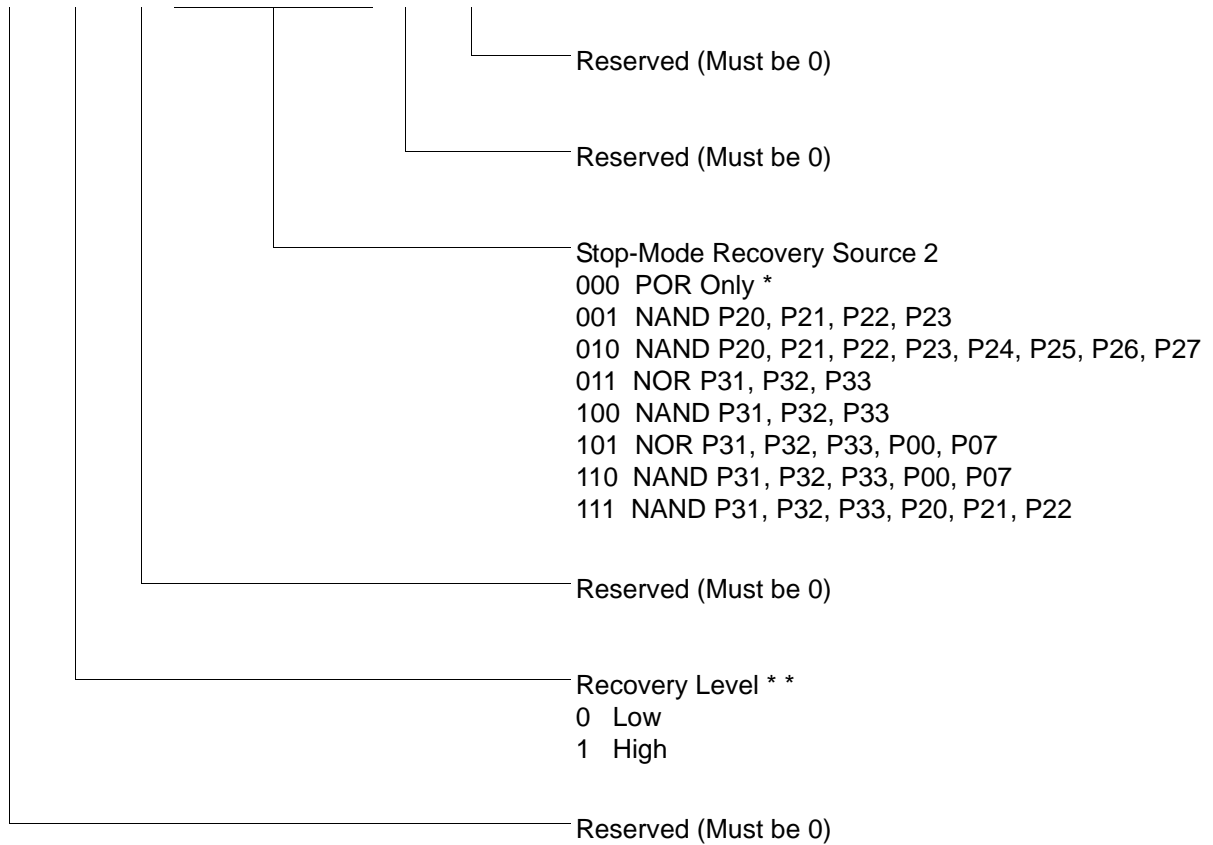


- \* Default setting after reset
- \*\* Set after Stop Mode Recovery
- \*\*\* At the XOR gate input
- \*\*\*\* Default setting after reset. Must be 1 if using a crystal or resonator clock source.
- \*\*\*\*\* Default setting after Power On Reset. Not reset with a Stop Mode recovery.

**Figure 45. Stop Mode Recovery Register ((0F)0BH: D6–D0=Write Only, D7=Read Only)**

SMR2(0F)0DH

D7	D6	D5	D4	D3	D2	D1	D0
----	----	----	----	----	----	----	----



Note: If used in conjunction with SMR, either of the two specified events causes a Stop-Mode Recovery.

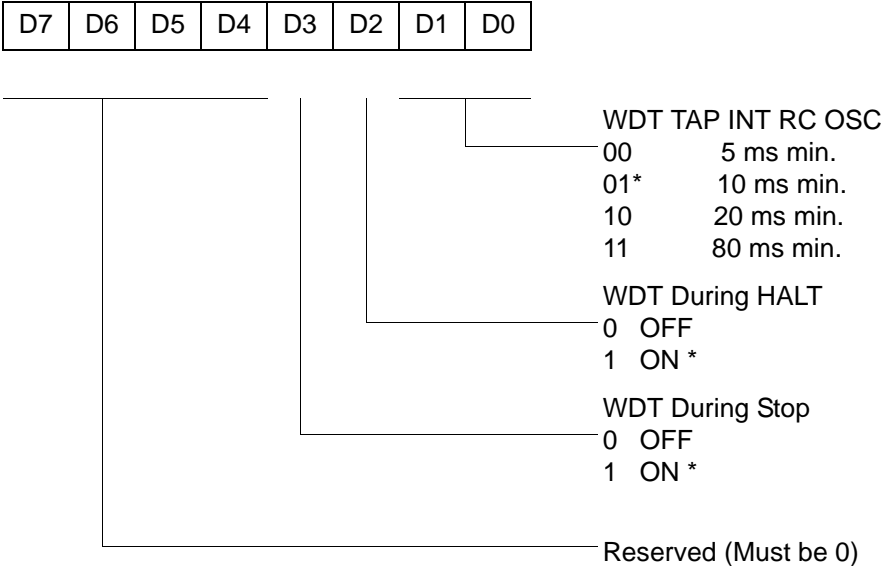
\* Default setting after reset. Not reset with a Stop Mode recovery.

\*\* At the XOR gate input

Figure 46. Stop Mode Recovery Register 2 ((0F)0DH:D2–D4, D6 Write Only)



WDTMR(0F)0FH

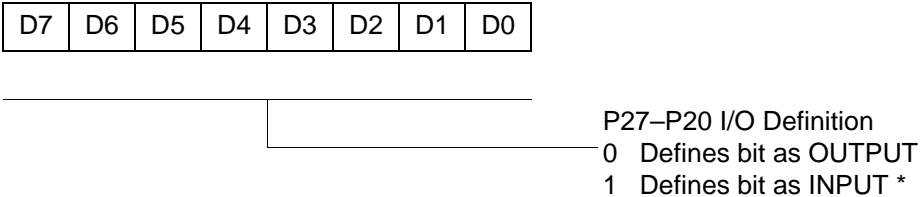


\* Default setting after reset. Not reset with a Stop Mode recovery.

Figure 47. Watch-Dog Timer Register ((0F) 0FH: Write Only)

### Standard Control Registers

R246 P2M(F6H)



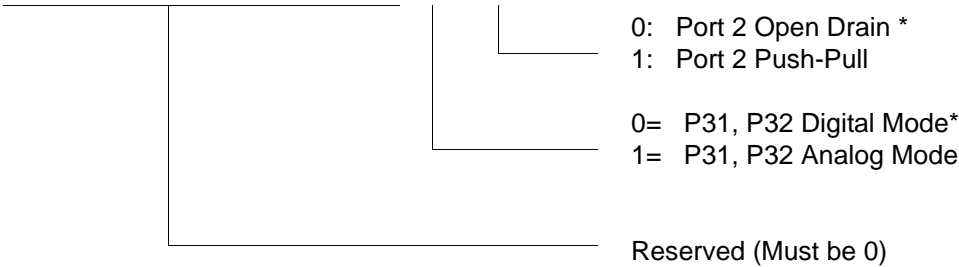
\* Default setting after reset. Not reset with a Stop Mode recovery.

Figure 48. Port 2 Mode Register (F6H: Write Only)



R247 P3M(F7H)

D7	D6	D5	D4	D3	D2	D1	D0
----	----	----	----	----	----	----	----

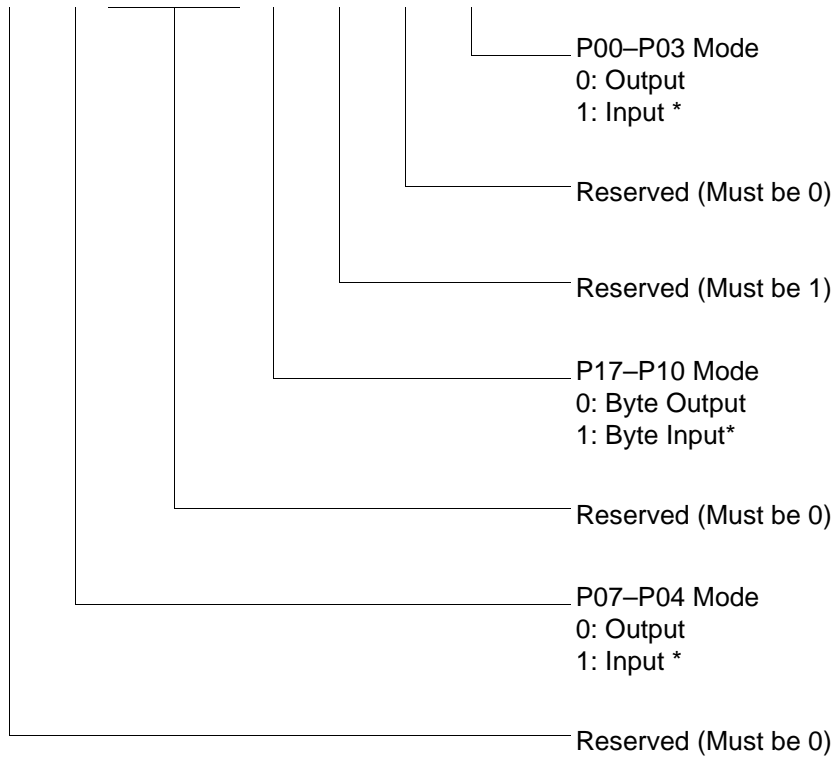


\* Default setting after reset. Not reset with a Stop Mode recovery.

Figure 49. Port 3 Mode Register (F7H: Write Only)

R248 P01M(F8H)

D7	D6	D5	D4	D3	D2	D1	D0
----	----	----	----	----	----	----	----



\* Default setting after reset; only P00, P01 and P07 are available on 20-pin configurations.

**Figure 50. Port 0 and 1 Mode Register (F8H: Write Only)**



R249 IPR(F9H)

D7	D6	D5	D4	D3	D2	D1	D0
----	----	----	----	----	----	----	----

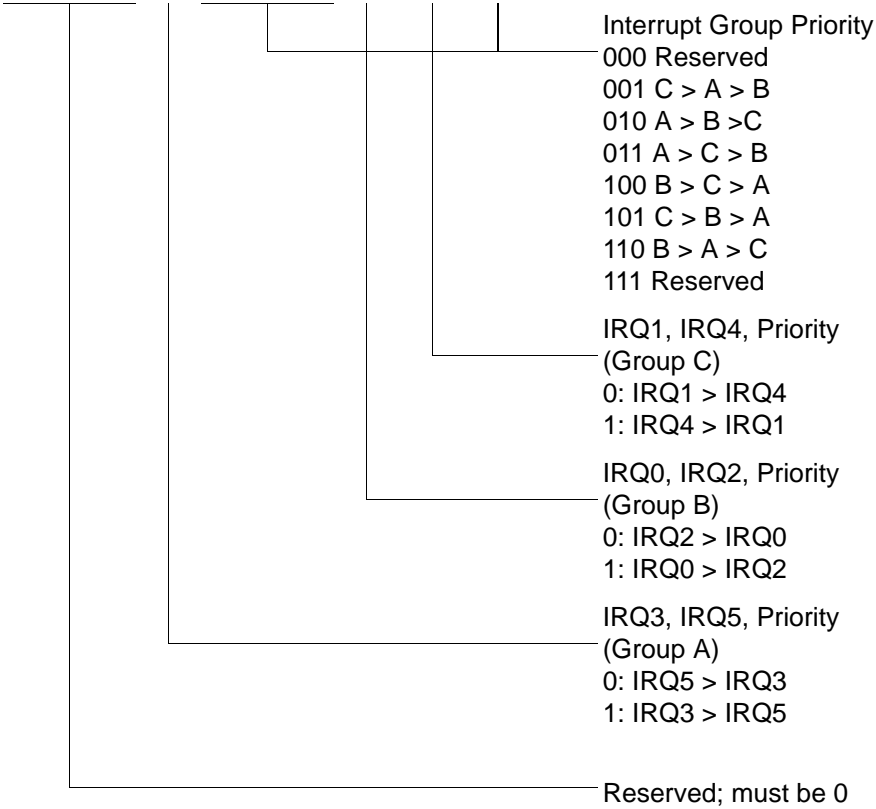


Figure 51. Interrupt Priority Register (F9H: Write Only)



R250 IRQ(FAH)

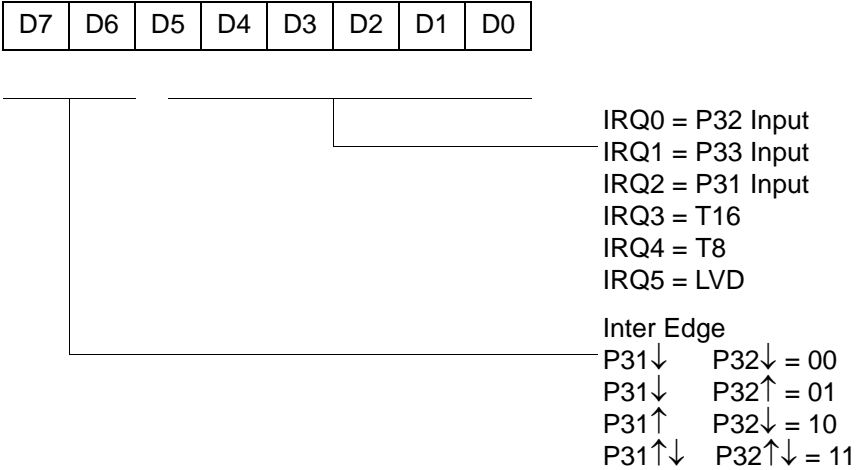


Figure 52. Interrupt Request Register (FAH: Read/Write)

R251 IMR(FBH)



\* Default setting after reset  
 \*\* Only by using EI, DI instruction; DI is required before changing the IMR register

Figure 53. Interrupt Mask Register (FBH: Read/Write)



R252 Flags(FCH)

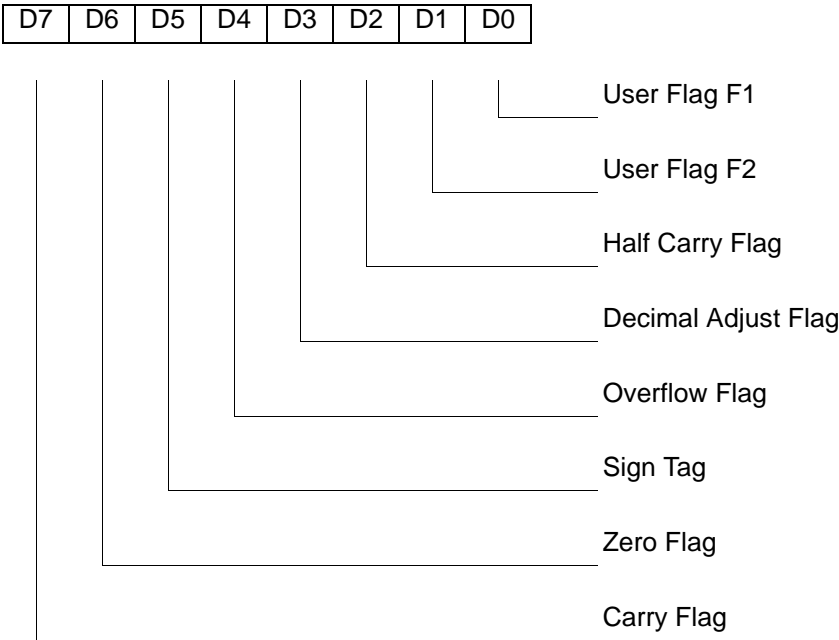
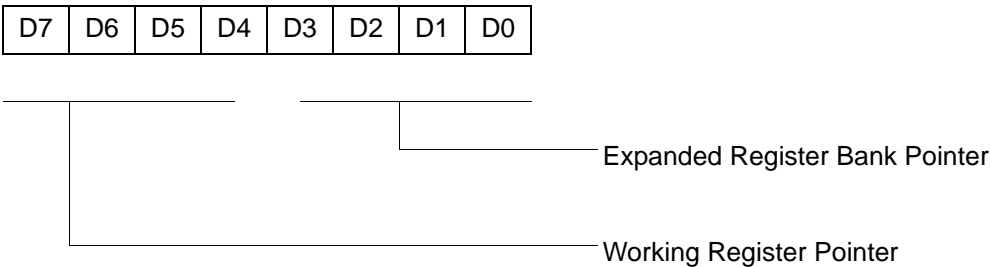


Figure 54. Flag Register (FCH: Read/Write)

R253 RP(FDH)



Default setting after reset = 0000 0000

Figure 55. Register Pointer (FDH: Read/Write)





R254 SPH(FEH)

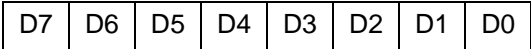


Figure 56. Stack Pointer High (FEH: Read/Write)

R255 SPL(FFH)

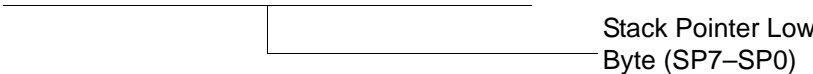
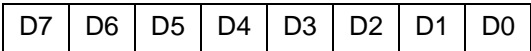


Figure 57. Stack Pointer Low (FFH: Read/Write)

## Package Information

Package information for all versions of ZGP323H is depicted in Figures 59 through Figure 68.

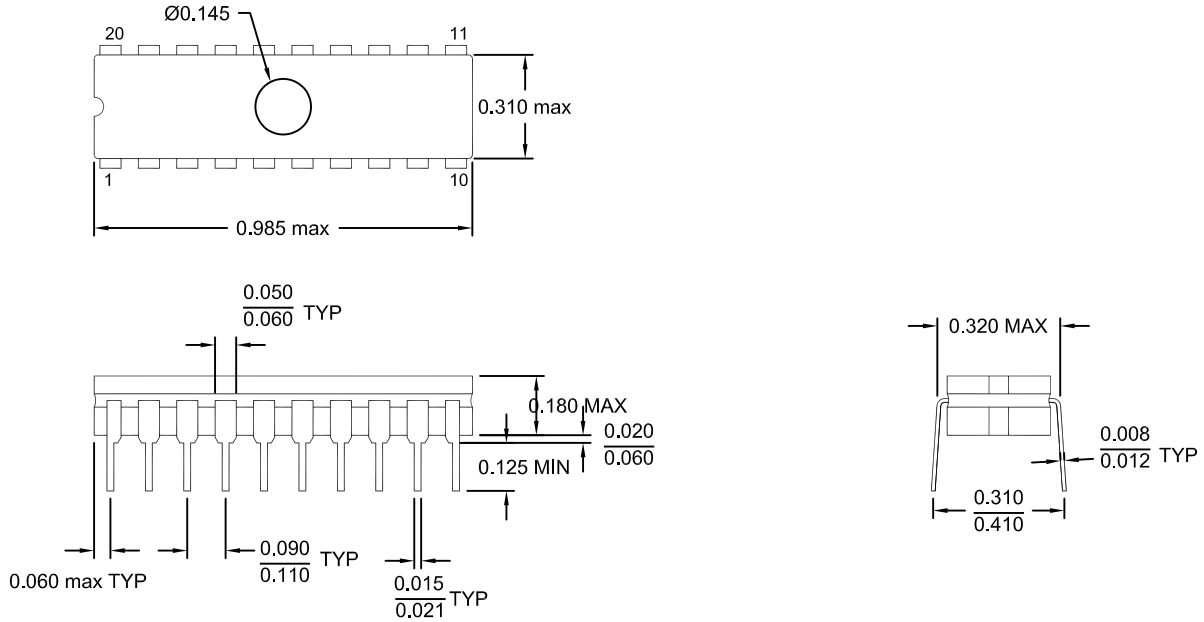


Figure 58. 20-Pin CDIP Package

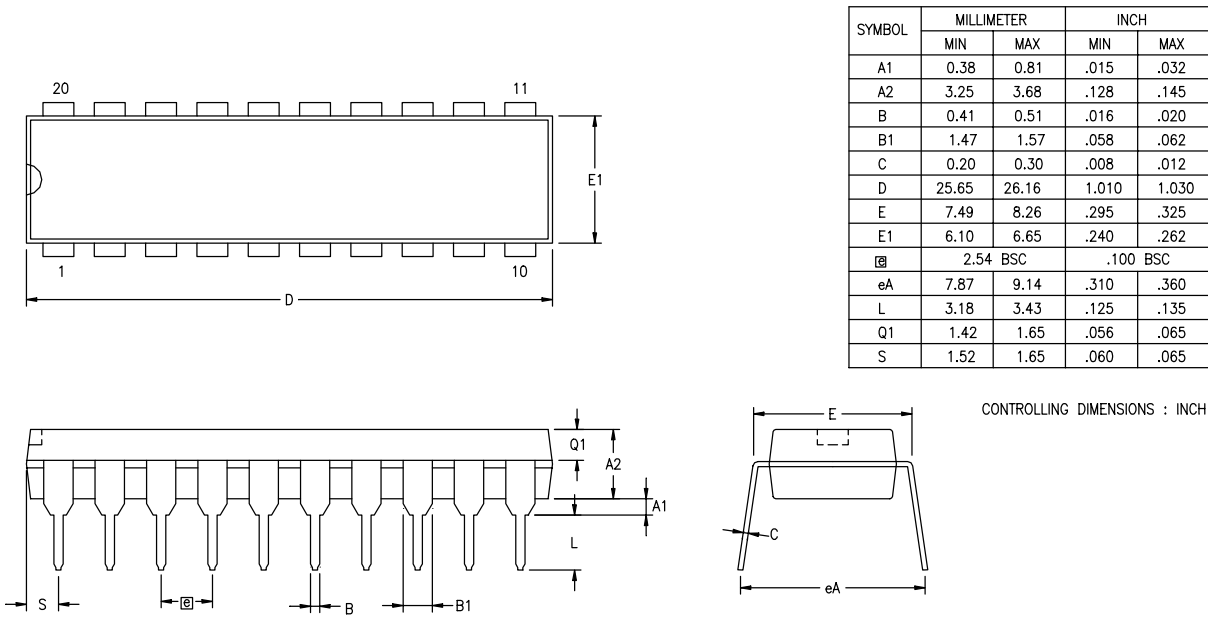
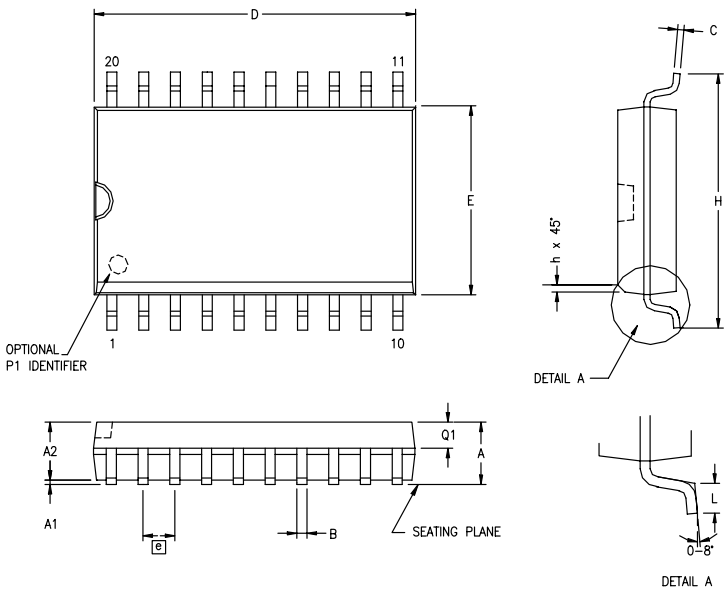


Figure 59. 20-Pin PDIP Package Diagram



SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A	2.40	2.65	.094	.104
A1	0.10	0.30	.004	.012
A2	2.24	2.44	.088	.096
B	0.36	0.46	.014	.018
C	0.23	0.30	.009	.012
D	12.60	12.95	.496	.510
E	7.40	7.60	.291	.299
g	1.27 BSC		.050 BSC	
H	10.00	10.65	.394	.419
h	0.30	0.40	.012	.016
L	0.60	1.00	.024	.039
Q1	0.97	1.07	.038	.042

CONTROLLING DIMENSIONS : MM  
 LEADS ARE COPLANAR WITHIN .004 INCH.

Figure 60. 20-Pin SOIC Package Diagram

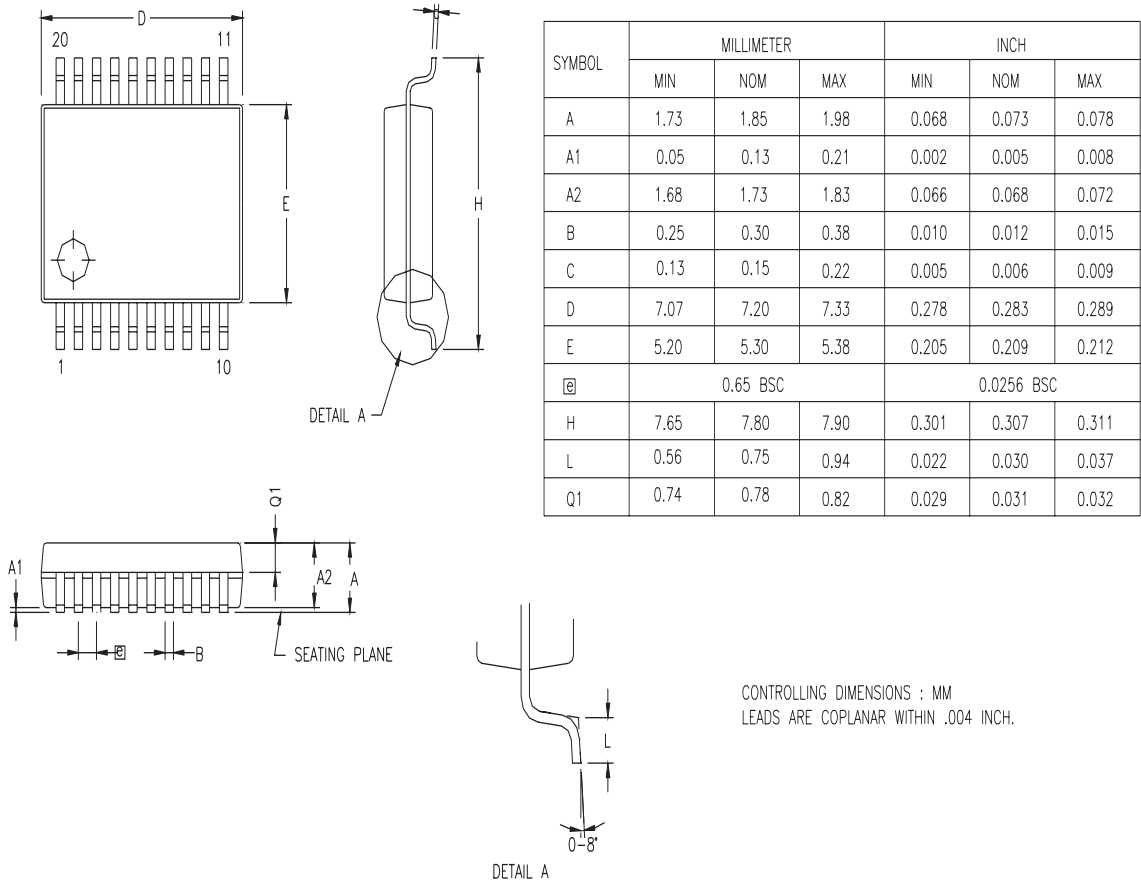
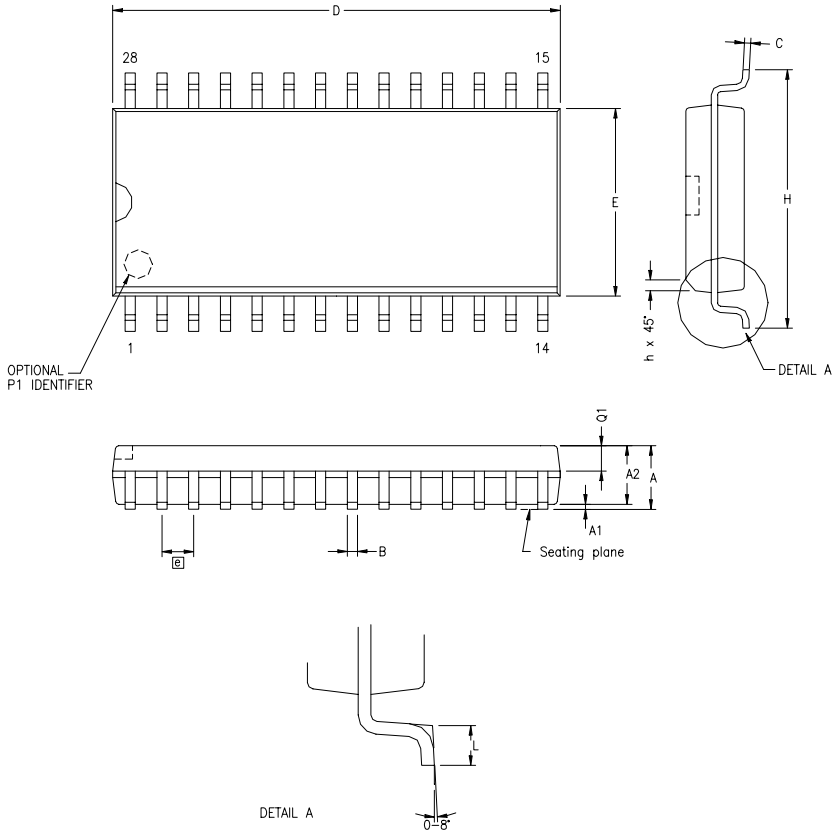


Figure 61. 20-Pin SSOP Package Diagram



SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A	2.40	2.64	.094	.104
A1	0.10	0.30	.004	.012
A2	2.24	2.44	.088	.096
B	0.36	0.46	.014	.018
C	0.23	0.30	.009	.012
D	17.78	18.00	.700	.710
E	7.40	7.60	.291	.299
Ⓜ	1.27 BSC		.050 BSC	
H	10.00	10.65	.394	.419
h	0.30	0.71	.012	.028
L	0.61	1.00	.024	.039
Q1	0.97	1.09	.038	.043

CONTROLLING DIMENSIONS : MM  
 LEADS ARE COPLANAR WITHIN .004 INCH.

Figure 62. 28-Pin SOIC Package Diagram

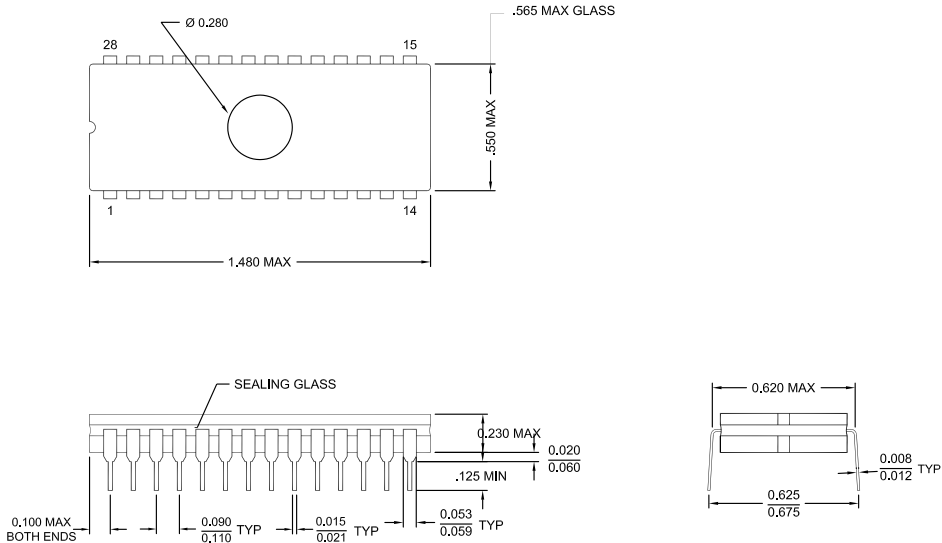
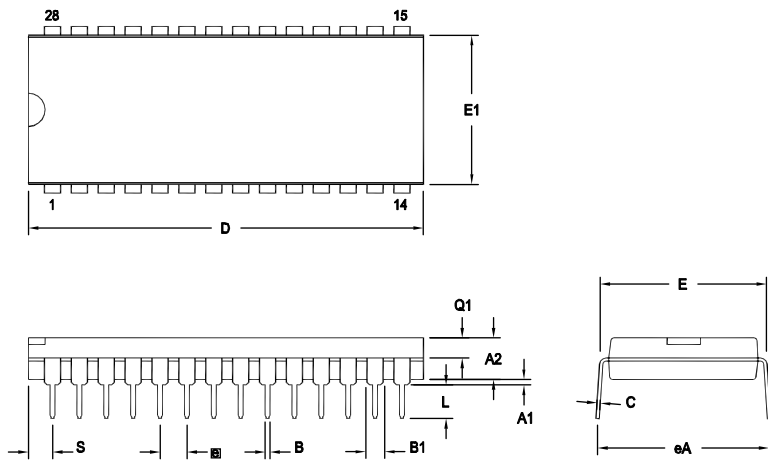


Figure 63. 28-Pin CDIP Package Diagram



SYMBOL	OPT #	MILLIMETER		INCH	
		MIN	MAX	MIN	MAX
A1		0.38	1.02	.015	.040
A2		3.18	4.19	.125	.165
B		0.38	0.53	.015	.021
B1	01	1.40	1.65	.055	.065
	02	1.14	1.40	.045	.055
C		0.23	0.38	.009	.015
D	01	36.58	37.34	1.440	1.470
	02	35.31	35.94	1.390	1.415
E		15.24	15.75	.600	.620
E1	01	13.59	14.10	.535	.555
	02	12.83	13.08	.505	.515
e		2.54 TYP		.100 BSC	
eA		15.49	16.76	.610	.660
L		3.05	3.81	.120	.150
Q1	01	1.40	1.91	.055	.075
	02	1.40	1.78	.055	.070
S	01	1.52	2.29	.060	.090
	02	1.02	1.52	.040	.060

CONTROLLING DIMENSIONS : INCH

OPTION TABLE	
OPTION #	PACKAGE
01	STANDARD
02	IDF

Note: ZILOG supplies both options for production. Component layout PCB design should cover bigger option 01.

Figure 64. 28-Pin PDIP Package Diagram

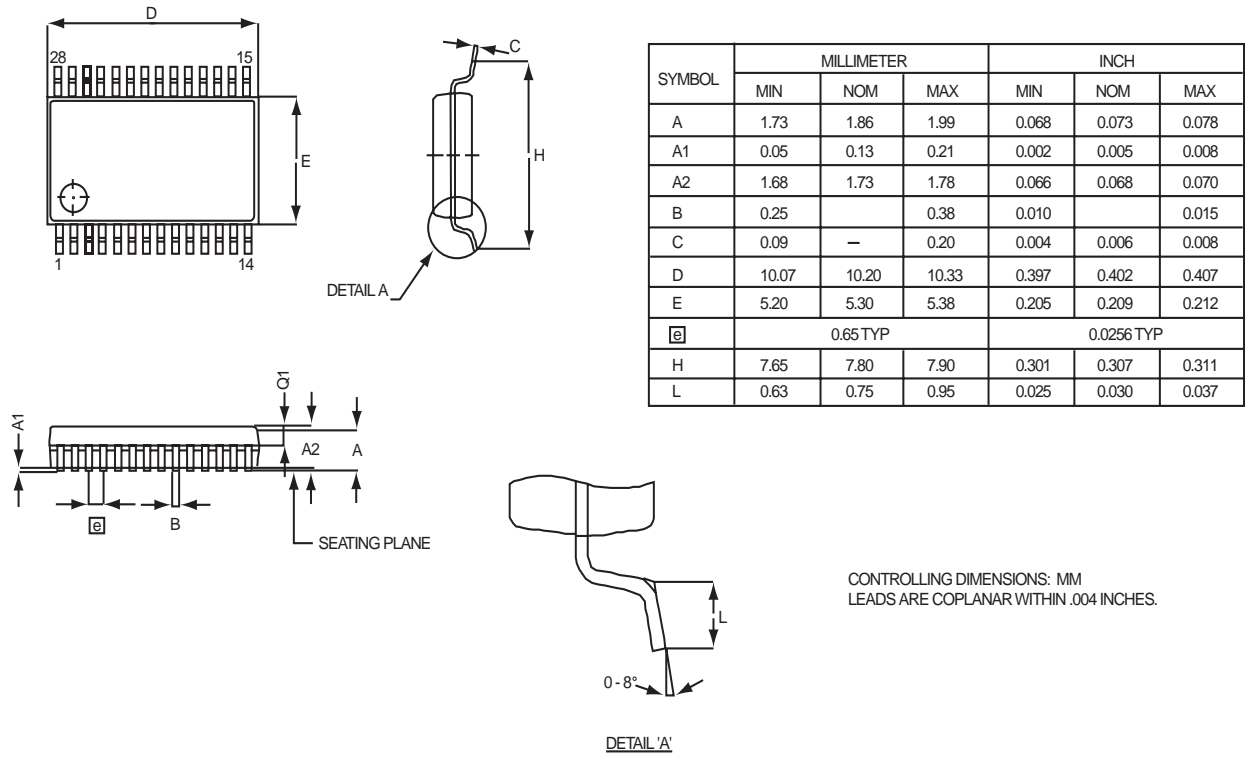


Figure 65. 28-Pin SSOP Package Diagram

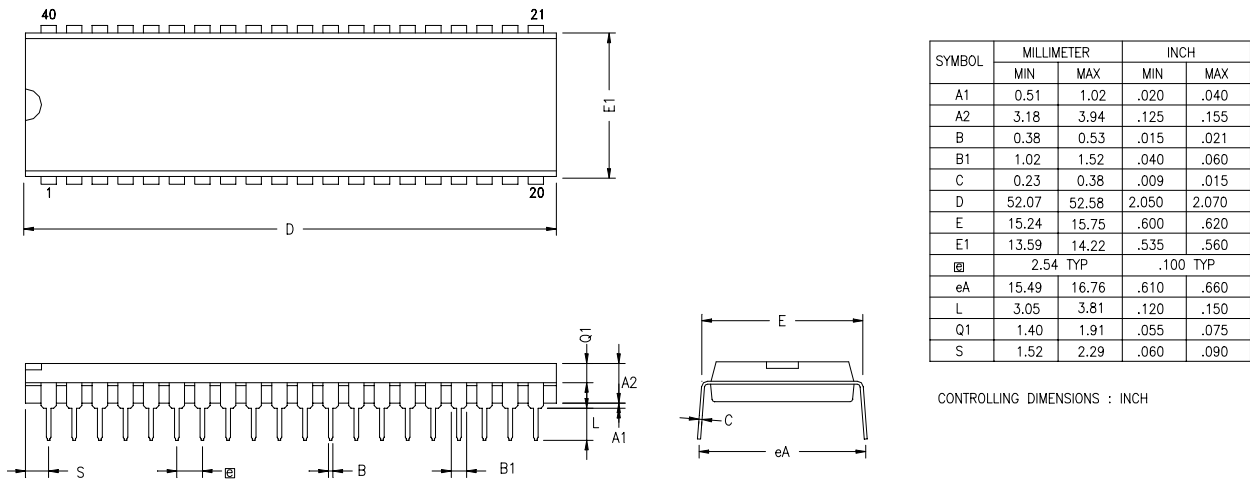


Figure 66. 40-Pin PDIP Package Diagram

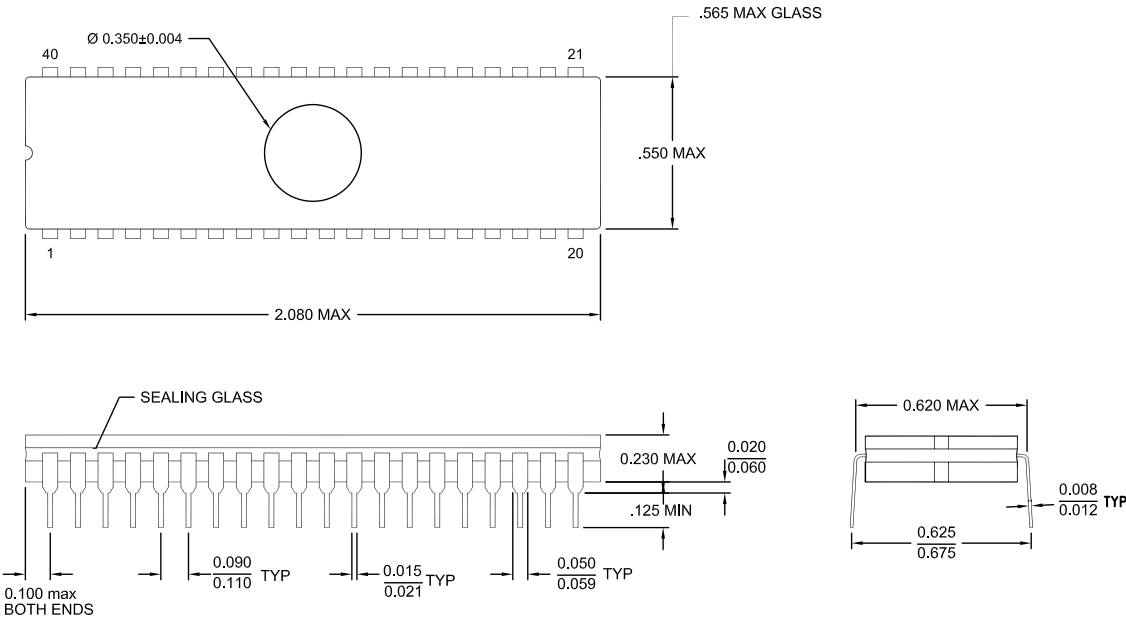
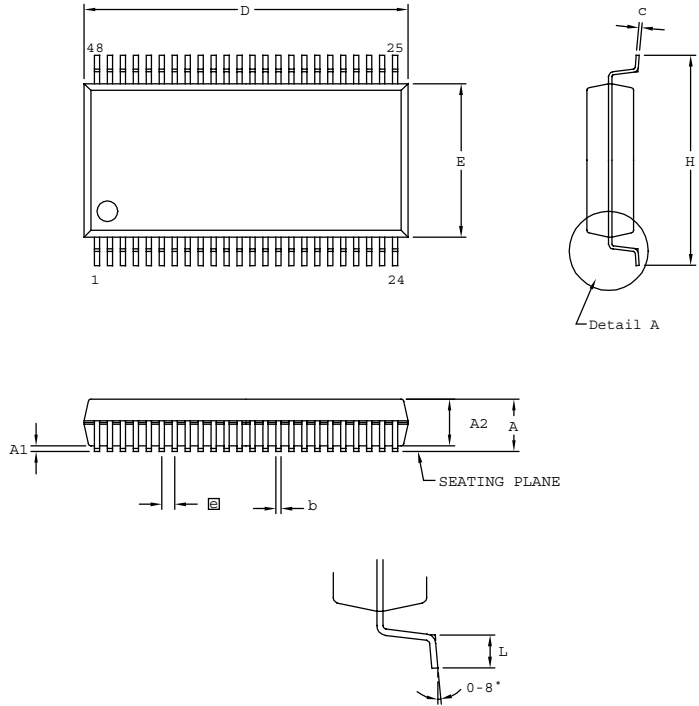


Figure 67. 40-Pin CDIP Package Diagram





SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A	2.41	2.79	0.095	0.110
A1	0.23	0.38	0.009	0.015
A2	2.18	2.39	0.086	0.094
b	0.20	0.34	0.008	0.0135
c	0.13	0.25	0.005	0.010
D	15.75	16.00	0.620	0.630
E	7.39	7.59	0.291	0.299
ⓐ	0.635 BSC		0.025 BSC	
H	10.16	10.41	0.400	0.410
L	0.51	1.016	0.020	0.040

CONTROLLING DIMENSIONS : MM  
LEADS ARE COPLANAR WITHIN .004 INCH

Figure 68. 48-Pin SSOP Package Design

► **Note:** Check with ZiLOG on the actual bonding diagram and coordinate for chip-on-board assembly.



## Ordering Information

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### 32KB Standard Temperature: 0° to +70°C

Part Number	Description	Part Number	Description
ZGP323HSH4832C	48-pin SSOP 32K OTP	ZGP323HSS2832C	28-pin SOIC 32K OTP
ZGP323HSP4032C	40-pin PDIP 32K OTP	ZGP323HSH2032C	20-pin SSOP 32K OTP
ZGP323HSK2832E	28-pin CDIP 32K OTP	ZGP323HSK2032E	20-pin CDIP 32K OTP
ZGP323HSK4032E	40-pin CDIP 32K OTP	ZGP323HSP2032C	20-pin PDIP 32K OTP
ZGP323HSH2832C	28-pin SSOP 32K OTP	ZGP323HSS2032C	20-pin SOIC 32K OTP
ZGP323HSP2832C	28-pin PDIP 32K OTP		

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### 32KB Extended Temperature: -40° to +105°C

Part Number	Description	Part Number	Description
ZGP323HEH4832C	48-pin SSOP 32K OTP	ZGP323HES2832C	28-pin SOIC 32K OTP
ZGP323HEP4032C	40-pin PDIP 32K OTP	ZGP323HEH2032C	20-pin SSOP 32K OTP
ZGP323HEH2832C	28-pin SSOP 32K OTP	ZGP323HEP2032C	20-pin PDIP 32K OTP
ZGP323HEP2832C	28-pin PDIP 32K OTP	ZGP323HES2032C	20-pin SOIC 32K OTP

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### 32KB Automotive Temperature: -40° to +125°C

Part Number	Description	Part Number	Description
ZGP323HAH4832C	48-pin SSOP 32K OTP	ZGP323HAS2832C	28-pin SOIC 32K OTP
ZGP323HAP4032C	40-pin PDIP 32K OTP	ZGP323HAH2032C	20-pin SSOP 32K OTP
ZGP323HAH2832C	28-pin SSOP 32K OTP	ZGP323HAP2032C	20-pin PDIP 32K OTP
ZGP323HAP2832C	28-pin PDIP 32K OTP	ZGP323HAS2032C	20-pin SOIC 32K OTP

Replace C with G for Lead-Free Packaging

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**16KB Standard Temperature: 0° to +70°C**

Part Number	Description	Part Number	Description
ZGP323HSH4816C	48-pin SSOP 16K OTP	ZGP323HSS2816C	28-pin SOIC 16K OTP
ZGP323HSP4016C	40-pin PDIP 16K OTP	ZGP323HSH2016C	20-pin SSOP 16K OTP
ZGP323HSH2816C	28-pin SSOP 16K OTP	ZGP323HSP2016C	20-pin PDIP 16K OTP
ZGP323HSP2816C	28-pin PDIP 16K OTP	ZGP323HSS2016C	20-pin SOIC 16K OTP

**16KB Extended Temperature: -40° to +105°C**

Part Number	Description	Part Number	Description
ZGP323HEH4816C	48-pin SSOP 16K OTP	ZGP323HES2816C	28-pin SOIC 16K OTP
ZGP323HEP4016C	40-pin PDIP 16K OTP	ZGP323HEH2016C	20-pin SSOP 16K OTP
ZGP323HEH2816C	28-pin SSOP 16K OTP	ZGP323HEP2016C	20-pin PDIP 16K OTP
ZGP323HEP2816C	28-pin PDIP 16K OTP	ZGP323HES2016C	20-pin SOIC 16K OTP

**16KB Automotive Temperature: -40° to +125°C**

Part Number	Description	Part Number	Description
ZGP323HAH4816C	48-pin SSOP 16K OTP	ZGP323HAS2816C	28-pin SOIC 16K OTP
ZGP323HAP4016C	40-pin PDIP 16K OTP	ZGP323HAH2016C	20-pin SSOP 16K OTP
ZGP323HAH2816C	28-pin SSOP 16K OTP	ZGP323HAP2016C	20-pin PDIP 16K OTP
ZGP323HAP2816C	28-pin PDIP 16K OTP	ZGP323HAS2016C	20-pin SOIC 16K OTP

Replace C with G for Lead-Free Packaging




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**8KB Standard Temperature: 0° to +70°C**

Part Number	Description	Part Number	Description
ZGP323HSH4808C	48-pin SSOP 8K OTP	ZGP323HSS2808C	28-pin SOIC 8K OTP
ZGP323HSP4008C	40-pin PDIP 8K OTP	ZGP323HSH2008C	20-pin SSOP 8K OTP
ZGP323HSH2808C	28-pin SSOP 8K OTP	ZGP323HSP2008C	20-pin PDIP 8K OTP
ZGP323HSP2808C	28-pin PDIP 8K OTP	ZGP323HSS2008C	20-pin SOIC 8K OTP

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**8KB Extended Temperature: -40° to +105°C**

Part Number	Description	Part Number	Description
ZGP323HEH4808C	48-pin SSOP 8K OTP	ZGP323HES2808C	28-pin SOIC 8K OTP
ZGP323HEP4008C	40-pin PDIP 8K OTP	ZGP323HEH2008C	20-pin SSOP 8K OTP
ZGP323HEH2808C	28-pin SSOP 8K OTP	ZGP323HEP2008C	20-pin PDIP 8K OTP
ZGP323HEP2808C	28-pin PDIP 8K OTP	ZGP323HES2008C	20-pin SOIC 8K OTP

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**8KB Automotive Temperature: -40° to +125°C**

Part Number	Description	Part Number	Description
ZGP323HAH4808C	48-pin SSOP 8K OTP	ZGP323HAS2808C	28-pin SOIC 8K OTP
ZGP323HAP4008C	40-pin PDIP 8K OTP	ZGP323HAH2008C	20-pin SSOP 8K OTP
ZGP323HAH2808C	28-pin SSOP 8K OTP	ZGP323HAP2008C	20-pin PDIP 8K OTP
ZGP323HAP2808C	28-pin PDIP 8K OTP	ZGP323HAS2008C	20-pin SOIC 8K OTP

Replace C with G for Lead-Free Packaging

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**4KB Standard Temperature: 0° to +70°C**

Part Number	Description	Part Number	Description
ZGP323HSH4804C	48-pin SSOP 4K OTP	ZGP323HSS2804C	28-pin SOIC 4K OTP
ZGP323HSP4004C	40-pin PDIP 4K OTP	ZGP323HSH2004C	20-pin SSOP 4K OTP
ZGP323HSH2804C	28-pin SSOP 4K OTP	ZGP323HSP2004C	20-pin PDIP 4K OTP
ZGP323HSP2804C	28-pin PDIP 4K OTP	ZGP323HSS2004C	20-pin SOIC 4K OTP

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**4KB Extended Temperature: -40° to +105°C**

Part Number	Description	Part Number	Description
ZGP323HEH4804C	48-pin SSOP 4K OTP	ZGP323HES2804C	28-pin SOIC 4K OTP
ZGP323HEP4004C	40-pin PDIP 4K OTP	ZGP323HEH2004C	20-pin SSOP 4K OTP
ZGP323HEH2804C	28-pin SSOP 4K OTP	ZGP323HEP2004C	20-pin PDIP 4K OTP
ZGP323HEP2804C	28-pin PDIP 4K OTP	ZGP323HES2004C	20-pin SOIC 4K OTP

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**4KB Automotive Temperature: -40° to +125°C**

Part Number	Description	Part Number	Description
ZGP323HAH4804C	48-pin SSOP 4K OTP	ZGP323HAS2804C	28-pin SOIC 4K OTP
ZGP323HAP4004C	40-pin PDIP 4K OTP	ZGP323HAH2004C	20-pin SSOP 4K OTP
ZGP323HAH2804C	28-pin SSOP 4K OTP	ZGP323HAP2004C	20-pin PDIP 4K OTP
ZGP323HAP2804C	28-pin PDIP 4K OTP	ZGP323HAS2004C	20-pin SOIC 4K OTP

Replace C with G for Lead-Free Packaging

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**Additional Components**

Part Number	Description	Part Number	Description
ZGP323ICE01ZEM	Emulator/programmer (For 3.6V Emulation only)	ZGP32300100ZPR	Programming system (Ethernet)
		ZGP32300200ZPR	Programming system (USB)



For fast results, contact your local ZiLOG sales office for assistance in ordering the part desired.

**Codes**

ZG = ZiLOG General Purpose Family

P = OTP

323 = Family Designation

H = High Voltage

T = Temperature

S = Standard 0° to +70°C

E = Extended -40° to +105°C

A = Automotive -40° to +125°C

P = Package Type:

K = CDIP

P = PDIP

H = SSOP

S = SOIC

## = Number of Pins

CC = Memory Size

M = Molding Compound

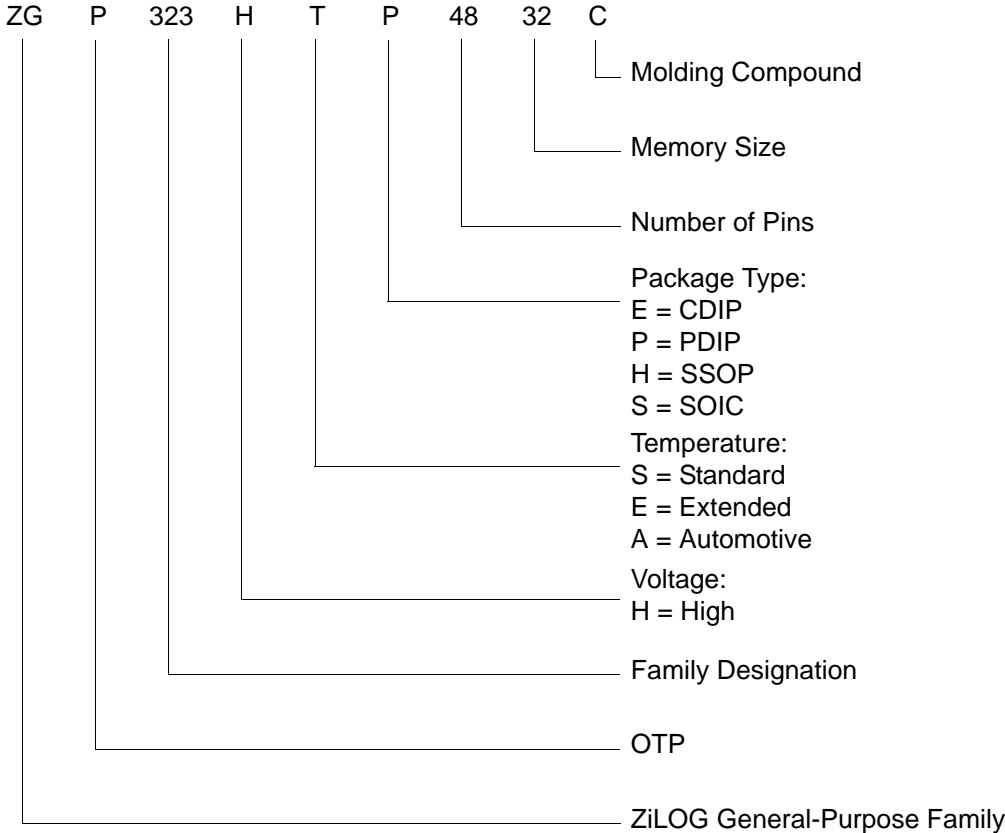
C = Standard Plastic Packaging Molding Compound

G = Green Plastic Molding Compound

E = Standard Cer Dip flow



Example



- Numerics
  - 16-bit counter/timer circuits 46
  - 20-pin DIP package diagram 82
  - 20-pin SSOP package diagram 84
  - 28-pin DIP package diagram 86
  - 28-pin SOIC package diagram 85
  - 28-pin SSOP package diagram 87
  - 40-pin DIP package diagram 87
  - 48-pin SSOP package diagram 89
  - 8-bit counter/timer circuits 42
- A
  - absolute maximum ratings 10
- AC
  - characteristics 16
  - timing diagram 16
- address spaces, basic 2
- architecture 2
  - expanded register file 28
- B
  - basic address spaces 2
  - block diagram, ZLP32300 functional 3
- C
  - capacitance 11
  - characteristics
    - AC 16
    - DC 11
  - clock 53
  - comparator inputs/outputs 25
  - configuration
    - port 0 19
    - port 1 20
    - port 2 21
    - port 3 22
    - port 3 counter/timer 24
  - counter/timer
    - 16-bit circuits 46
    - 8-bit circuits 42
    - brown-out voltage/standby 64
    - clock 53
    - demodulation mode count capture flow-  
chart 44
    - demodulation mode flowchart 45
    - EPROM selectable options 64
    - glitch filter circuitry 40
    - halt instruction 54
    - input circuit 40
    - interrupt block diagram 51
    - interrupt types, sources and vectors 52
    - oscillator configuration 53
    - output circuit 49
    - ping-pong mode 48
    - port configuration register 55
    - resets and WDT 63
    - SCLK circuit 58
    - stop instruction 54
    - stop mode recovery register 57
    - stop mode recovery register 2 61
    - stop mode recovery source 59
    - T16 demodulation mode 47
    - T16 transmit mode 46
    - T16\_OUT in modulo-N mode 47
    - T16\_OUT in single-pass mode 47
    - T8 demodulation mode 43
    - T8 transmit mode 40
    - T8\_OUT in modulo-N mode 43
    - T8\_OUT in single-pass mode 43
    - transmit mode flowchart 41
    - voltage detection and flags 65
    - watch-dog timer mode register 62
    - watch-dog timer time select 63
- CTR(D)01h T8 and T16 Common Functions 35
- D
  - DC characteristics 11
  - demodulation mode
    - count capture flowchart 44
    - flowchart 45
    - T16 47
    - T8 43
  - description
    - functional 25
    - general 2



- pin 4
- E
- EPROM
  - selectable options 64
- expanded register file 26
- expanded register file architecture 28
- expanded register file control registers 71
  - flag 80
  - interrupt mask register 79
  - interrupt priority register 78
  - interrupt request register 79
  - port 0 and 1 mode register 77
  - port 2 configuration register 75
  - port 3 mode register 76
  - port configuration register 75
  - register pointer 80
  - stack pointer high register 81
  - stack pointer low register 81
  - stop-mode recovery register 73
  - stop-mode recovery register 2 74
  - T16 control register 69
  - T8 and T16 common control functions register 67
  - T8/T16 control register 70
  - TC8 control register 66
  - watch-dog timer register 75
- F
- features
  - standby modes 1
- functional description
  - counter/timer functional blocks 40
    - CTR(D)01h register 35
    - CTR0(D)00h register 33
    - CTR2(D)02h register 37
    - CTR3(D)03h register 39
  - expanded register file 26
  - expanded register file architecture 28
  - HI16(D)09h register 32
  - HI8(D)0Bh register 32
  - L08(D)0Ah register 32
  - L0I6(D)08h register 32
  - program memory map 26
  - RAM 25
  - register description 65
  - register file 30
  - register pointer 29
  - register pointer detail 31
  - SMR2(F)0D1h register 40
  - stack 31
  - TC16H(D)07h register 32
  - TC16L(D)06h register 33
  - TC8H(D)05h register 33
  - TC8L(D)04h register 33
- G
- glitch filter circuitry 40
- H
- halt instruction, counter/timer 54
- I
- input circuit 40
- interrupt block diagram, counter/timer 51
- interrupt types, sources and vectors 52
- L
- low-voltage detection register 65
- M
- memory, program 25
- modulo-N mode
  - T16\_OUT 47
  - T8\_OUT 43
- O
- oscillator configuration 53
- output circuit, counter/timer 49
- P
- package information
  - 20-pin DIP package diagram 82
  - 20-pin SSOP package diagram 84
  - 28-pin DIP package diagram 86
  - 28-pin SOIC package diagram 85
  - 28-pin SSOP package diagram 87
  - 40-pin DIP package diagram 87
  - 48-pin SSOP package diagram 89
- pin configuration
  - 20-pin DIP/SOIC/SSOP 5

- 28-pin DIP/SOIC/SSOP 6
- 40- and 48-pin 8
- 40-pin DIP 7
- 48-pin SSOP 8
- pin functions
  - port 0 (P07 - P00) 18
  - port 0 (P17 - P10) 19
  - port 0 configuration 19
  - port 1 configuration 20
  - port 2 (P27 - P20) 20
  - port 2 (P37 - P30) 21
  - port 2 configuration 21
  - port 3 configuration 22
  - port 3 counter/timer configuration 24
  - reset) 25
  - XTAL1 (time-based input 18
  - XTAL2 (time-based output) 18
- ping-pong mode 48
- port 0 configuration 19
- port 0 pin function 18
- port 1 configuration 20
- port 1 pin function 19
- port 2 configuration 21
- port 2 pin function 20
- port 3 configuration 22
- port 3 pin function 21
- port 3 counter/timer configuration 24
- port configuration register 55
- power connections 3
- power supply 5
- program memory 25
  - map 26
- R
- ratings, absolute maximum 10
- register 61
  - CTR(D)01h 35
  - CTR0(D)00h 33
  - CTR2(D)02h 37
  - CTR3(D)03h 39
  - flag 80
  - HI16(D)09h 32
  - HI8(D)0Bh 32
  - interrupt priority 78
  - interrupt request 79
  - interruptmask 79
  - L016(D)08h 32
  - L08(D)0Ah 32
  - LVD(D)0Ch 65
  - pointer 80
  - port 0 and 1 77
  - port 2 configuration 75
  - port 3 mode 76
  - port configuration 55, 75
  - SMR2(F)0Dh 40
  - stack pointer high 81
  - stack pointer low 81
  - stop mode recovery 57
  - stop mode recovery 2 61
  - stop-mode recovery 73
  - stop-mode recovery 2 74
  - T16 control 69
  - T8 and T16 common control functions 67
  - T8/T16 control 70
  - TC16H(D)07h 32
  - TC16L(D)06h 33
  - TC8 control 66
  - TC8H(D)05h 33
  - TC8L(D)04h 33
  - voltage detection 71
  - watch-dog timer 75
- register description
  - Counter/Timer2 LS-Byte Hold 33
  - Counter/Timer2 MS-Byte Hold 32
  - Counter/Timer8 Control 33
  - Counter/Timer8 High Hold 33
  - Counter/Timer8 Low Hold 33
  - CTR2 Counter/Timer 16 Control 37
  - CTR3 T8/T16 Control 39
  - Stop Mode Recovery2 40
  - T16\_Capture\_LO 32
  - T8 and T16 Common functions 35
  - T8\_Capture\_HI 32

T8\_Capture\_LO 32  
 register file 30  
     expanded 26  
 register pointer 29  
     detail 31

reset pin function 25  
 resets and WDT 63

## S

SCLK circuit 58  
 single-pass mode  
     T16\_OUT 47  
     T8\_OUT 43

stack 31  
 standard test conditions 10  
 standby modes 1  
 stop instruction, counter/timer 54  
 stop mode recovery  
     2 register 61  
     source 59

stop mode recovery 2 61  
 stop mode recovery register 57

## T

T16 transmit mode 46  
 T16\_Capture\_HI 32  
 T8 transmit mode 40  
 T8\_Capture\_HI 32  
 test conditions, standard 10  
 test load diagram 10  
 timing diagram, AC 16  
 transmit mode flowchart 41

## V

VCC 5  
 voltage  
     brown-out/standby 64  
     detection and flags 65  
 voltage detection register 71

## W

watch-dog timer  
     mode registerwatch-dog timer mode regis-  
         ter 62  
     time select 63

## X

XTAL1 5  
 XTAL1 pin function 18  
 XTAL2 5  
 XTAL2 pin function 18