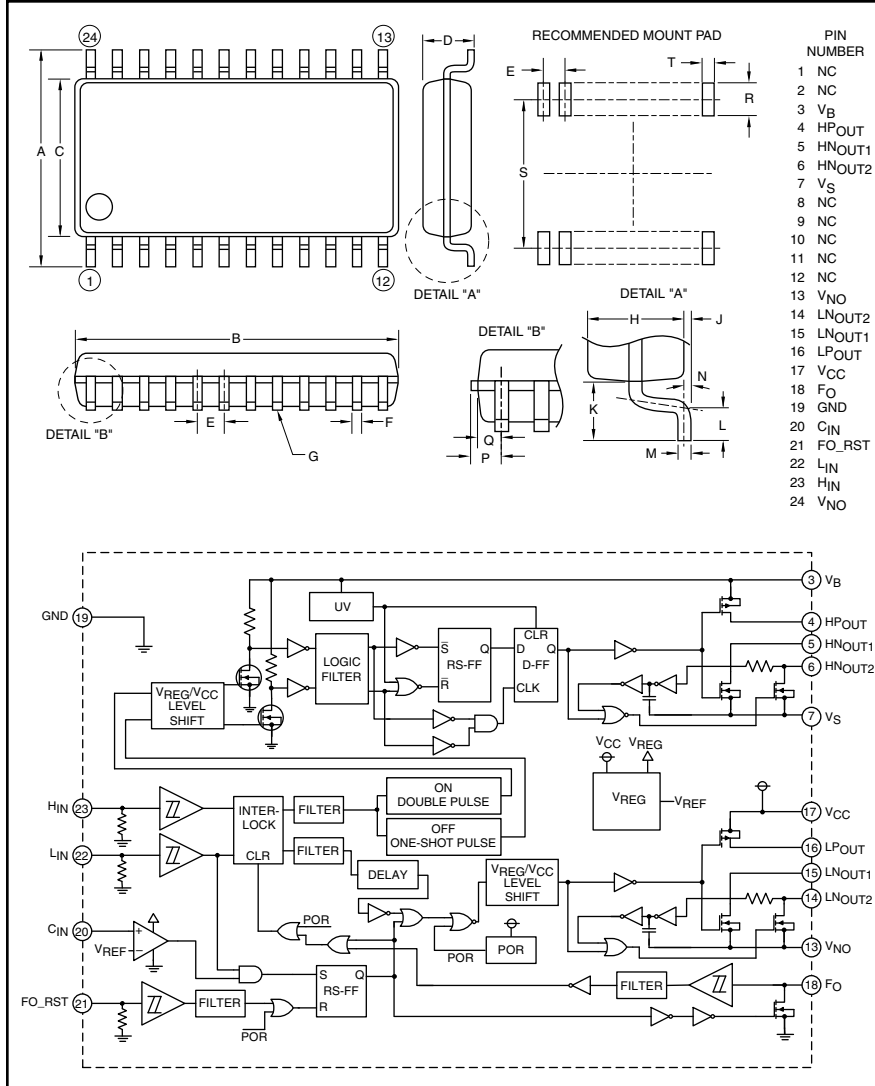


### HVIC High Voltage Half-Bridge Driver 1200 Volts/±1 Ampere



**Description:**  
M81019FP is a high voltage Power MOSFET and IGBT driver for half-bridge applications.

- Features:**
- Shoot Through Interlock
  - Output Current ±1 Ampere
  - Half-Bridge Driver
  - 24-Lead SSOP Package
  - Internal Dead Time - Fixed

- Applications:**
- HID Ballast
  - PDP
  - MOSFET Driver
  - IGBT Driver
  - Inverter Module Control

**Ordering Information:**  
M81019FP is a ±1 Ampere, 1200 Volt HVIC, High Voltage Half-Bridge Driver

Outline Drawing and Circuit Diagram

Dimensions	Inches	Millimeters
A	0.31±0.01	7.8±0.3
B	0.40±0.004	10.1±0.1
C	0.21±0.004	5.3±0.1
D	0.08 Max.	2.1 Max.
E	0.03	0.8
F	0.01+0.004/0.002	0.35±0.1/-0.05
G	0.004	0.1
H	0.07	1.8
J	0.008 Max.	0.2 Max.

Dimensions	Inches	Millimeters
K	0.05	1.25
L	0.02±0.008	0.6±0.2
M	0.008+0.002/-0.008	0.2+0.05/-0.2
N	8° Max.	8° Max.
P	0.03 Max.	0.8 Max.
Q	0.026	0.65
R	0.051 Min.	1.27 Min.
S	0.30	7.62
T	0.02	0.5



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**M81019FP**

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1200 Volts/±1 Ampere

**Absolute Maximum Ratings,  $T_a = 25^\circ\text{C}$  unless otherwise specified**

Characteristics	Symbol	M81019FP	Units
High Side Floating Supply Absolute Voltage	$V_B$	-0.5 ~ 1224	Volts
High Side Floating Supply Offset Voltage	$V_S$	$V_B-24 \sim V_B+0.5$	Volts
High Side Floating Supply Voltage ( $V_{BS} = V_B - V_S$ )	$V_{BS}$	-0.5 ~ 24	Volts
High Side Output Voltage	$V_{HO}$	$V_S-0.5 \sim V_B+0.5$	Volts
Low Side Fixed Supply Voltage	$V_{CC}$	-0.5 ~ 24	Volts
Power Ground	$V_{NO}$	$V_{CC}-24 \sim V_{CC}+0.5$	Volts
Low Side Output Voltage	$V_{LO}$	$V_{NO}-0.5 \sim V_{CC}+0.5$	Volts
Logic Input Voltage ( $H_{IN}, L_{IN}, FO\_RST$ )	$V_{IN}$	-0.5 ~ $V_{CC}+0.5$	Volts
$F_O$ Input/Output Voltage	$V_{FO}$	-0.5 ~ $V_{CC}+0.5$	Volts
$C_{IN}$ Input Voltage	$V_{CIN}$	-0.5 ~ $V_{CC}+0.5$	Volts
Allowable Offset Voltage Slew Rate	dVs/dt	±50	V/ns
Package Power Dissipation ( $T_a = 25^\circ\text{C}$ , On Board)	$P_d$	~1.6	Watts
Linear Derating Factor ( $T_a > 25^\circ\text{C}$ , On Board)	$K_\theta$	~16	mW/°C
Junction to Case Thermal Resistance	$R_{th(j-c)}$	~60	°C/W
Junction Temperature	$T_j$	-20 ~ 150	°C
Operation Temperature	$T_{opr}$	-20 ~ 125	°C
Storage Temperature	$T_{stg}$	-40 ~ 150	°C

**Recommended Operating Conditions**

All voltage parameters are absolute voltages referenced to GND unless otherwise specified.

Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Units
High Side Floating Supply Absolute Voltage	$V_B$		$V_S+13.5$	$V_S+15$	$V_S+20$	Volts
High Side Floating Supply Offset Voltage	$V_S$	$V_{BS} > 10V$	-5*	—	900**	Volts
High Side Floating Supply Voltage	$V_{BS}$	$V_B = V_B - V_S$	13.5	15	20	Volts
High Side Output Voltage	$V_{HO}$		$V_S$	—	$V_S+20$	Volts
Low Side Fixed Supply Voltage	$V_{CC}$		13.5	—	20	Volts
Power Ground	$V_{NO}$		-5	—	5	Volts
Low Side Output Voltage	$V_{LO}$		$V_{NO}$	—	$V_{CC}$	Volts
Logic Input Voltage	$V_{IN}$	$H_{IN}, L_{IN}, FO\_RST$	—	5	$V_{CC}$	Volts
$F_O$ Input/Output Voltage	$V_{FO}$		—	—	$V_{CC}$	Volts
$C_{IN}$ Input Voltage	$V_{CIN}$		—	—	5	Volts
Allowable Offset Voltage Slew Rate***	dVs/dt		-8	—	8	KV/μs

\*The lowest logic operational condition for  $V_S$  is -5V. The lowest state held condition for  $V_S$  is  $-V_{BS}$ . The surge of  $-V_S$  should not exceed -100V to avoid improper operation of output.

\*\*The maximum of allowable instantaneous voltage spike is up to 1200V.

\*\*\*At operation mode, dVs/dt should not go beyond recommended operation conditions or it will cause improper operation output.



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1200 Volts/±1 Ampere

**Electrical Characteristics,  $T_a = 25^\circ\text{C}$ ,  $V_{CC} = V_{BS} (= V_B - V_S) = 15\text{V}$  unless otherwise specified**

Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Units
High Side Leakage Current	$I_{FS}$	$V_B = V_S = 1200\text{V}$	—	—	1.0	$\mu\text{A}$
$V_{BS}$ Quiescent Supply Current	$I_{BS}$	$H_{IN} = L_{IN} = 0\text{V}$	—	0.4	0.8	mA
$V_{CC}$ Quiescent Supply Current	$I_{CC}$	$H_{IN} = L_{IN} = 0\text{V}$	—	0.9	1.5	mA
High Level Output Voltage	$V_{OH}$	$I_O = -20\text{mA}$ , $H_{POUT}$ , $L_{POUT}$	14.5	—	—	Volts
Low Level Output Voltage	$V_{OL}$	$I_O = 20\text{mA}$ , $H_{NOUT1}$ , $L_{NOUT1}$	—	—	0.5	Volts
High Level Input Threshold Voltage	$V_{IH}$	$H_{IN}$ , $L_{IN}$ , $FO\_RST$	3.0	—	—	Volts
Low Level Input Threshold Voltage	$V_{IL}$	$H_{IN}$ , $L_{IN}$ , $FO\_RST$	—	—	1.5	Volts
High Level Input Bias Current	$I_{IH}$	$V_{IN} = 5\text{V}$	—	1.0	1.4	mA
Low Level Input Bias Current	$I_{IL}$	$V_{IN} = 0\text{V}$	-1.0	—	—	$\mu\text{A}$
Input Signals Filter Time	$t_{Filter}$	$H_{IN}$ , $L_{IN}$ , $FO\_RST$ , $F_O$	100	200	400	ns
High Side Low Impedance	$V_{HNO2}$	$V_{IN} = 0\text{V}$	2.5	3.4	5.0	Volts
NMOS Input Threshold Voltage						
Low Side Low Impedance	$V_{LNO2}$	$V_{IN} = 0\text{V}$	6.5	7.6	9.0	Volts
NMOS Input Threshold Voltage						
Low Impedance NMOS Filter Time	$t_{VNO2}$	$V_{IN} = 0\text{V}$	200	400	650	ns
Low Level $F_O$ Output Voltage	$V_{OLFO}$	$I_{FO} = 1\text{mA}$	—	—	0.95	Volts
High Level $F_O$ Input Threshold Voltage	$V_{IHFO}$	—	3.0	—	—	Volts
Low Level $F_O$ Input Threshold Voltage	$V_{ILFO}$	—	—	—	1.5	Volts
$V_{BS}$ Supply UV Reset Voltage	$V_{BSuvr}$	—	10.5	11.3	12.1	Volts
$V_{BS}$ Supply UV Trip Voltage	$V_{BSuvt}$	—	10.0	10.8	11.6	Volts
$V_{BS}$ Supply UV Hysteresis Voltage	$V_{BSuvh}$	$V_{BSuvh} = V_{BSuvr} - V_{BSuvt}$	0.3	0.5	0.8	Volts
$V_{BS}$ Supply UV Filter Time	$t_{VBSuv}$	—	4.0	8.0	16.0	$\mu\text{s}$
$C_{IN}$ Trip Voltage	$V_{CIN}$	—	0.4	0.5	0.6	Volts
POR Trip Voltage	$V_{POR}$	—	4.5	5.5	7.0	Volts
Output High Level Short Circuit Pulsed Current	$I_{OH}$	$H_{POUT}(L_{POUT}) = 0\text{V}$ , $H_{IN} = 5\text{V}$ , $P_W < 5\mu\text{s}$	—	1.0	—	A
Output Low Level Short Circuit Pulsed Current	$I_{OL1}$	$H_{NOUT1}(L_{NOUT1}) = 15\text{V}$ , $L_{IN} = 5\text{V}$ , $P_W < 5\mu\text{s}$	—	-1.0	—	A
Low Impedance NMOS Output Low Level Short Circuit Pulsed Current	$I_{OL2}$	$H_{NOUT2}(L_{NOUT2}) = 15\text{V}$ , $L_{IN} = 5\text{V}$ , $P_W < 5\mu\text{s}$	—	-1.0	—	A
Output High Level ON Resistance	$R_{OH}$	$I_O = -200\text{mA}$ , $R_{OH} = (V_{OH} - V_O)/I_O$	—	15	—	$\Omega$
Output Low Level ON Resistance	$R_{OL1}$	$I_O = 200\text{mA}$ , $R_{OL1} = V_O/I_O$	—	15	—	$\Omega$
Low Impedance NMOS Output Low Level ON Resistance	$R_{OL2}$	$I_O = 200\text{mA}$ , $R_{OL2} = V_O/I_O$	—	15	—	$\Omega$

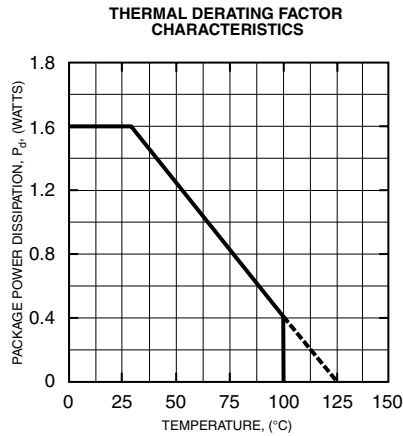


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**M81019FP**  
**HVIC, High Voltage Half-Bridge Driver**  
 1200 Volts/±1 Ampere

**Electrical Characteristics,  $T_a = 25^\circ\text{C}$ ,  $V_{CC} = V_{BS} (= V_B - V_S) = 15\text{V}$  unless otherwise specified**

Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Units
High Side Turn-On Propagation Delay	$t_{dLH(HO)}$	HPOUT Short to HNOUT1 & HNOUT2, $C_L = 1\text{nF}$	1.0	1.29	1.6	$\mu\text{s}$
High Side Turn-Off Propagation Delay	$t_{dHL(HO)}$	HPOUT Short to HNOUT1 & HNOUT2, $C_L = 1\text{nF}$	0.9	1.19	1.5	$\mu\text{s}$
Low Side Turn-On Propagation Delay	$t_{dLH(LO)}$	LPOUT Short to LNOUT1 & LNOUT2, $C_L = 1\text{nF}$	1.0	1.27	1.6	$\mu\text{s}$
Low Side Turn-Off Propagation Delay	$t_{dHL(LO)}$	LPOUT Short to LNOUT1 & LNOUT2, $C_L = 1\text{nF}$	0.9	1.21	1.5	$\mu\text{s}$
Output Turn-On Rise Time	$t_r$	$C_L = 1\text{nF}$	—	40.0	—	ns
Output Turn-Off Fall Time	$t_f$	$C_L = 1\text{nF}$	—	40.0	—	ns
Delay Matching, High Side Turn-On & Low Side Turn-Off	$\Delta t_{dLH}$	$t_{dLH(HO)} - t_{dLH(LO)}$	—	80.0	—	ns
Delay Matching, High Side Turn-Off & Low Side Turn-On	$\Delta t_{dHL}$	$t_{dHL(HO)} - t_{dHL(LO)}$	—	80.0	—	ns

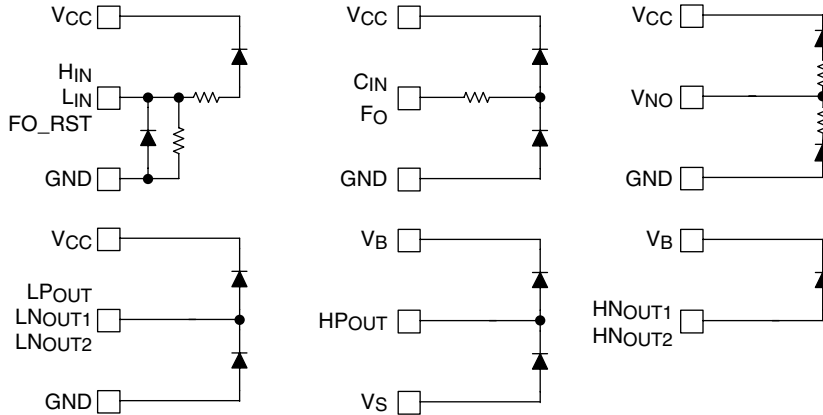


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DIODE CLAMP CIRCUITS FOR INPUT AND OUTPUT PINS



FUNCTION TABLE (X = H or L; Z = High Impedance; Q = Keep Previous Status)

H <sub>IN</sub>	L <sub>IN</sub>	FO_RST	C <sub>IN</sub>	FO (Input)	V <sub>BS</sub> /U <sub>V</sub>	V <sub>CC</sub> /P <sub>OR</sub>	H <sub>O</sub>	L <sub>O</sub>	FO (Output)	Behavioral State
L	L	L	L	-	H	H	L	L	H	
L	H	L	L	-	H	H	L	H	H	
H	L	L	L	-	H	H	H	L	H	
H	H	L	L	-	H	H	Q	Q	H	For Interlock
X	H	X	H	-	X	H	L	L	L	C <sub>IN</sub> Tripped When L <sub>IN</sub> = H
X	L	X	H	-	X	H	Q	Q	H	C <sub>IN</sub> Not Tripped When L <sub>IN</sub> = L
X	X	X	X	L	X	H	L	L	L	Output Shut Down When FO = L
X	X	X	X	-	X	L	L	L	H	V <sub>CC</sub> Power Reset Tripped
X	L	L	L	-	L	H	L	L	H	V <sub>BS</sub> Power Reset Tripped
X	H	L	L	-	L	H	L	H	H	V <sub>BS</sub> Power Reset Tripped When L <sub>IN</sub> = H

NOTE: "L" status of V<sub>BS</sub>/U<sub>V</sub> indicates high side UV tripped.

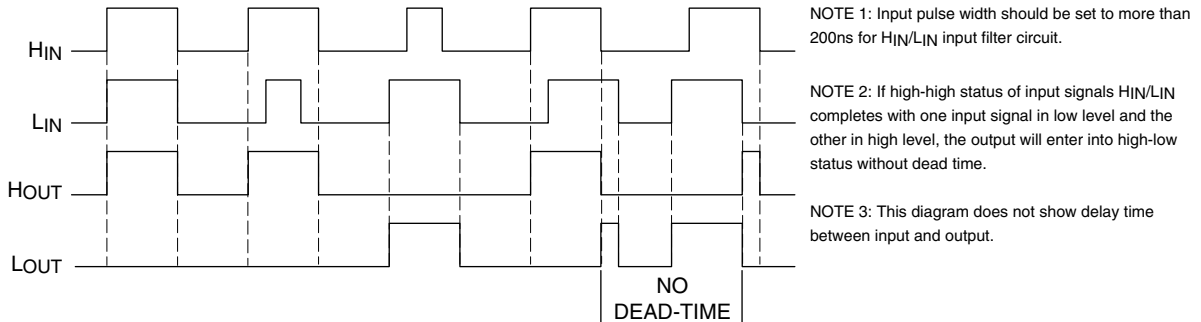
"L" status of V<sub>CC</sub>/P<sub>OR</sub> indicates V<sub>CC</sub> power reset tripped.

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**TIMING DIAGRAM**

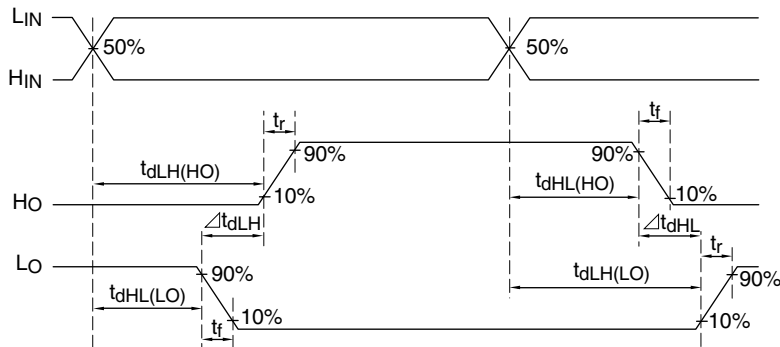
**1. Input Interlock Timing Diagram**

When the input signals ( $H_{IN}/L_{IN}$ ) are high at the same time, the output ( $H_{OUT}/L_{OUT}$ ) will maintain previous status. But if the input signals ( $H_{IN}/L_{IN}$ ) go high simultaneously,  $H_{IN}$  signals would be active and cause  $H_{OUT}$  to enter into high status.



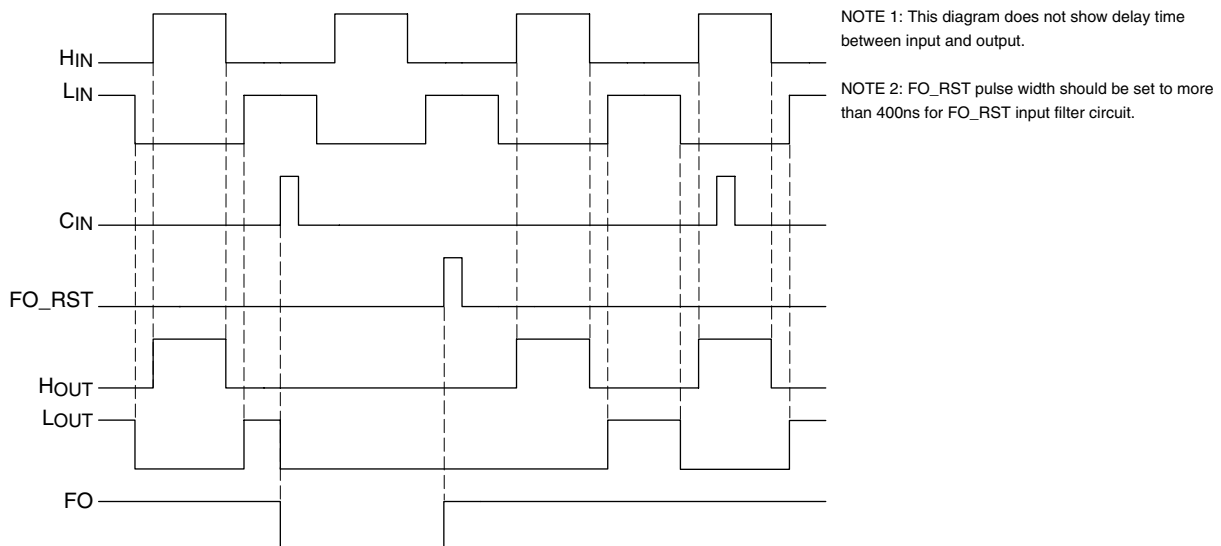
**2. Input/Output Timing Diagram**

The M81019FP matches delay between the low side and high side driver allowing minimized dead time control for better speed range and torque control in motor drive applications.



**3. Short Circuit Protection Timing Diagram**

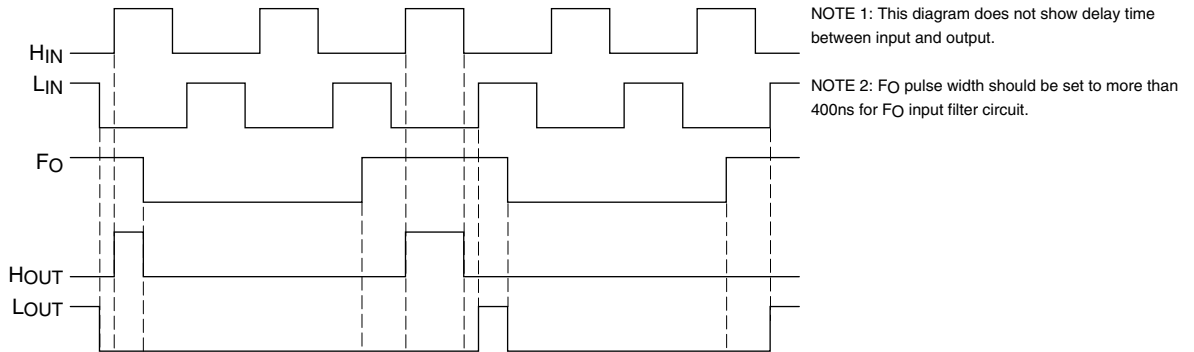
When overcurrent is detected,  $C_{IN}$  will be tripped if  $L_{IN}$  is high; then the short circuit protection will activate and shut down the outputs and  $F_O$  will indicate fault by going low. As soon as  $F_O\_RST$  is driven high, short circuit protection will deactivate and  $F_O$  goes high. The output will then respond to any subsequent active input signal.



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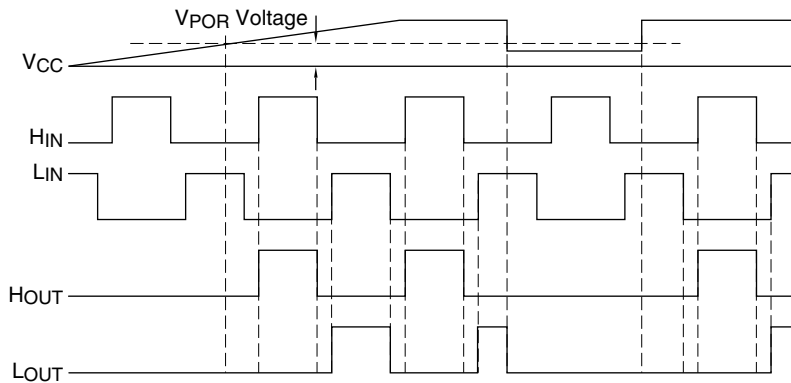
4. FO Input Timing Diagram

When FO is pulled low by an external signal, the output will be shut down. As soon as FO goes high again, the output will respond to the next active input signal.



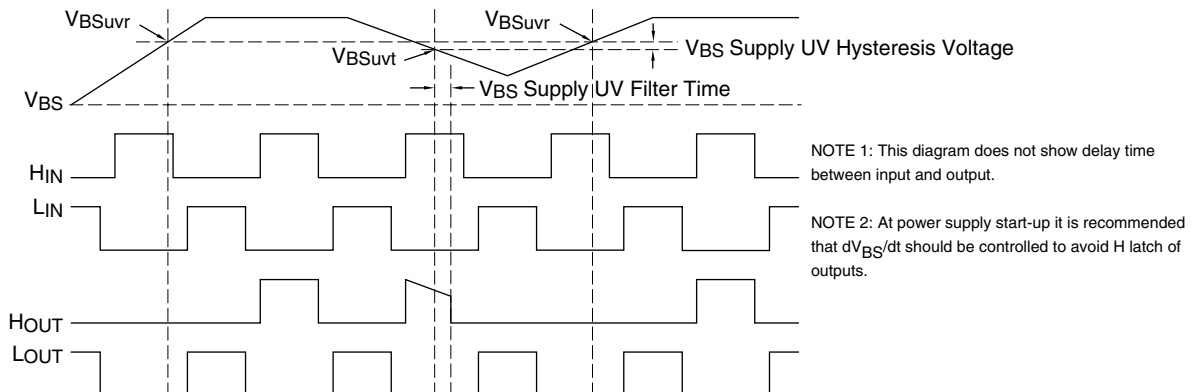
5. Low Side VCC Supply Power Reset Sequence

When VCC supply voltage is lower than power reset trip voltage, the power reset trips and output is locked out. As soon as VCC supply voltage does higher than power reset trip voltage, the output will respond to the next active input signal.



6. High-Side VBS Supply Under Voltage Lockout Sequence

When VBS supply voltage goes lower than VBS supply UV trip voltage for a period than the VBS supply UV filter time, HOUT goes low regardless of HIN. As soon as VBS supply voltage goes higher than VBS supply reset voltage, the output will respond to the next active HIN signal.

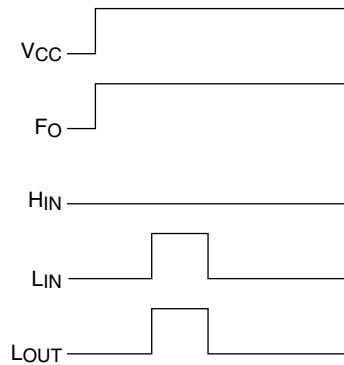


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7. Power Start-Up Sequence

At power supply start-up the following sequence is recommended when bootstrap supply topology is used.

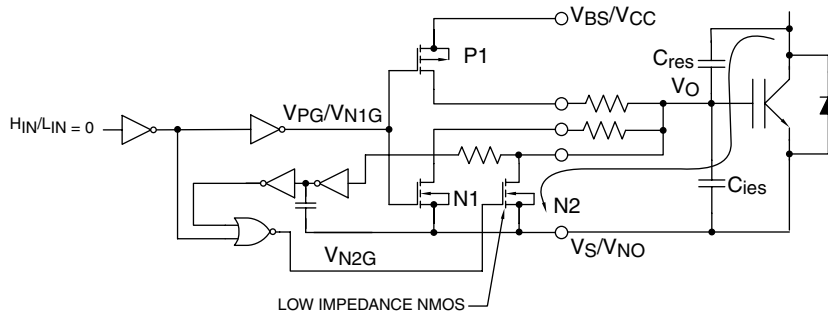
1. Set  $V_{CC}$ .
2. Make sure  $F_O$  is in high level.
3. Set  $L_{IN}$  to high level and set  $H_{IN}$  to low level so that bootstrap capacitor will charge.
4. Set  $L_{IN}$  to low level.



NOTE: If two power supplies are used to supply  $V_{CC}$  and  $V_{BS}$  individually, it is recommended to set  $V_{CC}$  first, then set  $V_{BS}$ .

8. Low Impedance NMOS Output Timing Diagram

Output configuration is shown in the following figure. At turn-off an n-channel NMOS with sink current up to 1A is used to offer a low impedance path (AKA "low impedance NMOS") to prevent the power switch from turning itself on because of the parasitic Miller capacitor in the power switch.



When  $H_{IN}/L_{IN}$  is low level and  $V_{OUT}$  voltage is lower than low impedance NMOS input threshold voltage, the low impedance NMOS continues to discharge the parasitic current through  $C_{res}$ .

