

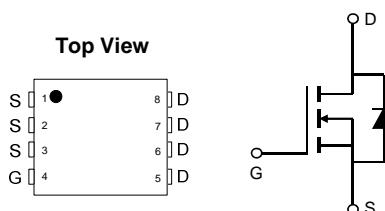
General Description

The AON7244 combines advanced trench MOSFET technology with a low resistance package to provide extremely low $R_{DS(ON)}$. This device is ideal for boost converters and synchronous rectifiers for consumer, telecom, industrial power supplies and LED backligh ting.

Product Summary

V_{DS}	60V
I_D (at $V_{GS}=10V$)	50A
$R_{DS(ON)}$ (at $V_{GS}=10V$)	< 8.5mΩ
$R_{DS(ON)}$ (at $V_{GS} = 4.5V$)	< 12mΩ

100% UIS Tested
100% R_g Tested



Absolute Maximum Ratings $T_A=25^\circ C$ unless otherwise noted

Parameter	Symbol	Maximum	Units
Drain-Source Voltage	V_{DS}	60	V
Gate-Source Voltage	V_{GS}	± 20	V
Continuous Drain Current ^G	I_D	50	A
		39	
Pulsed Drain Current ^C	I_{DM}	160	
Continuous Drain Current	I_{DSM}	20	A
		16	
Avalanche Current ^C	I_{AS}, I_{AR}	40	A
Avalanche energy L=0.1mH ^C	E_{AS}, E_{AR}	80	mJ
Power Dissipation ^B	P_D	83	W
		33	
Power Dissipation ^A	P_{DSM}	6.2	W
		4	
Junction and Storage Temperature Range	T_J, T_{STG}	-55 to 150	°C

Thermal Characteristics

Parameter	Symbol	Typ	Max	Units
Maximum Junction-to-Ambient ^A	$R_{\theta JA}$	16	20	°C/W
Maximum Junction-to-Ambient ^{A,D}		45	55	°C/W
Maximum Junction-to-Case	$R_{\theta JC}$	1.1	1.5	°C/W

Electrical Characteristics ($T_J=25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
STATIC PARAMETERS						
BV_{DSS}	Drain-Source Breakdown Voltage	$I_D=250\mu\text{A}, V_{GS}=0\text{V}$	60			V
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS}=60\text{V}, V_{GS}=0\text{V}$ $T_J=55^\circ\text{C}$			1 5	μA
I_{GSS}	Gate-Body leakage current	$V_{DS}=0\text{V}, V_{GS}=\pm 20\text{V}$			100	nA
$V_{\text{GS(th)}}$	Gate Threshold Voltage	$V_{DS}=V_{GS}, I_D=250\mu\text{A}$	1.5	2	2.5	V
$I_{\text{D(ON)}}$	On state drain current	$V_{GS}=10\text{V}, V_{DS}=5\text{V}$	160			A
$R_{\text{DS(ON)}}$	Static Drain-Source On-Resistance	$V_{GS}=10\text{V}, I_D=20\text{A}$ $T_J=125^\circ\text{C}$		7 12	8.5 15	$\text{m}\Omega$
		$V_{GS}=4.5\text{V}, I_D=16\text{A}$		9	12	$\text{m}\Omega$
g_{FS}	Forward Transconductance	$V_{DS}=5\text{V}, I_D=20\text{A}$		100		S
V_{SD}	Diode Forward Voltage	$I_S=1\text{A}, V_{GS}=0\text{V}$		0.7	1	V
I_S	Maximum Body-Diode Continuous Current ^G				50	A
DYNAMIC PARAMETERS						
C_{iss}	Input Capacitance	$V_{GS}=0\text{V}, V_{DS}=30\text{V}, f=1\text{MHz}$	1625	2030	2435	pF
C_{oss}	Output Capacitance		150	215	280	pF
C_{rss}	Reverse Transfer Capacitance		2.5	8.5	14.5	pF
R_g	Gate resistance	$V_{GS}=0\text{V}, V_{DS}=0\text{V}, f=1\text{MHz}$	0.4	0.8	1.2	Ω
SWITCHING PARAMETERS						
$Q_g(10\text{V})$	Total Gate Charge	$V_{GS}=10\text{V}, V_{DS}=30\text{V}, I_D=20\text{A}$	20	26	32	nC
$Q_g(4.5\text{V})$	Total Gate Charge		9	11.5	14	nC
Q_{gs}	Gate Source Charge			6.5		nC
Q_{gd}	Gate Drain Charge			2.5		nC
$t_{\text{D(on)}}$	Turn-On Delay Time	$V_{GS}=10\text{V}, V_{DS}=30\text{V}, R_L=1.5\Omega, R_{\text{GEN}}=3\Omega$		7.5		ns
t_r	Turn-On Rise Time			2.5		ns
$t_{\text{D(off)}}$	Turn-Off Delay Time			24.5		ns
t_f	Turn-Off Fall Time			1.5		ns
t_{rr}	Body Diode Reverse Recovery Time	$I_F=20\text{A}, dI/dt=500\text{A}/\mu\text{s}$	12	18	24	ns
Q_{rr}	Body Diode Reverse Recovery Charge	$I_F=20\text{A}, dI/dt=500\text{A}/\mu\text{s}$	45	68	90	nC

A. The value of R_{QJA} is measured with the device mounted on 1 in² FR-4 board with 2oz. Copper, in a still air environment with $T_A=25^\circ\text{C}$. The Power dissipation P_{DSM} is based on R_{QJA} , $t \leqslant 10\text{s}$ value and the maximum allowed junction temperature of 150°C . The value in any given application depends on the user's specific board design.

B. The power dissipation P_b is based on $T_{J(\text{MAX})}=150^\circ\text{C}$, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.

C. Repetitive rating, pulse width limited by junction temperature $T_{J(\text{MAX})}=150^\circ\text{C}$. Ratings are based on low frequency and duty cycles to keep initial $T_J=25^\circ\text{C}$.

D. The R_{QJA} is the sum of the thermal impedance from junction to case R_{QJC} and case to ambient.

E. The static characteristics in Figures 1 to 6 are obtained using <300μs pulses, duty cycle 0.5% max.

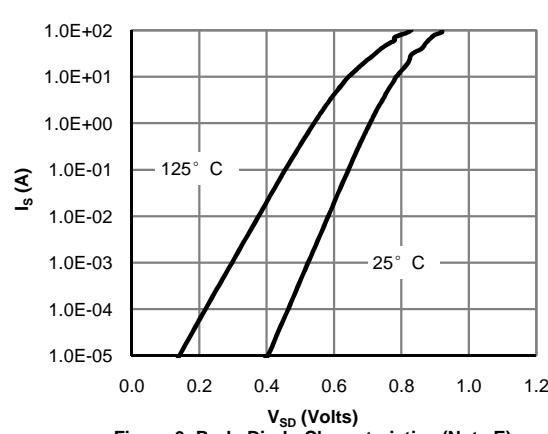
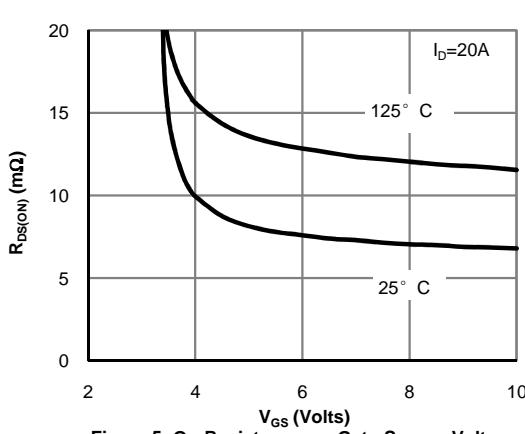
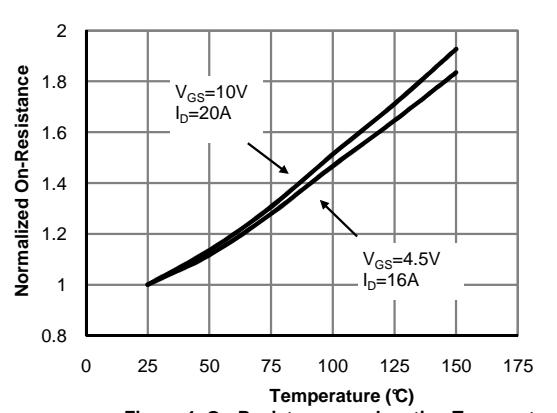
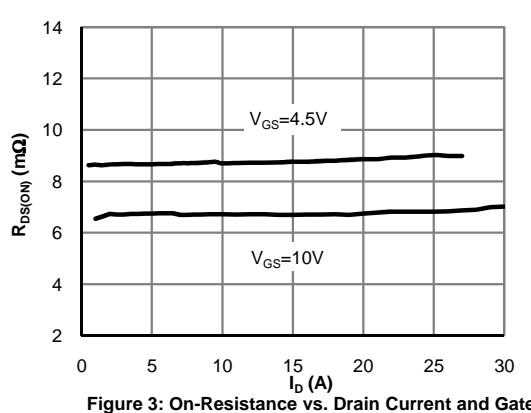
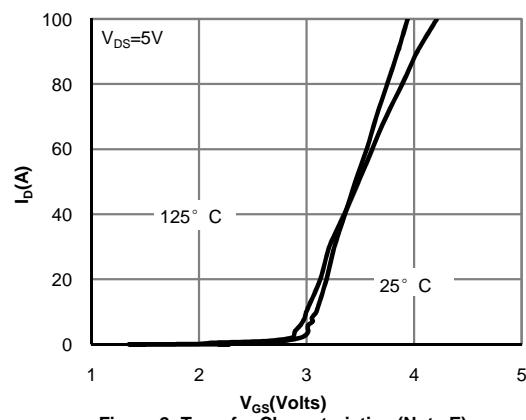
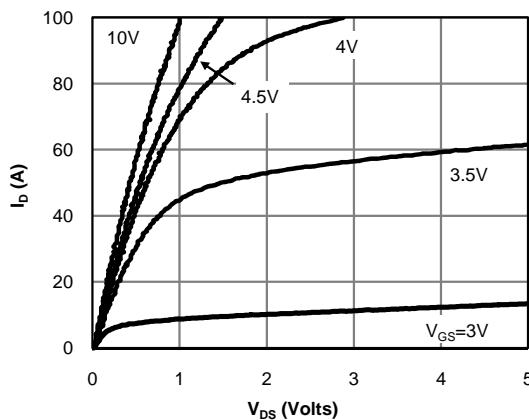
F. These curves are based on the junction-to-case thermal impedance which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of $T_{J(\text{MAX})}=150^\circ\text{C}$. The SOA curve provides a single pulse rating.

G. The maximum current rating is package limited.

H. These tests are performed with the device mounted on 1 in² FR-4 board with 2oz. Copper, in a still air environment with $T_A=25^\circ\text{C}$.

THIS PRODUCT HAS BEEN DESIGNED AND QUALIFIED FOR THE CONSUMER MARKET. APPLICATIONS OR USES AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS ARE NOT AUTHORIZED. AOS DOES NOT ASSUME ANY LIABILITY ARISING OUT OF SUCH APPLICATIONS OR USES OF ITS PRODUCTS. AOS RESERVES THE RIGHT TO IMPROVE PRODUCT DESIGN, FUNCTIONS AND RELIABILITY WITHOUT NOTICE.

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS



TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

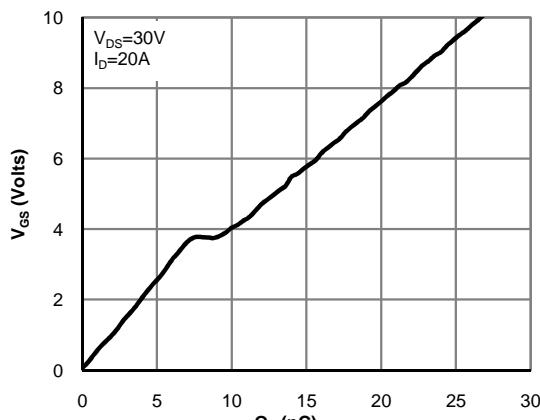


Figure 7: Gate-Charge Characteristics

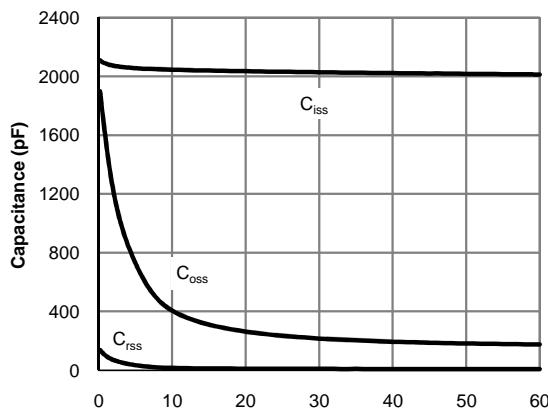


Figure 8: Capacitance Characteristics

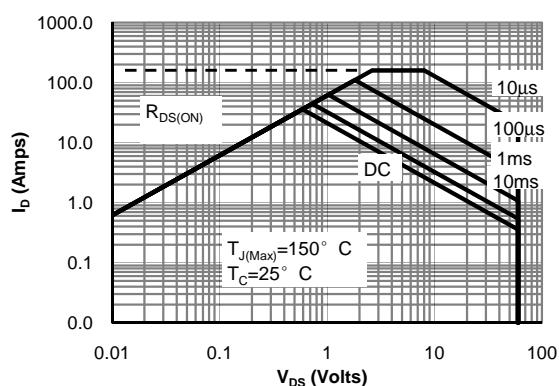


Figure 9: Maximum Forward Biased Safe Operating Area (Note F)

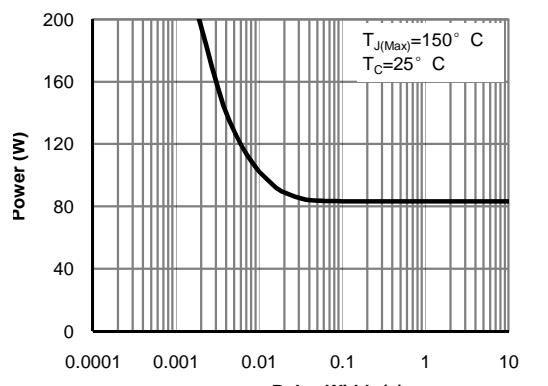


Figure 10: Single Pulse Power Rating Junction-to-Case (Note F)

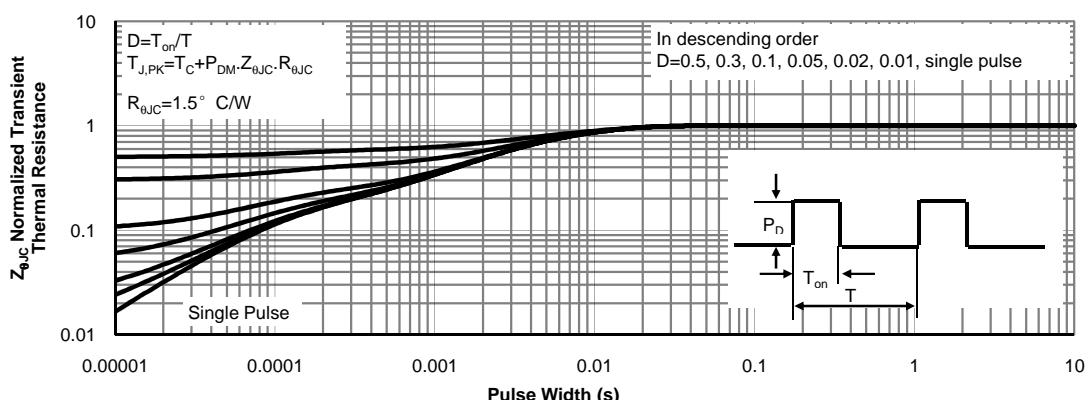


Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)

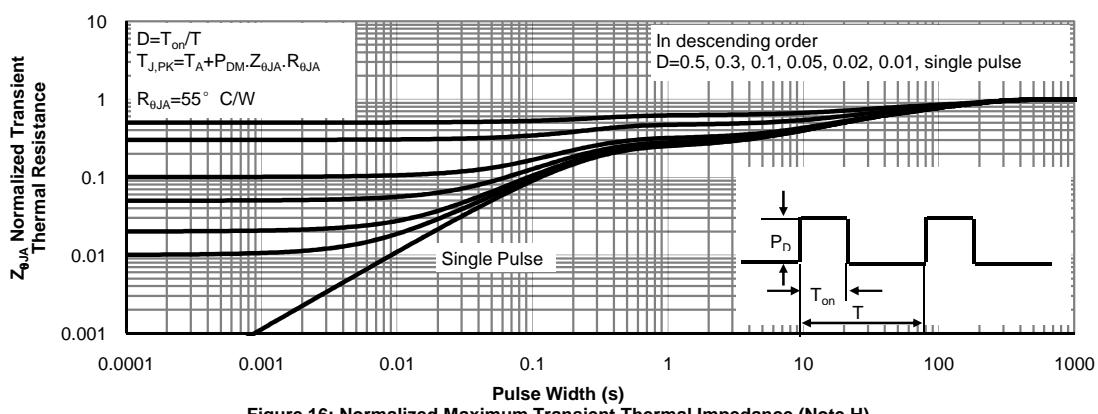
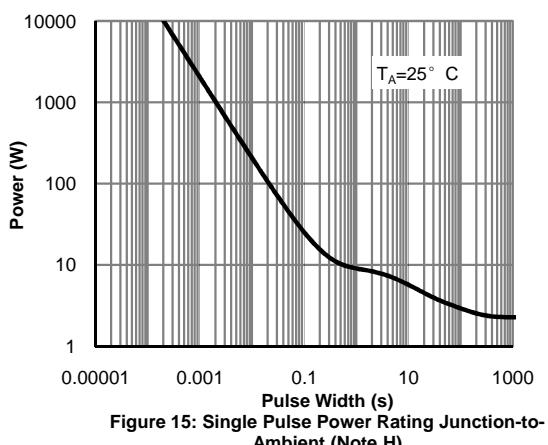
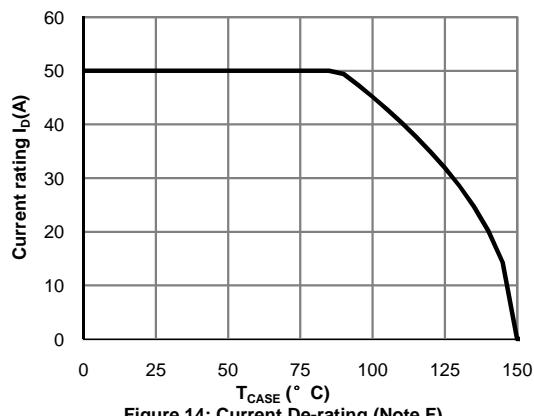
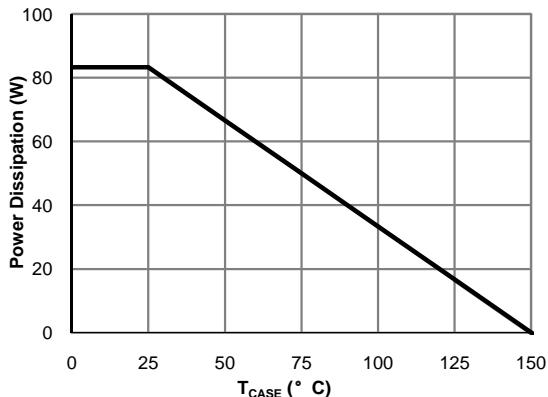
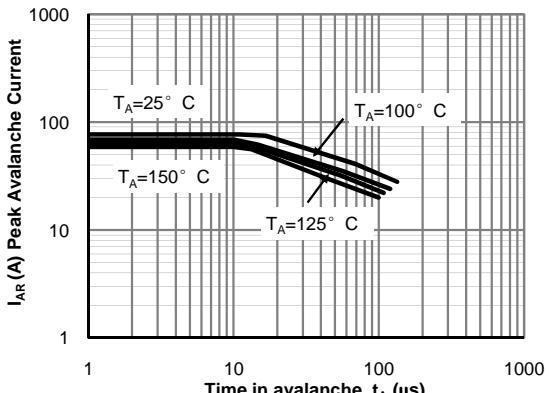


freescale

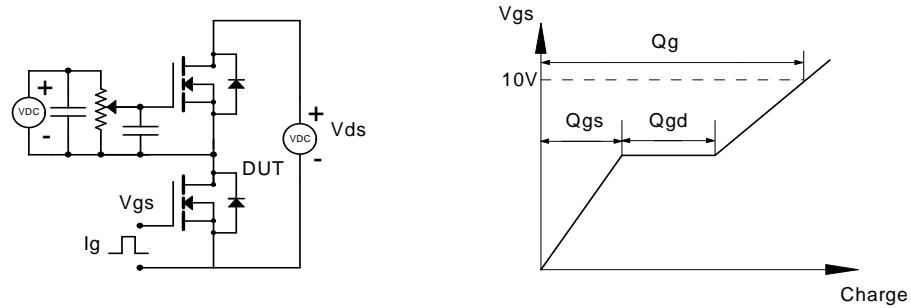
AON7244

飞思卡尔(深圳)功率半导体有限公司

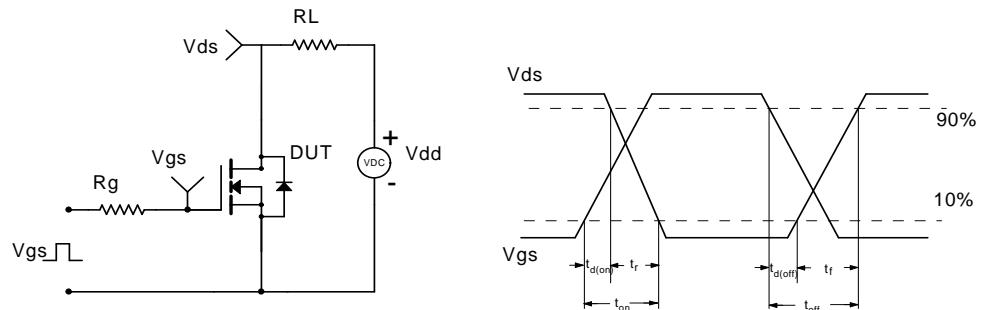
TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS



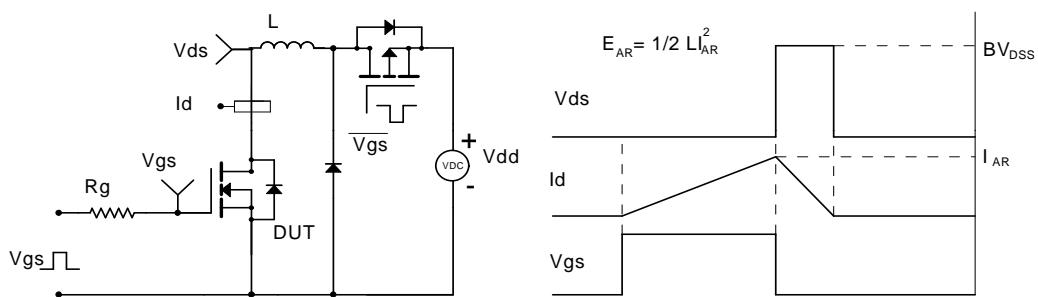
Gate Charge Test Circuit & Waveform



Resistive Switching Test Circuit & Waveforms



Unclamped Inductive Switching (UIS) Test Circuit & Waveforms



Diode Recovery Test Circuit & Waveforms

