AON7421

20V P-Channel MOSFET

General Description

The AON7421 combines advanced trench MOSFET technology with a low resistance package to provide extremely low $R_{DS(ON)}$. This device is ideal for load switch and battery protection applications.

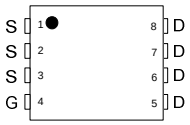
Product Summary

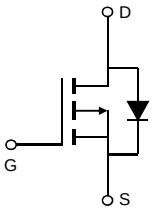
V_{DS}	-20V
I_D (at V_{GS}=-10V)	-50A
$R_{DS(ON)}$ (at V_{GS}=-10V)	< 4.6mΩ
$R_{DS(ON)}$ (at V_{GS} =-4.5V)	< 5.8mΩ
$R_{DS(ON)}$ (at V_{GS} =-2.5V)	< 9.0mΩ

100% UIS Tested
100% R_g Tested

Green Product

Top View





Absolute Maximum Ratings T_A=25℃ unless otherwise noted

Parameter		Symbol	Maximum	Units
Drain-Source Voltage		V_{DS}	-20	V
Gate-Source Voltage		V_{GS}	±12	V
Continuous Drain Current [G]	T_C=25℃	I_D	-50	A
	T_C=100℃		-39	
Pulsed Drain Current [C]		I_{DM}	-200	
Continuous Drain Current	T_A=25℃	I_{DSM}	-30	A
	T_A=70℃		-24.5	
Avalanche Current [C]		I_{AS}	50	A
Avalanche energy L=0.1mH [C]		E_{AS}	125	mJ
Power Dissipation [B]	T_C=25℃	P_D	83	W
	T_C=100℃		33	
Power Dissipation [A]	T_A=25℃	P_{DSM}	6.2	W
	T_A=70℃		4	
Junction and Storage Temperature Range		T_J, T_{STG}	-55 to 150	℃

Thermal Characteristics					
Parameter		**Symbol**	**Typ**	**Max**	**Units**
Maximum Junction-to-Ambient [A]	t ≤ 10s	$R_{\theta JA}$	16	20	℃/W
Maximum Junction-to-Ambient [A D]	Steady-State		45	55	℃/W
Maximum Junction-to-Case	Steady-State	$R_{\theta JC}$	1.1	1.5	℃/W

Electrical Characteristics (T_J=25℃ unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
STATIC PARAMETERS						
BV_{DSS}	Drain-Source Breakdown Voltage	I_D=-250µA, V_{GS}=0V	-20			V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}=-20V, V_{GS}=0V			-1	µA
		T_J=55℃			-5	
I_{GSS}	Gate-Body leakage current	V_{DS}=0V, V_{GS}=±12V			±100	nA
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS}, I_D=-250µA	-0.5	-0.8	-1.2	V
$I_{D(ON)}$	On state drain current	V_{GS}=-10V, V_{DS}=-5V	-200			A
$R_{DS(ON)}$	Static Drain-Source On-Resistance	V_{GS}=-10V, I_D=-20A		3.7	4.6	mΩ
		T_J=125℃		5	6.2	
		V_{GS}=-4.5V, I_D=-20A		4.5	5.8	mΩ
		V_{GS}=-2.5V, I_D=-20A		6.3	9	mΩ
g_{FS}	Forward Transconductance	V_{DS}=-5V, I_D=-20A		90		S
V_{SD}	Diode Forward Voltage	I_S=-1A,V_{GS}=0V		-0.58	-1	V
I_S	Maximum Body-Diode Continuous Current [G]				-50	A
DYNAMIC PARAMETERS						
C_{iss}	Input Capacitance	V_{GS}=0V, V_{DS}=-10V, f=1MHz		4550		pF
C_{oss}	Output Capacitance			823		pF
C_{rss}	Reverse Transfer Capacitance			563		pF
R_g	Gate resistance	V_{GS}=0V, V_{DS}=0V, f=1MHz		2.1	4.2	Ω
SWITCHING PARAMETERS						
Q_g(10V)	Total Gate Charge	V_{GS}=-10V, V_{DS}=-10V, I_D=-20A		95	114	nC
Q_g(4.5V)	Total Gate Charge			44	53	nC
Q_{gs}	Gate Source Charge			6.5		nC
Q_{gd}	Gate Drain Charge			14		nC
$t_{D(on)}$	Turn-On DelayTime	V_{GS}=-10V, V_{DS}=-10V, R_L=0.5Ω, R_{GEN}=3Ω		7		ns
t_r	Turn-On Rise Time			12		ns
$t_{D(off)}$	Turn-Off DelayTime			134		ns
t_f	Turn-Off Fall Time			45		ns
t_{rr}	Body Diode Reverse Recovery Time	I_F=-20A, dI/dt=500A/µs		30		ns
Q_{rr}	Body Diode Reverse Recovery Charge	I_F=-20A, dI/dt=500A/µs		75		nC

A. The value of $R_{\theta JA}$ is measured with the device mounted on 1in² FR-4 board with 2oz. Copper, in a still air environment with T_A =25° C. The Power dissipation P_{DSM} is based on $R_{\theta JA}$ t ≤ 10s value and the maximum allowed junction temperature of 150° C. The value in any given application depends on the user's specific board design.
B. The power dissipation P_D is based on $T_{J(MAX)}$=150° C, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.
C. Repetitive rating, pulse width limited by junction temperature $T_{J(MAX)}$=150° C. Ratings are based on low frequency and duty cycles to keep initial T_J =25° C.
D. The $R_{\theta JA}$ is the sum of the thermal impedance from junction to case $R_{\theta JC}$ and case to ambient.
E. The static characteristics in Figures 1 to 6 are obtained using <300µs pulses, duty cycle 0.5% max.
F. These curves are based on the junction-to-case thermal impedance which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of $T_{J(MAX)}$=150° C. The SOA curve provides a single pulse rating.
G. The maximum current rating is package limited.
H. These tests are performed with the device mounted on 1 in² FR-4 board with 2oz. Copper, in a still air environment with T_A=25° C.

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

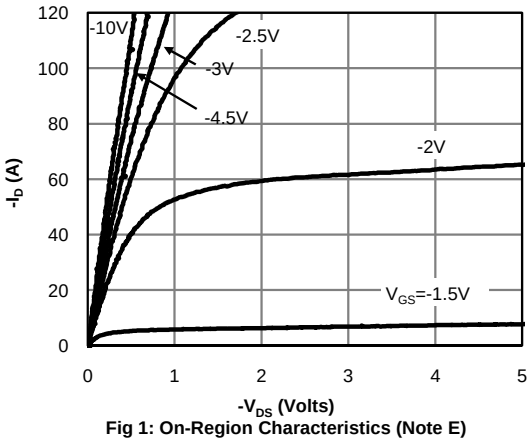


Fig 1: On-Region Characteristics (Note E)

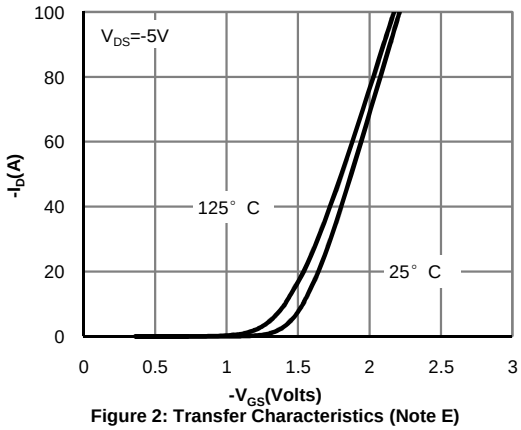


Figure 2: Transfer Characteristics (Note E)

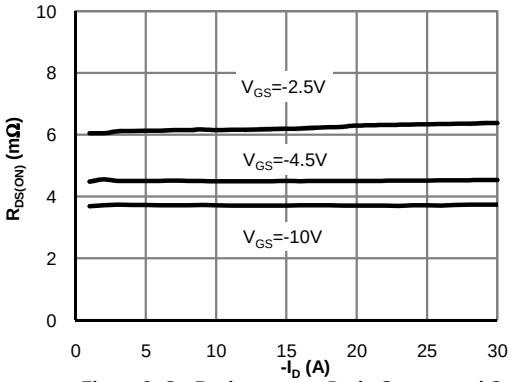


Figure 3: On-Resistance vs. Drain Current and Gate Voltage (Note E)

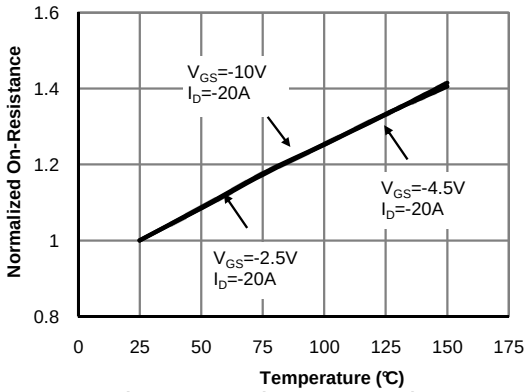


Figure 4: On-Resistance vs. Junction Temperature (Note E)

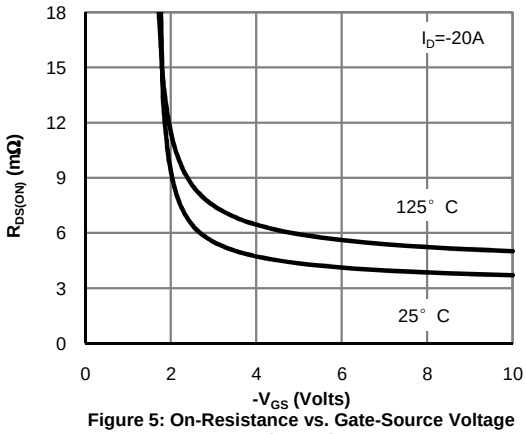


Figure 5: On-Resistance vs. Gate-Source Voltage (Note E)

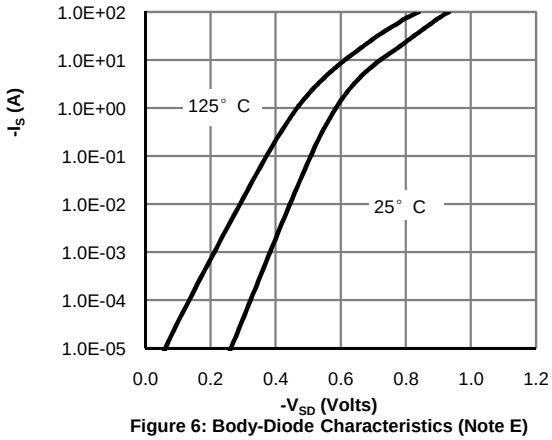


Figure 6: Body-Diode Characteristics (Note E)

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

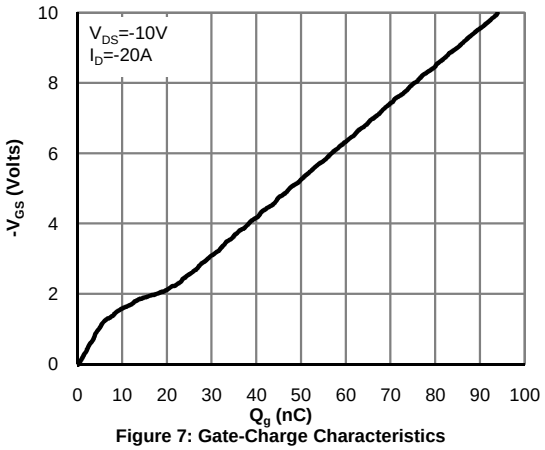


Figure 7: Gate-Charge Characteristics

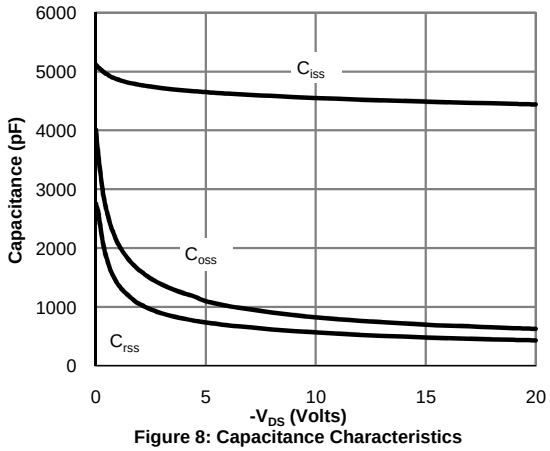


Figure 8: Capacitance Characteristics

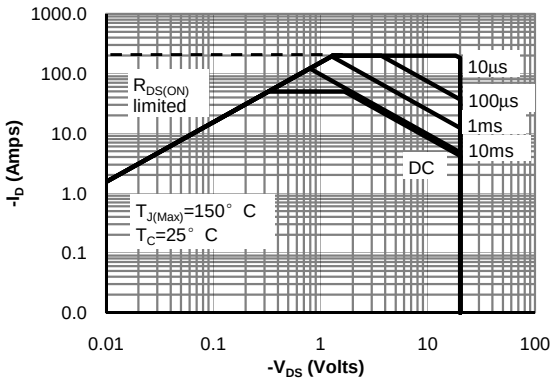


Figure 9: Maximum Forward Biased Safe Operating Area (Note F)

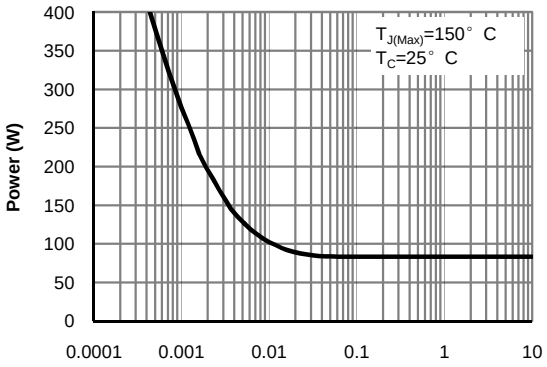


Figure 10: Single Pulse Power Rating Junction-to-Ca (Note F)

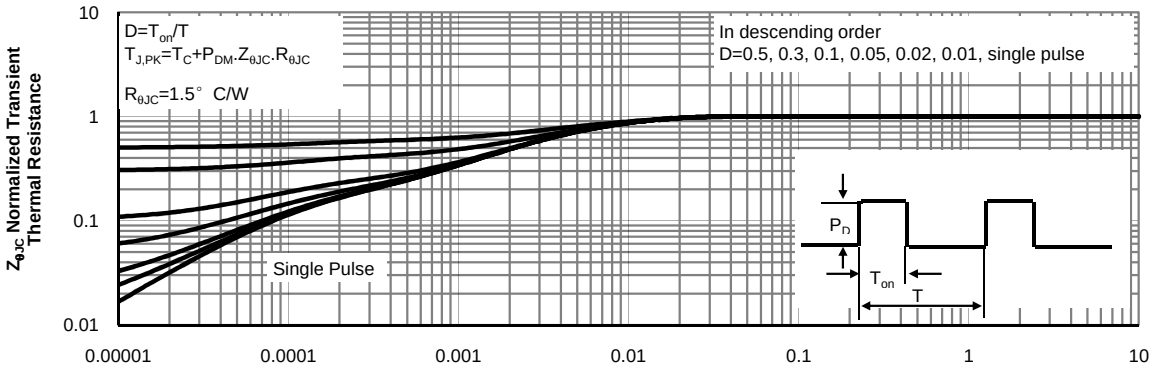


Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

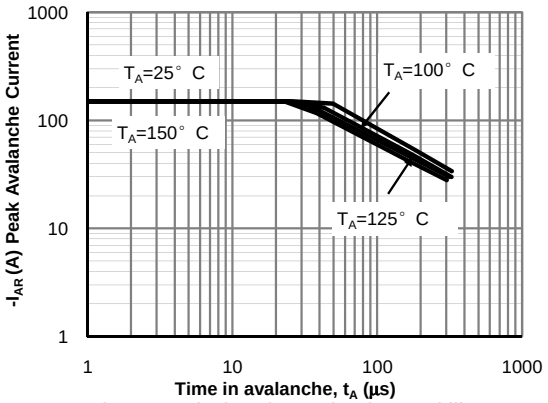


Figure 12: Single Pulse Avalanche capability (Note C)

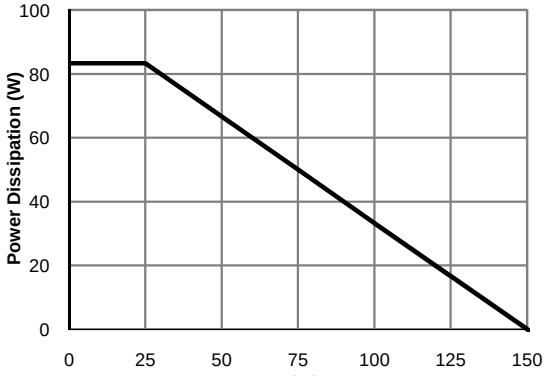


Figure 13: Power De-rating (Note F)

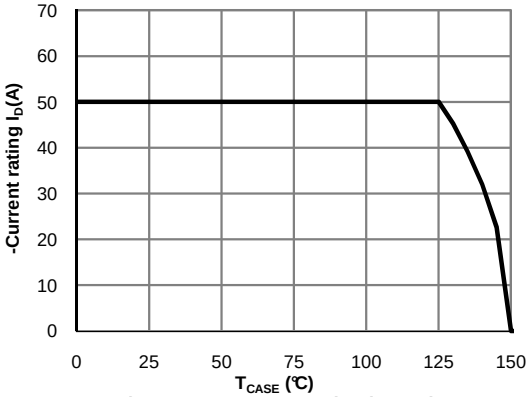


Figure 14: Current De-rating (Note F)

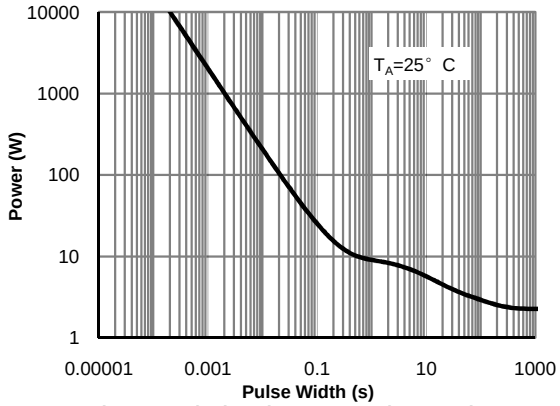


Figure 15: Single Pulse Power Rating Junction-to-Ambient (Note H)

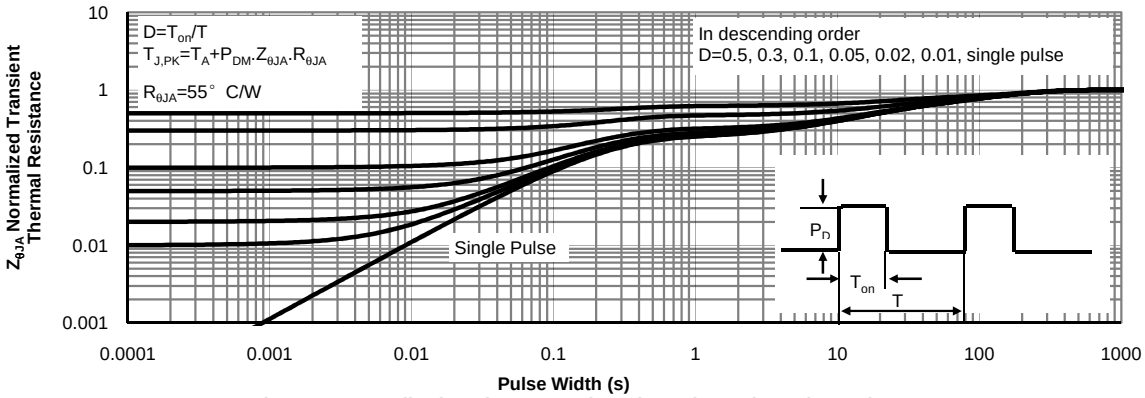
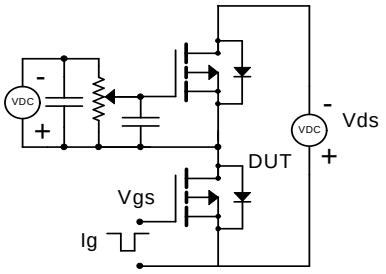
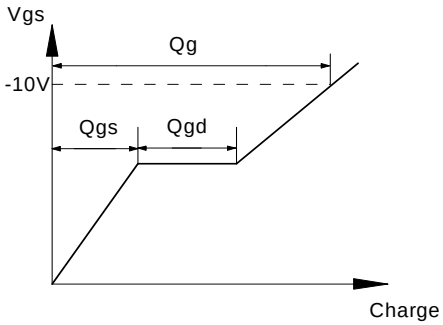


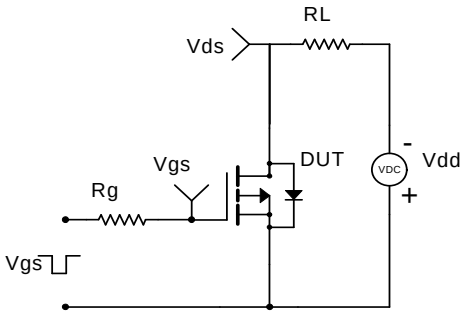
Figure 16: Normalized Maximum Transient Thermal Impedance (Note H)

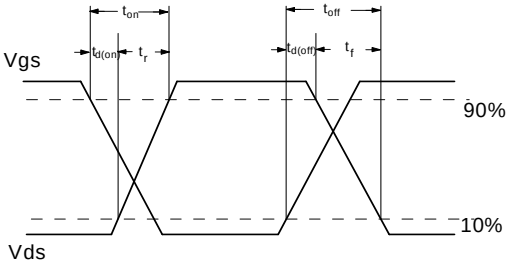
Gate Charge Test Circuit & Waveform



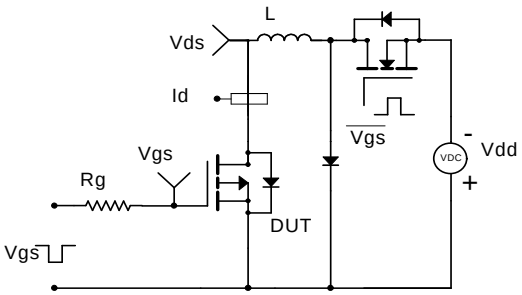


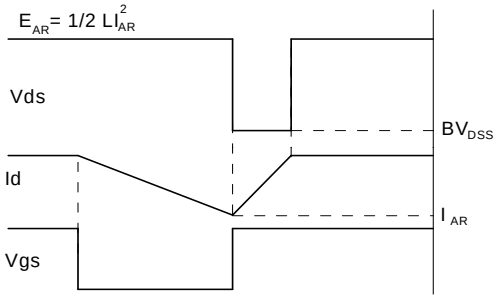
Resistive Switching Test Circuit & Waveforms





Unclamped Inductive Switching (UIS) Test Circuit & Waveforms





Diode Recovery Test Circuit & Waveforms