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50 MHz Current-Feedback Amplifier

Preliminary Data Sheet
CA2020

FEATURES

- **Drives** . . . . ±2.4V into 75Ω
- **Slew Rate** . . . . 500V/Sec.
- **Supplies** . . . . ±5V to ±18V
- **Short Circuit Protection**
- **Compatible with EL2020**

APPLICATIONS

- **Coax Cable Driver with Gain**
- **Video Gain Block**
- **Multiplex Systems**
- **Current to Voltage Converter**
- **Radar Systems**

DESCRIPTION

The CA2020 is a fast settling amplifier specifically designed to drive low impedance loads, such as coax cables. The current mode feedback feature makes this amplifier's bandwidth and slew rate less dependent on the set gain than a conventional operational amplifier. The 50 MHz bandwidth at unity gain drops to 30 MHz at a gain of 10.

The device is capable of driving ±2.4 Volts into a 75Ω coax cable. If more current is required a buffer can be included in the feedback loop of the CA2020.

The CA2020 is designed for military temperature ranges, −55°C to 125°C, and is available in an 8-pin HERMETIC-DIP. The CA2020C is for operation in the industrial temperature range, −25°C to 85°C, and is available in an 8-pin HERMETIC-DIP and in an 8-pin PLASTIC MINI-DIP.

ORDERING INFORMATION

PACKAGE		
HERMETIC CERDIP 8-PIN	PLASTIC DIP 8-PIN	OPERATING TEMPERATURE RANGE
CA2020Z		MIL
CA2020CZ	CA2020CP	IND

Pin Connections (Top View)

BAL 1   8 DISABLE
IN- 2   7 V+
IN+ 3   6 OUT
V- 4   5 BAL
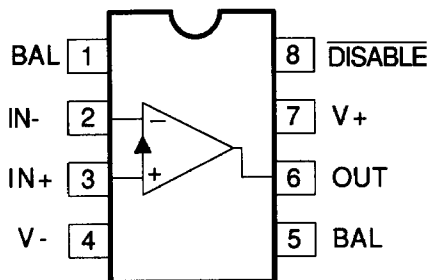
EPOXY MINI-DIP (P-Suffix)
8-PIN HERMETIC DIP (Z-Suffix)

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ABSOLUTE MAXIMUM RATINGS

Supply Voltage (V_S) . . . . ±18V
Input Voltage . . . . ±15V or V_S
Differential Input Voltage . . . . ±10V
Input Current (Pins 2 or 3) . . . . ±10mA
Input Current (Pins 1, 5 or 8) . . . . ±5mA
Output Short Circuit Duration with Heatsink is continuous
Peak Output Current . . . . Short Circuit Protected

Storage Temperature Range
  Z Package . . . . −65°C to +150°C
  P Package . . . . −65°C to +125°C
Operating Temperature Range
  CA2020 . . . . −55°C to +125°C
  CA2020C . . . . −25°C to +85°C
Lead Temperature (Soldering, 60 sec.) . . . . 300°C
DICE Junction Temperature (T_j)
  Z Package . . . . 175°C
  P Package . . . . 150°C

Die Layout
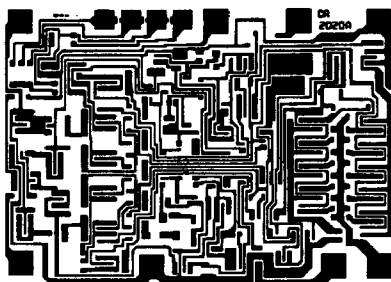
DIE SIZE:
0.077×0.056 inch, 4312 sq. mils
(1.956×1.422mm, 2.781 sq. mm)

OPEN LOOP ELECTRICAL CHARACTERISTICS $V_S = \pm15V$, $T_A = 25°C$

PARAMETER & TEST CONDITIONS	SYMBOL	MIN.	TYP.	MAX.	UNITS
Input Offset Voltage	V_{OS}	−10	3	+10	mV
Common Mode Rejection Ratio ($V_{CM} = \pm10V$)	CMRR	50	60	—	dB
Power Supply Rejection Ratio ($\pm4.5V \leq V_S \leq \pm18V$)	PSRR	65	75	—	dB
Non-Inverting Input Current	+I_{in}	−15	5	+15	μA
Non-Inverting Input Resistance	+R_{in}	1	5	—	MΩ
Non-Inverting Input Current Power Supply Rejection ($\pm4.5V \leq V_S \leq \pm18V$)	+IPSR	—	0.05	0.5	μA/V
Inverting Input Current	−I_{in}	−40	10	+40	μA
Inverting Input Current Common Mode Rejection ($V_{CM} = \pm10V$)	−ICMR	—	0.5	2.0	μA/V
Inverting Input Current Power Supply Rejection ($\pm4.5V \leq V_S \leq \pm18V$)	−IPSR	—	0.05	0.5	μA/V
Transimpedance ($\Delta V_{out}/\Delta(-I_{in})$), RL = 400Ω, $V_{out} = \pm10V$	R_{ol}	300	1000	—	V/mA
Open Loop DC Voltage Gain, RL = 400Ω, $V_{out} = \pm10V$	A_{vol1}	70	80	—	dB
Open Loop DC Voltage Gain, RL = 1000Ω, $V_{out} = \pm2.5V$	A_{vol2}	60	70	—	dB
Output Voltage Swing, RL = 400Ω	V_o	±12	±13	—	V
Output Current, RL = 400Ω	I_{out}	±30	±32.5	—	mA
Quiescent Supply Current	I_s	—	9	12	mA
Supply Current, Disabled, Pin 8 = 0V	I_{soff}	—	5.5	7.5	mA
Pin 8 Current, Pin 8 = 0V	I_{logic}	—	1.1	1.5	mA
Min Pin 8 Current to Disable	I_d	—	120	250	μA
Max Pin 8 Current to Enable	I_e	—	—	10	μA

NOTES:
1. The input offset voltage and the inverting input current can be adjusted with an external 10 kΩ pot between pin 1 and 5 with the wiper connected to pin 7 (V_{CC}) to make the output offset voltage zero.

2. A heatsink is required to keep the junction temperature below its maximum rating when the output is short circuited.

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OPEN LOOP ELECTRICAL CHARACTERISTICS $V_S = \pm 15V$, $T_A = -55°C$ to $+125°C$ for CA2020, $T_A = -25°C$ to $85°C$ for CA2020C

PARAMETER & TEST CONDITIONS	TEMP RANGE	SYMBOL	MIN.	TYP.	MAX.	UNITS
Input Offset Voltage	T_{max} & T_{min}	V_{OS}	-15	—	$+15$	mV
Common Mode Rejection Ratio ($V_{CM} = \pm 10V$)	T_{max} & T_{min}	CMRR	50	60	—	dB
Power Supply Rejection Ratio ($\pm 4.5V \le V_S \le \pm 18V$)	T_{max} & T_{min}	PSRR	60	—	—	dB
Non-Inverting Input Current	T_{max}	$+I_{in}$	-15	5	$+15$	μA
	T_{min}		-25	—	$+25$	μA
Non-Inverting Input Resistance	T_{max} & T_{min}	$+R_{in}$	1	5	—	MΩ
Non-Inverting Input Current Power Supply Rejection ($\pm 4.5V \le V_S \le \pm 18V$)	T_{max}	$+IPSR$	—	0.05	0.5	μA/V
	T_{min}		—	—	1.0	μA/V
Inverting Input Current	T_{max}	$-I_{in}$	-40	10	$+40$	μA
	T_{min}		-50	—	$+50$	μA
Inverting Input Current Common Mode Rejection ($V_{CM} = \pm 10V$)	T_{max}	$-ICMR$	—	0.5	2.0	μA/V
	T_{min}		—	—	4.0	μA
Inverting Input Current Power Supply Rejection ($\pm 4.5V \le V_S \le \pm 18V$)	T_{max}	$-IPSR$	—	0.05	0.5	μA/V
	T_{min}		—	—	1.0	μA/V
Transimpedance ($\Delta V_{out}/\Delta(-I_{in})$), RL = 400$\Omega$, $V_{out} = \pm 10V$	T_{max}	R_{ol}	300	1000	—	V/mA
	T_{min}		100	—	—	V/mA
Open Loop DC Voltage Gain, RL = 400Ω, $V_{out} = \pm 10V$	T_{max}	A_{vol1}	70	80	—	dB
	T_{min}		65	—	—	dB
Open Loop DC Voltage Gain, RL = 1000Ω, $V_{out} = \pm 2.5V$	T_{max}	A_{vol2}	60	70	—	dB
	T_{min}		55	—	—	dB
Output Voltage Swing, RL = 400Ω	T_{max}	V_O	± 12	± 13	—	V
	T_{min}		± 11	—	—	V
Output Current, RL = 400Ω	T_{max}	I_{out}	± 30	± 32.5	—	mA
	T_{min}		± 27.5	—	—	mA
Quiescent Supply Current	T_{max} & T_{min}	I_s	—	—	15	mA
Supply Current, Disabled, Pin 8 = 0V	T_{max} & T_{min}	I_{soff}	—	5.5	7.5	mA
Pin 8 Current, Pin 8 = 0V	T_{max} & T_{min}	I_{logic}	—	1.1	1.5	mA
Min Pin 8 Current to Disable	T_{max} & T_{min}	I_d	—	120	250	μA
Max Pin 8 Current to Enable	T_{max} & T_{min}	I_e	—	—	10	μA

AC CLOSED LOOP CHARACTERISTICS EL2020/EL2020C $V_S = \pm 15V$, $T_A = 25°C$

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Closed loop gain of 1V/V (0 dB), $R_f = 1k\Omega$						
Slew Rate	SR1	$R_l = 400\Omega$, $V_O = \pm 10V$, test at $V_O = \pm 5V$	300	500	—	V/μs
Rise Time	tr1	$R_l = 100\Omega$, $V_{out} = 1V$, 10% to 90%	—	6	—	ns
Fall Time	tf1	$R_l = 100\Omega$, $V_{out} = 1V$, 10% to 90%	—	6	—	ns
Propagation Delay	tp1	$R_l = 100\Omega$, $V_{out} = 1V$, 50% points	—	8	—	ns
Closed loop gain of 1V/V (0 dB), Rf = 820Ω						
–3dB Small signal Bandwidth	BW1	$R_l = 100\Omega$, $V_O = 100mV$	—	50	—	MHz
1% settling time	ts1	$R_l = 400\Omega$, $V_O = 10V$	—	50	—	ns
0.1% settling time	ts2	$R_l = 400\Omega$, $V_O = 10V$	—	90	—	ns
Closed loop gain of 10V/V (20 dB), $R_f = 1k\Omega$, $R_g = 111\Omega$						
Slew Rate	SR10	$R_l = 400\Omega$, $V_O = \pm 10V$, test at $V_O = \pm 5V$	300	500	—	V/μs
Rise Time	tr10	$R_l = 100\Omega$, $V_{out} = 1V$, 10% to 90%	—	25	—	ns
Fall Time	tf10	$R_l = 100\Omega$, $V_{out} = 1V$, 10% to 90%	—	25	—	ns
Propagation Delay	tp10	$R_l = 100\Omega$, $V_{out} = 1V$, 50 % points	—	12	—	ns
Closed loop gain of 10V/V (20 dB), $R_f = 680\Omega$, $R_g = 76\Omega$						
–3dB Small signal Bandwidth	BW10	$R_l = 100\Omega$, $V_O = 100mV$	—	30	—	MHz
1% settling time	ts11	$R_l = 400\Omega$, $V_O = 10V$	—	55	—	ns
0.1% settling time	ts12	$R_l = 400\Omega$, $V_O = 10V$	—	280	—	ns

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Burn-In Circuits
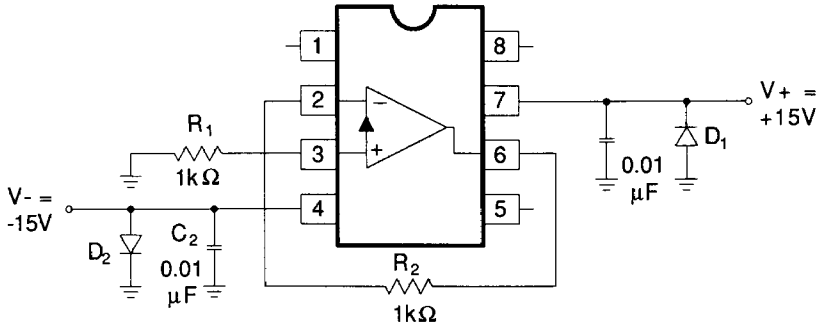
PIN NUMBERS ARE FOR DIP PACKAGES.
ALL PACKAGES USE THE SAME SCHEMATIC.

Simplified Schematic