



PRELIMINARY

CY7C3387P
CY7C3388P

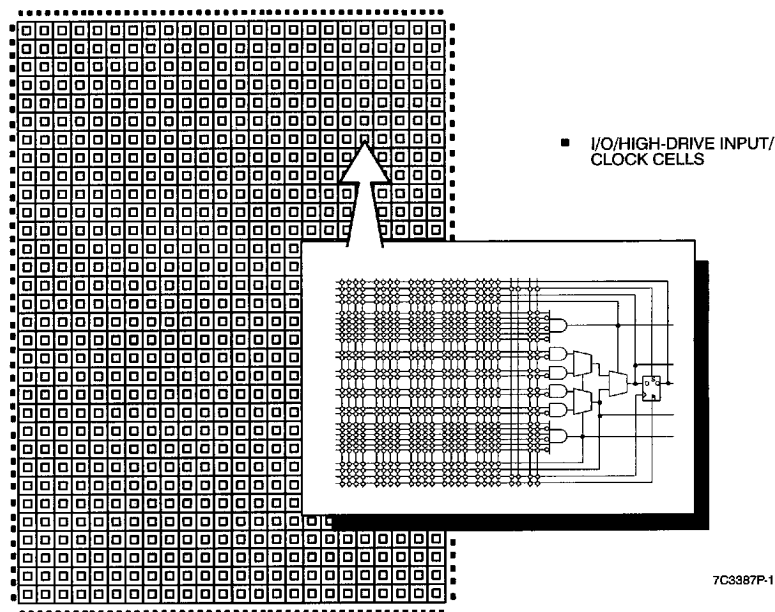
UltraLogic™ Very High Speed 8K Gate CMOS FPGA

Features

- Very high speed
 - Loadable counter frequencies greater than 80 MHz
 - Chip-to-chip operating frequencies up to 60 MHz
- Unparalleled FPGA performance for counters, data path, state machines, arithmetic, and random logic
- High usable density
 - 24 x 32 array of 768 logic cells provides 24,000 total available gates
 - 8,000 typically usable "gate array" gates in 144-pin TQFP and 208-pin PQFP
- Fully 3.3V PCI compliant inputs and outputs for commercial and industrial temperature range
- Minimum I_{OL} of 16 mA and I_{OH} of 8 mA
- Low power, high output drive
 - Standby current typically 250 μ A

- 16-bit counter operating at 80 MHz consumes 25 mA
- Flexible logic cell architecture
 - Wide fan-in (up to 14 input gates)
 - Multiple outputs in each cell
- Powerful design tools—*Warp3*™
 - Designs entered in VHDL, schematics, or mixed mode
 - Fast, fully automatic place and route
 - Waveform simulation with back annotated net delays
 - PC and workstation platforms
- Extensive third-party tool support
 - See Development Systems section
- Robust routing resources
 - Fully automatic place and route of designs using up to 100 percent of logic resources
 - No hand routing required
- 5V tolerant Inputs (see I_{IH} spec)
- 116 (7C3387P) to 172 (7C3388P) bidirectional input/output pins
- 6 dedicated input/high-drive pins
- 2 clock/dedicated input pins with fan-out-independent, low-skew nets
 - Clock skew <0.5 ns
- Input hysteresis provides high noise immunity
- Thorough testability at 3.3V
 - Built-in scan path permits 100 percent factory testing of logic and I/O cells
- 0.65 μ CMOS process with ViaLink™ programming technology
 - High-speed metal-to-metal link
 - Non-volatile antifuse technology
- 144-pin TQFP pinout compatible with the 4K (CY7C3386A) devices
- Pinout compatible with the 5V (CY7C387P/8P) devices

Logic Block Diagram



7C3387P-1

144 and 208 PIN PACKAGES, 172 I/O CELLS, 6 INPUT HIGH DRIVE CELLS, 2 INPUT/CLK (HIGH DRIVE) CELLS

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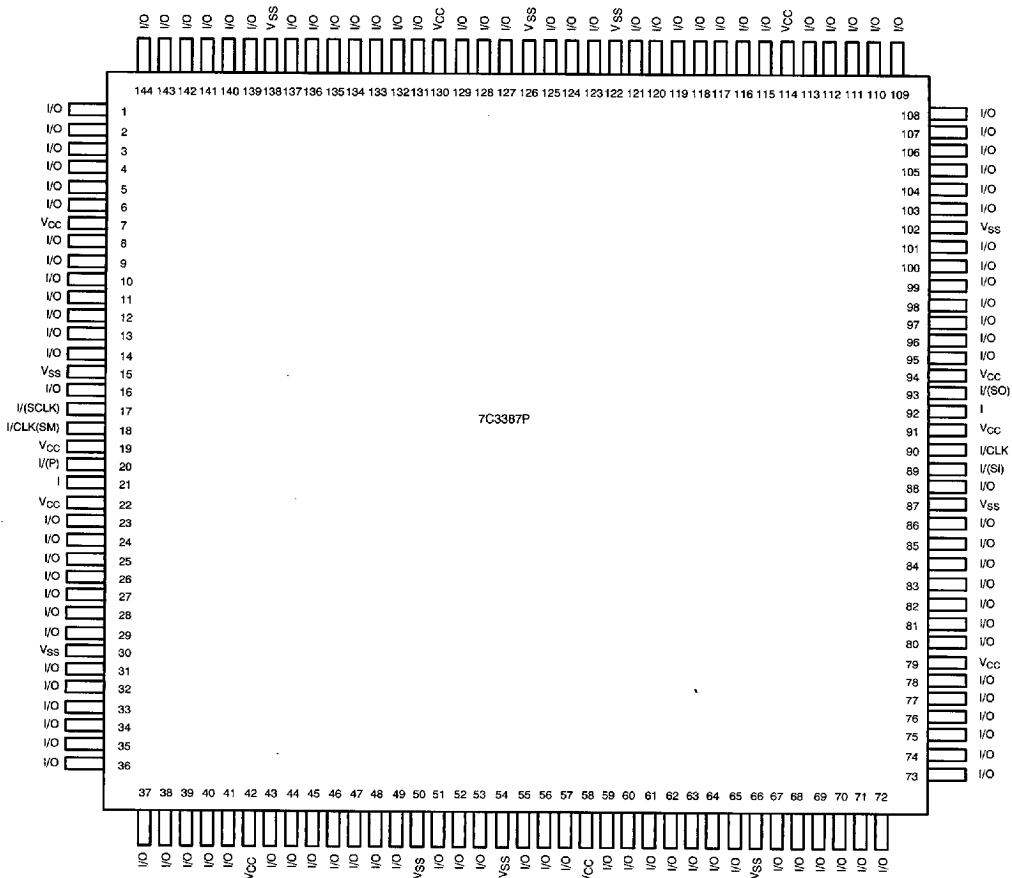
Functional Description

The CY7C3387P and CY7C3388P are very high speed, CMOS, user-programmable ASIC (pASIC™) devices. The 768 logic cell field-programmable gate array (FPGA) offers 8,000 typically usable "gate array" gates. This is equivalent to 24,000 EPLD or LCA gates. The CY7C3387P is available in a 144-pin TQFP. The CY7C3388P is available in 208-pin PQFP.

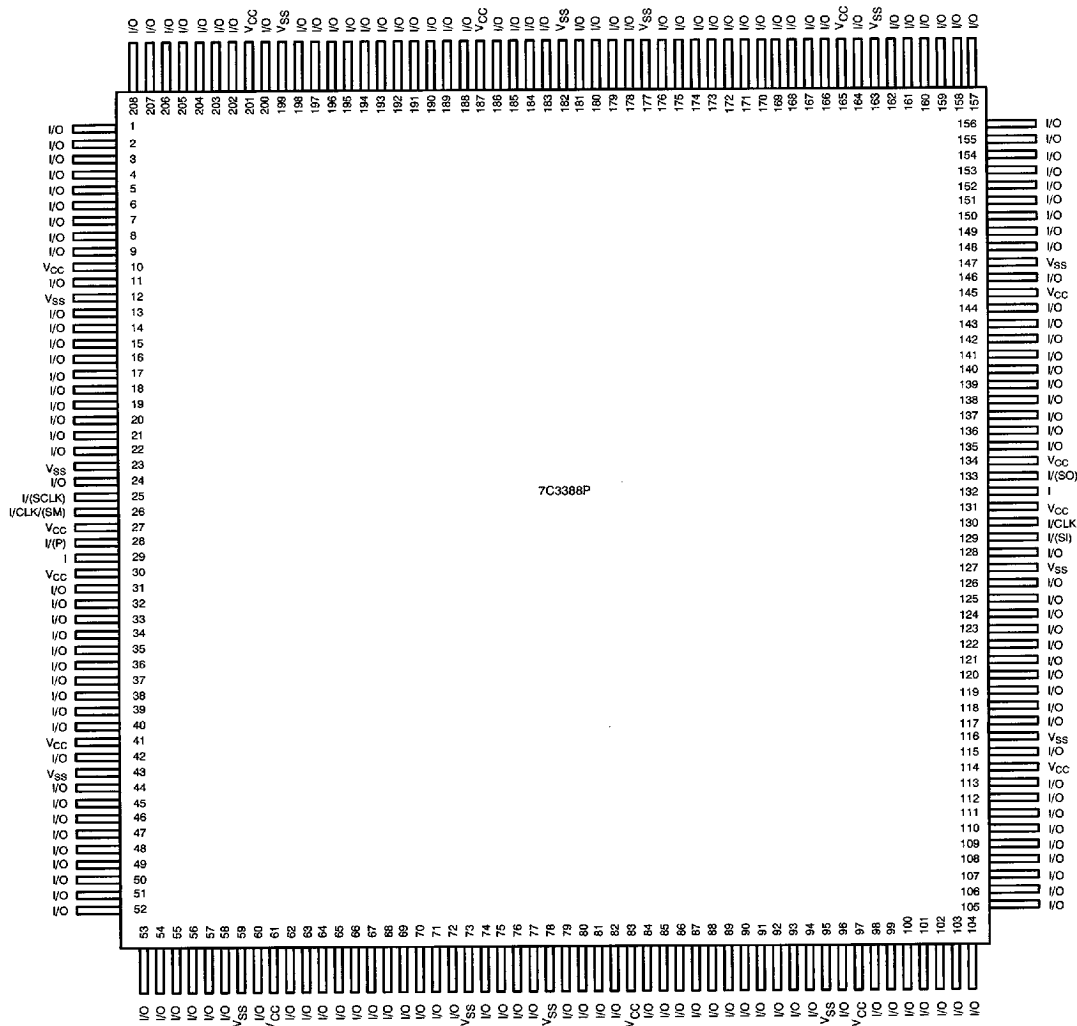
Low-impedance, metal-to-metal ViaLink interconnect technology provides non-volatile custom logic capable of operating at speeds above 80 MHz. This permits high-density programmable devices to be used with today's fastest CISC and RISC microprocessors.

Pin Configurations

**144-Pin Thin Quad Flat Pack (TQFP)
Top View**



7C3387P-2

Pin Configurations (continued)
**208-Pin Plastic Quad Flat Pack (PQFP)
Top View**


7C3387P-3

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature	
Ceramic	−65°C to +150°C
Plastic	−40°C to +125°C
Lead Temperature	300°C
Supply Voltage	−0.5V to +7.0V
Input Voltage	−0.5V to $V_{CC} + 0.5V$
ESD Pad Protection	±2000 V
DC Input Voltage	−0.5V to 7.0V

DC Input Current	±20 mA
Latch-Up Current	±200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	3.3V ± 0.3V
Industrial	−40°C to +85°C	3.3V ± 0.3V

Delay Factor (K)

Speed Grade	Commercial		Industrial	
	Min.	Max.	Min.	Max.
−X	0.46	3.52	0.4	3.77
−0	0.46	2.61	0.4	2.81
−1	0.46	2.23	0.4	2.39

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions	Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	$I_{OH} = -8 \text{ mA}$	2.4		V
		$I_{OH} = -10.0 \mu\text{A}$	$V_{CC} - 0.1$		V
V_{OL}	Output LOW Voltage	$I_{OL} = 16 \text{ mA}$		0.4	V
		$I_{OL} = 10.0 \mu\text{A}$		0.1	V
V_{IH}	Input HIGH Voltage		2.0		V
V_{IL}	Input LOW Voltage			0.8	V
I_{IH}	Input HIGH Current Sink (for 5V Inputs)	$5V > V_{IN} > V_{CC}$		12 ^[1]	mA
I_I	Input Leakage Current	$V_{IN} = V_{CC} \text{ or } V_{SS}$	−10	+10	μA
I_{OZ}	Three-State Output Leakage Current	$V_{IN} = V_{CC} \text{ or } V_{SS}$	−10	+10	μA
I_{OS}	Output Short Circuit Current ^[2]	$V_{OUT} = V_{SS}$	−5	−50	mA
		$V_{OUT} = V_{CC}$	15	100	mA
I_{CC1}	Standby Supply Current	$V_{IN}, V_{IO} = V_{CC} \text{ or } V_{SS}$		650	μA

Capacitance

Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	$T_A = 25^\circ\text{C}, f = 1 \text{ MHz}, V_{CC} = 3.3V$	10	pF
C_{OUT}	Output Capacitance		10	pF

Notes:

- User must limit current to 12 mA.
- Only one output at a time. Duration should not exceed 30 seconds.

Switching Characteristics (V_{CC}=3.3V, T_A=25°C, K=1)

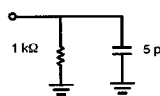
Parameter	Description	Propagation Delays ^[3] with Fanout of					Unit
		1	2	3	4	8	
LOGIC CELLS							
t _{PD}	Combinatorial Delay ^[4]	1.7	2.2	2.7	3.3	5.5	ns
t _{SU}	Set-Up Time ^[4]	2.1	2.1	2.1	2.1	2.1	ns
t _H	Hold Time	0.0	0.0	0.0	0.0	0.0	ns
t _{CLK}	Clock to Q Delay	1.0	1.5	1.9	2.7	4.9	ns
t _{CWHI}	Clock HIGH Time	2.0	2.0	2.0	2.0	2.0	ns
t _{CWLO}	Clock LOW Time	2.0	2.0	2.0	2.0	2.0	ns
t _{SET}	Set Delay	1.7	2.2	2.7	3.3	5.5	ns
t _{RESET}	Reset Delay	1.5	1.9	2.3	2.8	4.6	ns
t _{SW}	Set Width	1.9	1.9	1.9	1.9	1.9	ns
t _{RW}	Reset Width	1.8	1.8	1.8	1.8	1.8	ns

Parameter	Description	Propagation Delays ^[3] with Fanout of								Unit
		1	2	3	4	8	12	16		
INPUT CELLS										
t _{IN}	Input Delay (HIGH Drive)	3.1	3.2	3.3	3.4	4.4	3.8	6.5	ns	
t _{INI}	Input, Inverting Delay (HIGH Drive)	3.3	3.4	3.5	3.6	4.6	6.0	6.7	ns	
t _{IO}	Input Delay (Bidirectional Pad)	1.4	1.9	2.3	3.0	4.8	6.7	8.5	ns	
t _{GCK}	Clock Buffer Delay ^[5]	2.7	2.8	2.9	3.0	3.1	3.3	3.4	ns	
t _{GCKHI}	Clock Buffer Min. HIGH ^[5]	2.0	2.0	2.0	2.0	2.0	2.0	2.0	ns	
t _{GCKLO}	Clock Buffer Min. LOW ^[5]	2.0	2.0	2.0	2.0	2.0	2.0	2.0	ns	

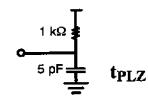
Parameter	Description	Propagation Delays ^[3] with Output Load Capacitance (pF) of					Unit
		30	50	75	100	150	
OUTPUT CELLS							
t _{OUTLH}	Output Delay LOW to HIGH	2.7	3.3	3.8	4.3	5.4	ns
t _{OUTH}	Output Delay HIGH to LOW	2.8	3.7	4.5	5.3	6.9	ns
t _{PZH}	Output Delay Three-State to HIGH	2.1	2.6	3.1	3.7	4.8	ns
t _{PZL}	Output Delay Three-State to LOW	2.6	3.3	4.1	4.9	6.5	ns
t _{PHZ}	Output Delay HIGH to Three-State ^[6]	2.9					ns
t _{PLZ}	Output Delay LOW to Three-State ^[6]	3.3					ns

Notes:

- Worst-case propagation delay times over process variation at V_{CC} = 3.3V and T_A = 25°C. Multiply by the appropriate delay factor, K, for speed grade to get worst-case parameters over full V_{CC} and temperature range as specified in the operating range. All inputs are TTL with 3-ns linear transition time between 0 and 3 volts.
- These limits are derived from worst-case values for a representative selection of the slowest paths through the pASIC380 logic cell including net delays. Guaranteed delay values for specific paths should be determined from simulation results.
- Clock buffer fanout refers to the maximum number of flip-flops per half column. The number of half columns used does not affect clock buffer delay.
- The following loads are used for t_{PHZ}:



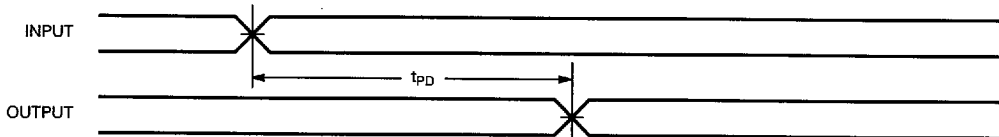
t_{PHZ}



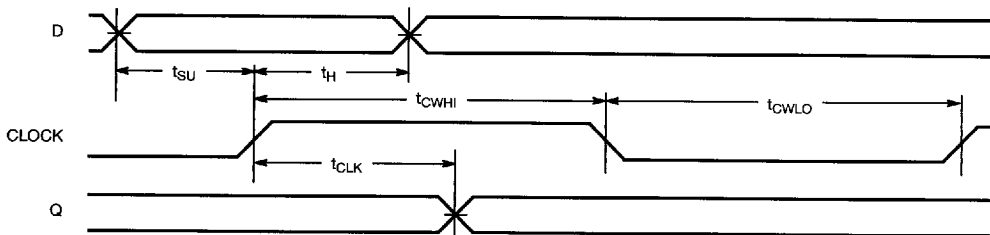
t_{PLZ}

High Drive Buffer

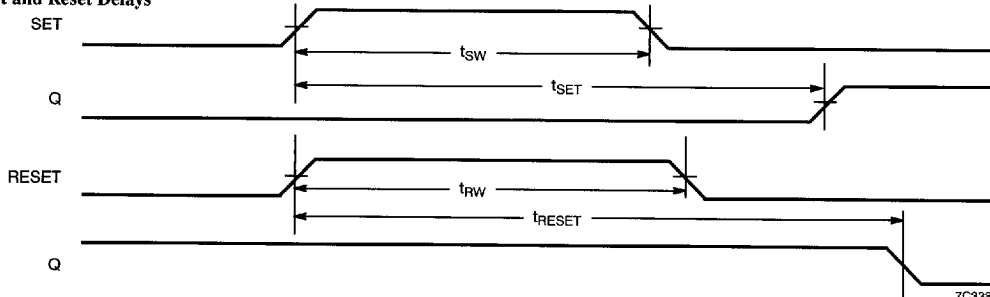
Parameter	Description	# High Drives Wired Together	Propagation Delays ^[3] with Fanout of					Unit
			12	24	48	72	96	
t_{IN}	High Drive Input Delay	1	5.8	7.3				ns
		2		5.0	7.1			ns
		3			5.8	6.7	7.7	ns
		4				5.4	6.8	ns
t_{INi}	High Drive Input, Inverting Delay	1	6.0	7.4				ns
		2		5.2	7.3			ns
		3			6.0	6.9	7.9	ns
		4				6.1	7.0	ns

Switching Waveforms
Combinatorial Delay


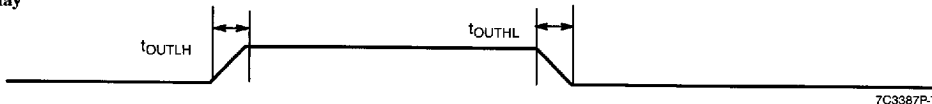
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Set-Up and Hold Times


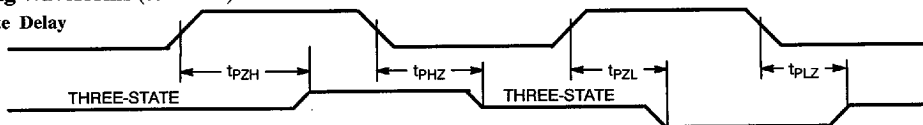
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Set and Reset Delays


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Output Delay


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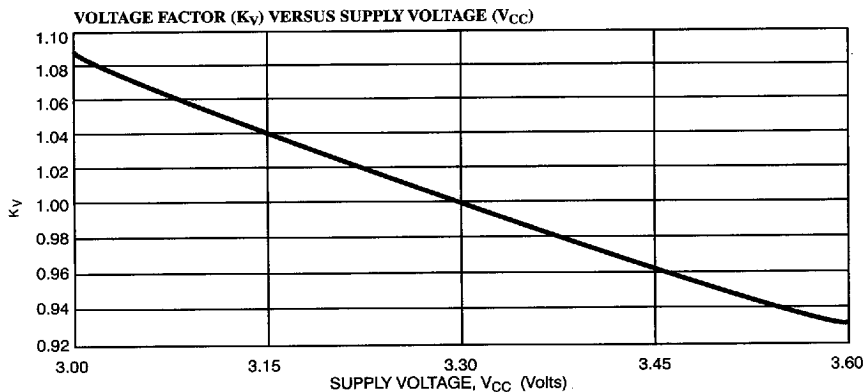
Switching Waveforms (continued)
Three-State Delay


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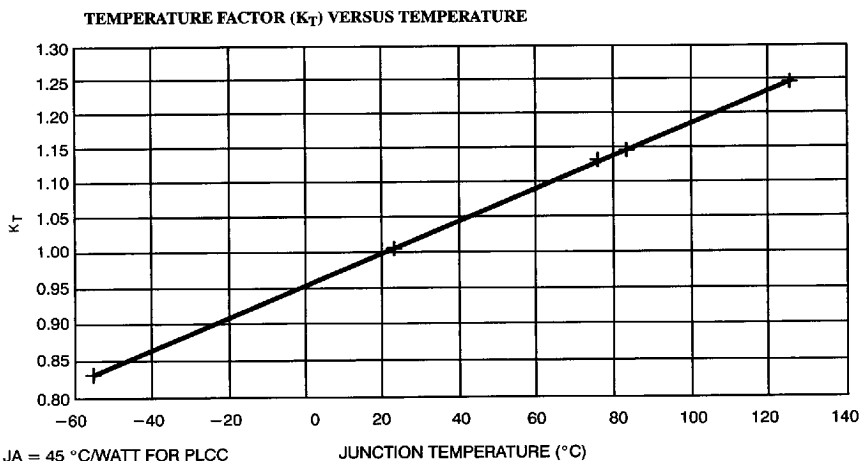
Typical AC Characteristics

Propagation delays depend on routing, fanout, load capacitance, supply voltage, junction temperature, and process variation. The AC Characteristics are a design guide to provide initial timing estimates at nominal conditions. Worst-case estimates are obtained when nominal propagation delays are multiplied by the appropriate

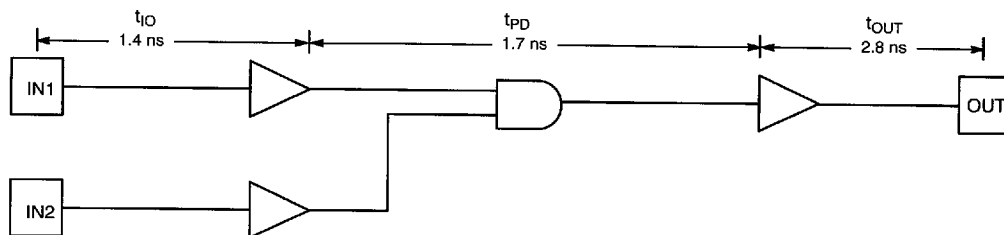
Delay Factor, K , as specified by the speed grade in the Delay Factor table. The effects of voltage and temperature variation are illustrated in the graphs below. The *Warp3* Delay Modeler extracts specific timing parameters for precise simulation results following place and route.



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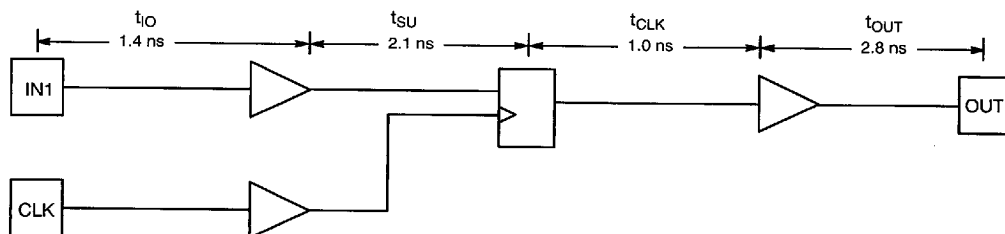


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Combinatorial Delay Example (Load = 30 pF, Fanout =1, K=1.0)


INPUT DELAY + COMBINATORIAL DELAY + OUTPUT DELAY = 5.9 ns

7C3387P-11

Sequential Delay Example (Load = 30 pF, Fanout =1, K=1.0)


INPUT DELAY + REG SET-UP + CLOCK TO Q DELAY + OUTPUT DELAY = 7.3 ns

7C3387P-12

4

Ordering Information

Speed Grade	Ordering Code	Package Name	Package Type	Operating Range
1	CY7C3387P-1AC	A144	144-Pin Thin Quad Flat Pack	Commercial
	CY7C3387P-1AI	A144	144-Pin Thin Quad Flat Pack	Industrial
0	CY7C3387P-0AC	A144	144-Pin Thin Quad Flat Pack	Commercial
	CY7C3387P-0AI	A144	144-Pin Thin Quad Flat Pack	Industrial
X	CY7C3387P-XAC	A144	144-Pin Thin Quad Flat Pack	Commercial
	CY7C3387P-XAI	A144	144-Pin Thin Quad Flat Pack	Industrial

Speed Grade	Ordering Code	Package Name	Package Type	Operating Range
1	CY7C3388P-1NC	N208	208-Pin Plastic Quad Flat Pack	Commercial
	CY7C3388P-1NI	N208	208-Pin Plastic Quad Flat Pack	Industrial
0	CY7C3388P-0NC	N208	208-Pin Plastic Quad Flat Pack	Commercial
	CY7C3388P-0NI	N208	208-Pin Plastic Quad Flat Pack	Industrial
X	CY7C3388P-XNC	N208	208-Pin Plastic Quad Flat Pack	Commercial
	CY7C3388P-XNI	N208	208-Pin Plastic Quad Flat Pack	Industrial

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