FEDL7022-01-06

# OKI Semiconductor

This version: May 2000
Previous version: Sep. 1999

# ML7022-01

**Single Rail Dual Channel PCM CODEC**

## GENERAL DESCRIPTION

The ML7022 is a two-channel single-rail CODEC CMOS IC for voice signals ranging from 300 to 3400Hz. This device contains two-channel analog-to-digital (A/D) and digital-to-analog (D/A) converters on a single chip. The ML7022 is designed especially for a single power supply and low power applications and achieves a reduced footprint.
The ML7022 is best suited for line card applications with easy interface to subscriber line interface circuits (SLICs). The SLIC interface latches are embedded onto this CODEC, thus eliminating the need for external components and optimizing board space.

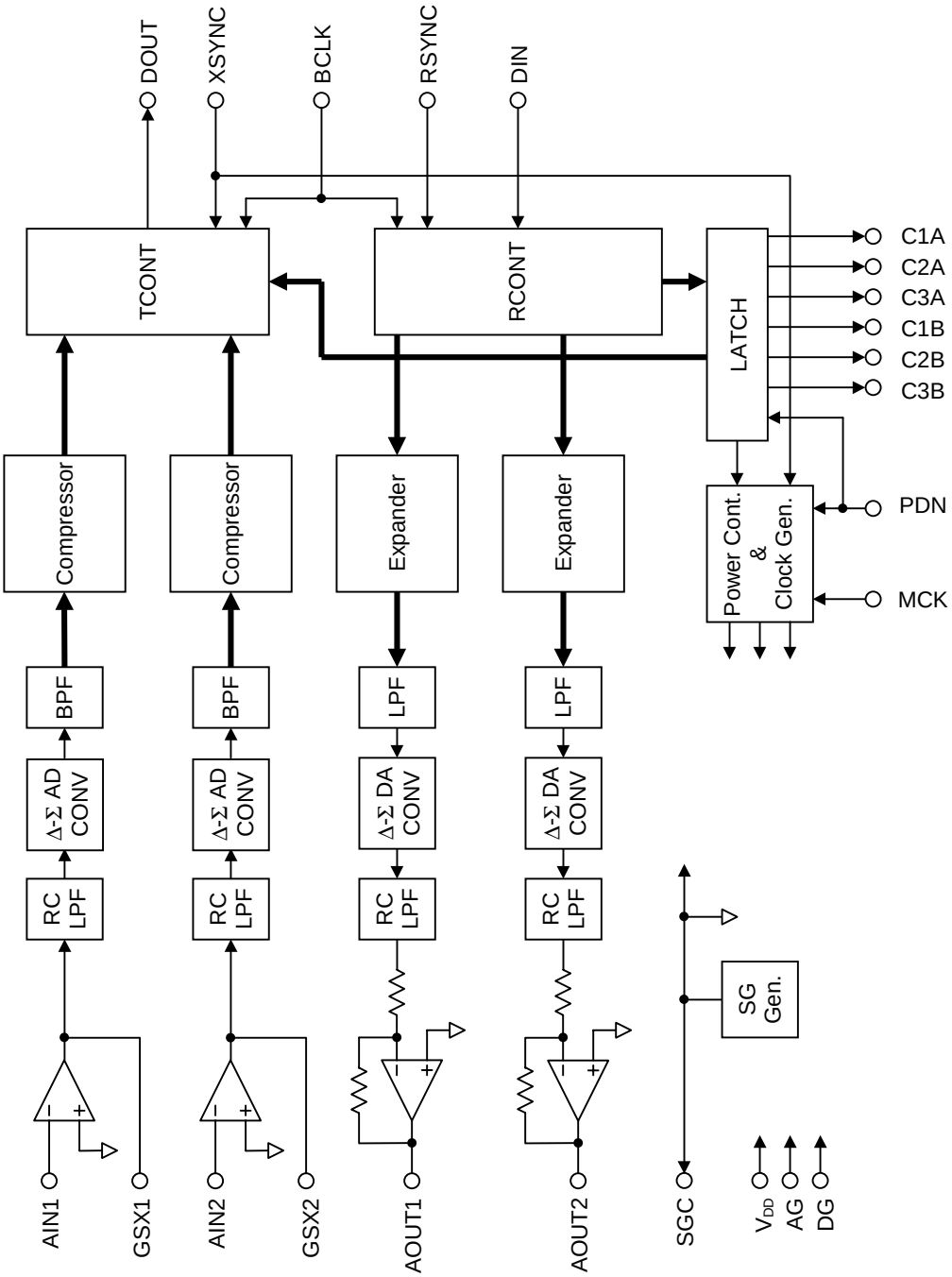
## FEATURES

- Single 5 V Power Supply Operation
- Using Δ-Σ ADC and DAC Technique
- Low Power Consumption

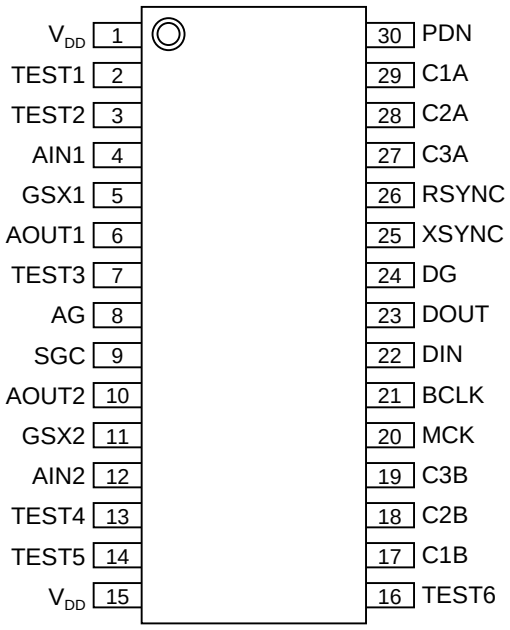
| | | | | |
|---|---|---|---|---|
| 2-Channel Operating Mode: | typical: | 70 mW | max.: | 90 mW |
| 1-Channel Operating Mode: | typical: | 40 mW | max.: | 55 mW |
| Power Saving Mode: (CPD1 = CPD2 = “0”) | typical: | 9 mW | max.: | 12.5 mW |
| Power Down Mode: (PDN = “0”) | typical: | 0.05 mW | max.: | 0.25 mW |

- ITU-T Companding Law - μ-law
- Built-in Dual 3-bit Latches with CMOS Drive Capability
- Serial PCM Interface
- Master Clock: 4.096 MHz
- Transmission Clocks:
  256 to 4096 kbps
- Adjustable Transmit Gain
- Built-in Reference Voltage Supply
- Analog Output can Directly Drive a 600Ω Line Transformer
- Latched Content Echo-back Function
- Package Type:
  30-pin plastic SSOP (SSOP30-P-56-0.65-K) (Product name: ML7022-01MB)

## BLOCK DIAGRAM



## PIN CONFIGURATION (TOP VIEW)




**30-Pin Plastic SSOP**

## PIN DESCRIPTIONS

| Pin | Symbol | Type | Description |
|---|---|---|---|
| 1 | $V_{DD}$ | — | Power Supply * |
| 2 | TEST1 | I | Device Test Pin 1 |
| 3 | TEST2 | I | Device Test Pin 2 |
| 4 | AIN1 | I | Channel-1 Transmit Op-amp Input |
| 5 | GSX1 | O | Channel-1 Transmit Op-amp Output |
| 6 | AOUT1 | O | Channel-1 Receive Output |
| 7 | TEST3 | I | Device Test Pin 3 |
| 8 | AG | — | Analog Ground |
| 9 | SGC | O | Signal Ground |
| 10 | AOUT2 | O | Channel-2 Receive Output |
| 11 | GSX2 | O | Channel-2 Transmit Op-amp Output |
| 12 | AIN2 | I | Channel-2 Transmit Op-amp Input |
| 13 | TEST4 | I | Device Test Pin 4 |
| 14 | TEST5 | I | Device Test Pin 5 |
| 15 | $V_{DD}$ | — | Power Supply * |
| 16 | TEST6 | I | Device Test Pin 6 |
| 17 | C1B | O | C1B Bit Latched Output |
| 18 | C2B | O | C2B Bit Latched Output |
| 19 | C3B | O | C3B Bit Latched Output |
| 20 | MCK | I | Master Clock (4.096 MHz) |
| 21 | BCLK | I | Shift Clock for the DIN and DOUT |
| 22 | DIN | I | Data Input |
| 23 | DOUT | O | Data Output |
| 24 | DG | — | Digital Ground |
| 25 | XSYNC | I | Transmit Synchronizing Signal |
| 26 | RSYNC | I | Receive Synchronizing Signal |
| 27 | C3A | O | C3A Bit Latched Output |
| 28 | C2A | O | C2A Bit Latched Output |
| 29 | C1A | O | C1A Bit Latched Output |
| 30 | PDN | I | Power Down Control |

* $V_{DD}$ of pin 1 and $V_{DD}$ of pin 15 are connected internally, but these pins must be connected on the printed circuit board.

## ABSOLUTE MAXIMUM RATINGS

| Parameter | Symbol | Condition | Rating | Unit |
|---|---|---|---|---|
| Power Supply Voltage | $V_{DD}$ | — | –0.3 to +7.0 | V |
| Analog Input Voltage | $V_{AIN}$ | — | –0.3 to $V_{DD}$+0.3 | V |
| Digital Input Voltage | $V_{DIN}$ | — | –0.3 to $V_{DD}$+0.3 | V |
| Storage Temperature | $T_{STG}$ | — | –55 to +150 | °C |

## RECOMMENDED OPERATING CONDITIONS

| Parameter | Symbol | Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| Power Supply Voltage | $V_{DD}$ | Voltage must be fixed | 4.75 | 5.0 | 5.25 | V |
| Operating Temperature | $T_{OP}$ | — | –40 | — | +85 | °C |
| Analog Input Voltage | $V_{AIN}$ | Gain = 1 | — | — | 3.4 | $V_{PP}$ |
| High Level Input Voltage | $V_{IH}$ | All Digital Input Pins | 2.2 | — | $V_{DD}$ | V |
| Low Level Input Voltage | $V_{IL}$ | | 0 | — | 0.8 | V |
| MCK Frequency | $F_{MCK}$ | MCK | –0.01% | 4096 | +0.01% | kHz |
| BCLK Frequency | $F_{BCLK}$ | BCLK | 256 | — | 4096 | kHz |
| Sync Pulse Frequency | $F_{SYNC}$ | XSYNC, RSYNC | — | 8 | — | kHz |
| Clock Duty Ratio | $D_{CLK}$ | MCK, BCLK | 40 | 50 | 60 | % |
| Digital Input Rise Time | $T_{IR}$ | All Digital Input Pins | — | — | 50 | ns |
| Digital Input Fall Time | $T_{IF}$ | | — | — | 50 | ns |
| MCK to BCLK Phase Difference | $T_{MB}$ | MCK, BCLK | — | — | 50 | ns |
| Transmit Sync Pulse Setting Time | $T_{XS}$ | BCLK to XSYNC | 50 | — | — | ns |
| | $T_{SX}$ | XSYNC to BCLK | 50 | — | — | ns |
| Receive Sync Pulse Setting Time | $T_{RS}$ | BCLK to RSYNC | 50 | — | — | ns |
| | $T_{SR}$ | RSYNC to BCLK | 50 | — | — | ns |
| Sync Pulse Width | $T_{WS}$ | XSYNC, RSYNC | 1 BCLK | — | 100 | µs |
| DIN Set-up Time | $T_{DS}$ | DIN | 50 | — | — | ns |
| DIN Hold Time | $T_{DH}$ | DIN | 50 | — | — | ns |
| Digital Output Load | $R_{DL}$ | Pull-up Resistor, DOUT | 0.5 | — | — | kΩ |
| | $C_{DL}$ | DOUT | — | — | 50 | pF |
| | | C1A, C2A, C3A,C1B, C2B, C3B | — | — | 50 | pF |
| Bypass Capacitor for SGC | $C_{SG}$ | SG to AG | 0.1 | — | — | µF |

## ELECTRICAL CHARACTERISTICS

### DC and Digital Interface Characteristics

($V_{DD}$ = 4.75 to 5.25 V, Ta = –40 to +85°C)

| Parameter | Symbol | Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| Power Supply Current | $I_{DD1}$ | 2CH Operating Mode, No Signal PDN = "1", CPD1 = CPD2 = "1" | — | 14.0 | 18.0 | mA |
| | $I_{DD2}$ | 1CH Operating Mode, No Signal PDN = "1", CPD1 = "1", CPD2 = "0" or PDN = "1", CPD1 = "0", CPD2 = "1" | — | 8.0 | 11.0 | mA |
| | $I_{DD3}$ | Power Saving Mode, PDN = "1", CPD1 = CPD2 = "0" | — | 1.8 | 2.5 | mA |
| | $I_{DD4}$ | Power Down Mode, PDN = "0" | — | 0.01 | 0.05 | mA |
| High Level Input Leakage Current | $I_{IH}$ | All Digital Input Pins $V_I = V_{DD}$ | — | — | 2.0 | µA |
| Low Level Input Leakage Current | $I_{IL}$ | All Digital Input Pins $V_I$ = 0 V | — | — | 0.5 | µA |
| Digital Output Low Voltage | $V_{OL}$ | DOUT, Pull-up = 0.5 kΩ | 0 | 0.2 | 0.4 | V |
| | | C1A, C2A, C3A, C1B, C2B, C3B $I_{OL}$ = 0.4 mA | 0 | 0.2 | 0.4 | V |
| Digital Output High Voltage | $V_{OH}$ | C1A, C2A, C3A, C1B, C2B, C3B $I_{OH}$ = 0.4 mA | 2.5 | — | — | V |
| | | C1A, C2A, C3A, C1B, C2B, C3B $I_{OH}$ = 50 µA | $V_{DD}$ –0.5 | — | — | V |
| Digital Output Leakage Current | $I_O$ | DOUT High Impedance State | — | — | 10 | µA |
| Input Capacitance | $C_{IN}$ | — | — | 5 | — | pF |

### Analog Interface Characteristics

($V_{DD}$ = 4.75 to 5.25 V, Ta = –40 to +85°C)

| Parameter | Symbol | Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| SGC Rise Time | $T_{SGC}$ | SG to AG 0.1 µF Rise time to 90% of max. level | — | — | 10 | ms |

### Transmit Analog Interface Characteristics

($V_{DD}$ = 4.75 to 5.25 V, Ta = –40 to +85°C)

| Parameter | Symbol | Condition | | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|---|
| Input Resistance | $R_{INX}$ | AIN1, AIN2 | | 10 | — | — | MΩ |
| Output Load Resistance | $R_{LGX}$ | GSX1, GSX2 with respect to SG *1 | | 20 | — | — | kΩ |
| Output Load Capacitance | $C_{LGX}$ | | | — | — | 30 | pF |
| Output Amplitude | $V_{OGX}$ | | | –1.13 | — | 1.13 | V |
| Offset Voltage | $V_{OSGX}$ | | Gain = 1 | –20 | — | 20 | mV |

*1 0.27 dBm (600Ω) = 3.17 dBm0 (µ-law) = 2.26 $V_{PP}$

### Receive Analog Interface Characteristics

($V_{DD}$ = 4.75 to 5.25 V, Ta = –40 to +85°C)

| Parameter | Symbol | Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| Output Load Resistance | $R_{LAO}$ | AOUT1, AOUT2 (each) with respect to SG | 0.6 | — | — | kΩ |
| Output Load Capacitance | $C_{LAO}$ | AOUT1, AOUT2 | — | — | 50 | pF |
| Output Amplitude | $V_{OAO}$ | AOUT1, AOUT2, $R_{LAO}$ = 0.6 kΩ with respect to SG | –1.7 | — | 1.7 | V |
| Offset Voltage | $V_{OSAO}$ | AOUT1, AOUT2 with respect to SG | –100 | — | 100 | mV |

### AC Characteristics

($V_{DD}$ = 4.75 to 5.25 V, Ta = –40 to +85°C)

| Parameter | Symbol | Condition | | | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|---|---|
| | | Freq. (Hz) | Level (dBm0) | | | | | |
| Transmit Frequency Response | Loss T1 | 60 | 0 | GSXn to DOUT (Attenuation) | 25 | 45 | — | dB |
| | Loss T2 | 300 | | | –0.15 | 0.15 | 0.20 | |
| | Loss T3 | 1020 | | | Reference | | | |
| | Loss T4 | 3000 | | | –0.15 | 0.02 | 0.20 | |
| | Loss T5 | 3300 | | | –0.15 | 0.1 | 0.80 | |
| | Loss T6 | 3400 | | | 0 | 0.6 | 0.80 | |
| Receive Frequency Response | Loss R1 | 100 | 0 | DIN to AOUTn (Attenuation) | –0.15 | 0.04 | 0.2 | dB |
| | Loss R2 | 1020 | | | Reference | | | |
| | Loss R3 | 3000 | | | –0.15 | 0.07 | 0.2 | |
| | Loss R4 | 3300 | | | –0.15 | 0.2 | 0.8 | |
| | Loss R5 | 3400 | | | 0 | 0.6 | 0.8 | |
| Transmit Signal to Distortion Ratio | SDT1 | 1020 | 3 | GSXn to DOUT *2 | 36 | 43 | — | dB |
| | SDT2 | | 0 | | 36 | 40 | — | |
| | SDT3 | | –30 | | 36 | 38 | — | |
| | SDT4 | | –40 | | 30 | 32 | — | |
| | SDT5 | | –45 | | 25 | 29 | — | |
| Receive Signal to Distortion Ratio | SDR1 | 1020 | 3 | DIN to AOUTn *2 | 36 | 42 | — | dB |
| | SDR2 | | 0 | | 36 | 39 | — | |
| | SDR3 | | –30 | | 36 | 39 | — | |
| | SDR4 | | –40 | | 30 | 33 | — | |
| | SDR5 | | –45 | | 25 | 30 | — | |
| Transmit Gain Tracking | GTT1 | 1020 | 3 | GSXn to DOUT | –0.2 | 0.02 | 0.2 | dB |
| | GTT2 | | –10 | | Reference | | | |
| | GTT3 | | –40 | | –0.2 | 0.06 | 0.2 | |
| | GTT4 | | –50 | | –0.6 | 0.4 | 0.6 | |
| | GTT5 | | –55 | | –1.2 | 0.4 | 1.2 | |
| Receive Gain Tracking | GTR1 | 1020 | 3 | DIN to AOUTn | –0.2 | 0 | 0.2 | dB |
| | GTR2 | | –10 | | Reference | | | |
| | GTR3 | | –40 | | –0.2 | –0.02 | 0.2 | |
| | GTR4 | | –50 | | –0.6 | –0.1 | 0.6 | |
| | GTR5 | | –55 | | –1.2 | –0.2 | 1.2 | |
| Idle Channel Noise | $NIDLE_T$ | — | — | AINn = SG *2 AINn to DOUT | — | 14 | 16 | dBrnc0 |
| | $NIDLE_R$ | — | — | DIN = 0 code *2 DIN to AOUTn | — | 6 | 10 | |

*2 C-message Filter is used

**AC Characteristics (Continued)**

($V_{DD}$ = 4.75 to 5.25 V, Ta = –40 to +85°C)

| Parameter | Symbol | Condition | | | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|---|---|
| | | Freq. (Hz) | Level (dBm0) | | | | | |
| Absolute Level (Initial Difference) | $AV_T$ | 1020 | 0 | GSXn to DOUT $V_{DD}$ = 5 V, Ta = 25°C | 0.535 | 0.555 | 0.574 | Vrms |
| | $AV_R$ | | | DIN to AOUTn $V_{DD}$ = 5 V, Ta = 25°C | 0.806 | 0.835 | 0.864 | |
| Absolute level (Deviation of Temperature and power) | $AV_{TT}$ | | | $V_{DD}$ = 4.75 to 5.25 V Ta = –40 to 85°C | –0.3 | — | 0.3 | dB |
| | $AV_{RT}$ | | | | –0.3 | — | 0.3 | |
| Absolute Delay | $T_D$ | 1020 | 0 | A to A Mode BCLK = 2048 kHz | — | 0.58 | 0.6 | ms |
| Transmit Group Delay | $T_{GD}$ T1 | 500 | 0 | *3 | — | 0.26 | 0.75 | ms |
| | $T_{GD}$ T2 | 600 | | | — | 0.16 | 0.35 | |
| | $T_{GD}$ T3 | 1000 | | | — | 0.02 | 0.125 | |
| | $T_{GD}$ T4 | 2600 | | | — | 0.05 | 0.125 | |
| | $T_{GD}$ T5 | 2800 | | | — | 0.07 | 0.75 | |
| Receive Group Delay | $T_{GD}$ R1 | 500 | 0 | *3 | — | 0.00 | 0.75 | ms |
| | $T_{GD}$ R2 | 600 | | | — | 0.00 | 0.35 | |
| | $T_{GD}$ R3 | 1000 | | | — | 0.00 | 0.125 | |
| | $T_{GD}$ R4 | 2600 | | | — | 0.09 | 0.125 | |
| | $T_{GD}$ R5 | 2800 | | | — | 0.12 | 0.75 | |
| Cross Talk Attenuation | $CR_T$ | 1020 | 0 | Trans to Receive | 75 | 83 | — | dB |
| | $CR_R$ | | | Receive to Trans | 75 | 80 | — | |
| | $CR_{CH}$ | | | Channel to Channel | 75 | 78 | — | |
| Discrimination | DIS | 4.6 to 72k | 0 | 0 to 4 kHz | 30 | 32 | — | dB |
| Out of Band Spurious | OBS | 300 to 3.4k | 0 | 4.6 kHz to 1000 kHz | — | –37.5 | –35 | dB |
| Signal Frequency Distortion | $SFD_T$ | 1020 | 0 | 0 to 4 kHz | — | –50 | –40 | dBm0 |
| | $SFD_R$ | | | | — | –48 | –40 | |
| Intermoduration Distortion | $IMD_T$ | fa = 470 fb = 320 | –4 | 2 fa - fb | — | –50 | –40 | dBm0 |
| | $IMD_R$ | | | | — | –54 | –40 | |
| Power Supply Noise Rejection Ratio | $PSR_{T1}$ | 0 to 4k | 100 mVrms | *4 | 40 | 44 | — | dB |
| | $PSR_{T2}$ | 4 to 50k | | | 50 | 55 | — | |
| | $PSR_{R1}$ | 0 to 4k | | | 40 | 45 | — | |
| | $PSR_{R2}$ | 4 to 50k | | | 50 | 56 | — | |
| Digital Output Delay Time | $T_{SD}$ | DOUT Pull-up resister = 0.5 kΩ $C_L$ = 50 pF and 1 LSTTL | | | 20 | — | 100 | ns |
| | $T_{XD1}$ | | | | 20 | — | 100 | |
| | $T_{XD2}$ | | | | 20 | — | 100 | |
| | $T_{PDC}$ | C1A, C2A, C3A, C1B, C2B, C3B $C_L$ = 50 pF and 1 LSTTL | | | 20 | — | 1000 | ns |
| DOUT Operation Delay Time | $T_{DDO}$ | Time of operation start after power on | | | — | 4 | — | ms |
| AOUT Signal Output Delay Time | $T_{DAO}$ | Time of base band signal output start after power on | | | — | 4 | — | ms |

*3 Minimum value of the group delay distortion

*4 The measurement under idle channel noise

## TIMING DIAGRAM

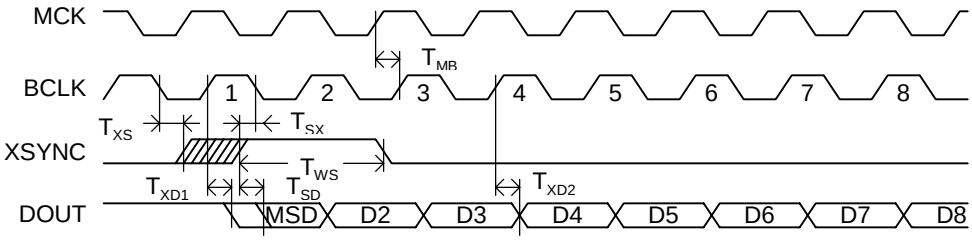



**Figure 1 Transmit Side Timing Diagram**

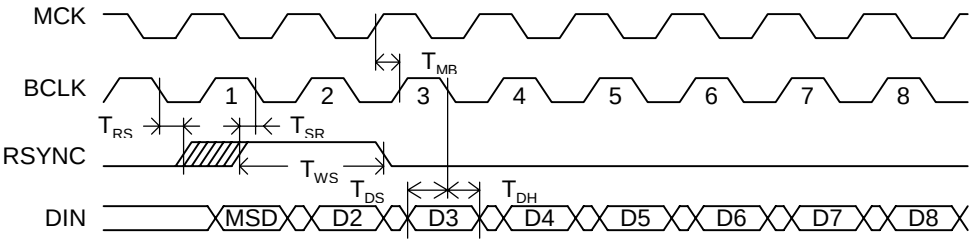



**Figure 2 Receive Side Timing Diagram**

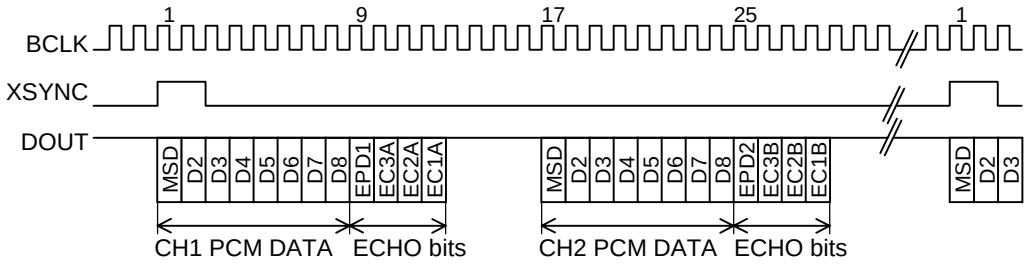



**Figure 3 Transmit Side Bit Configuration**

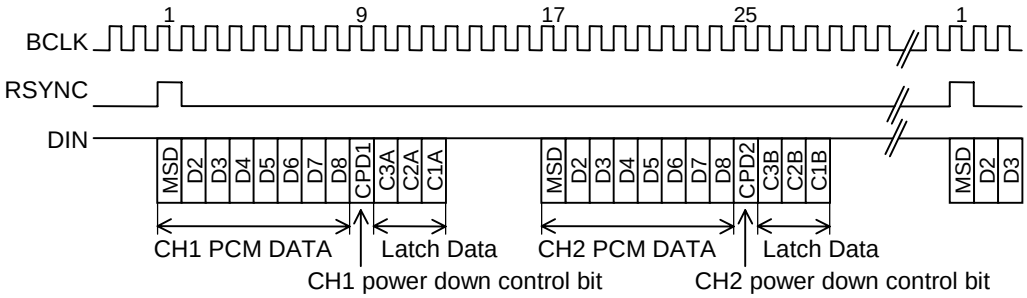



**Figure 4 Receive Side Bit Configuration**

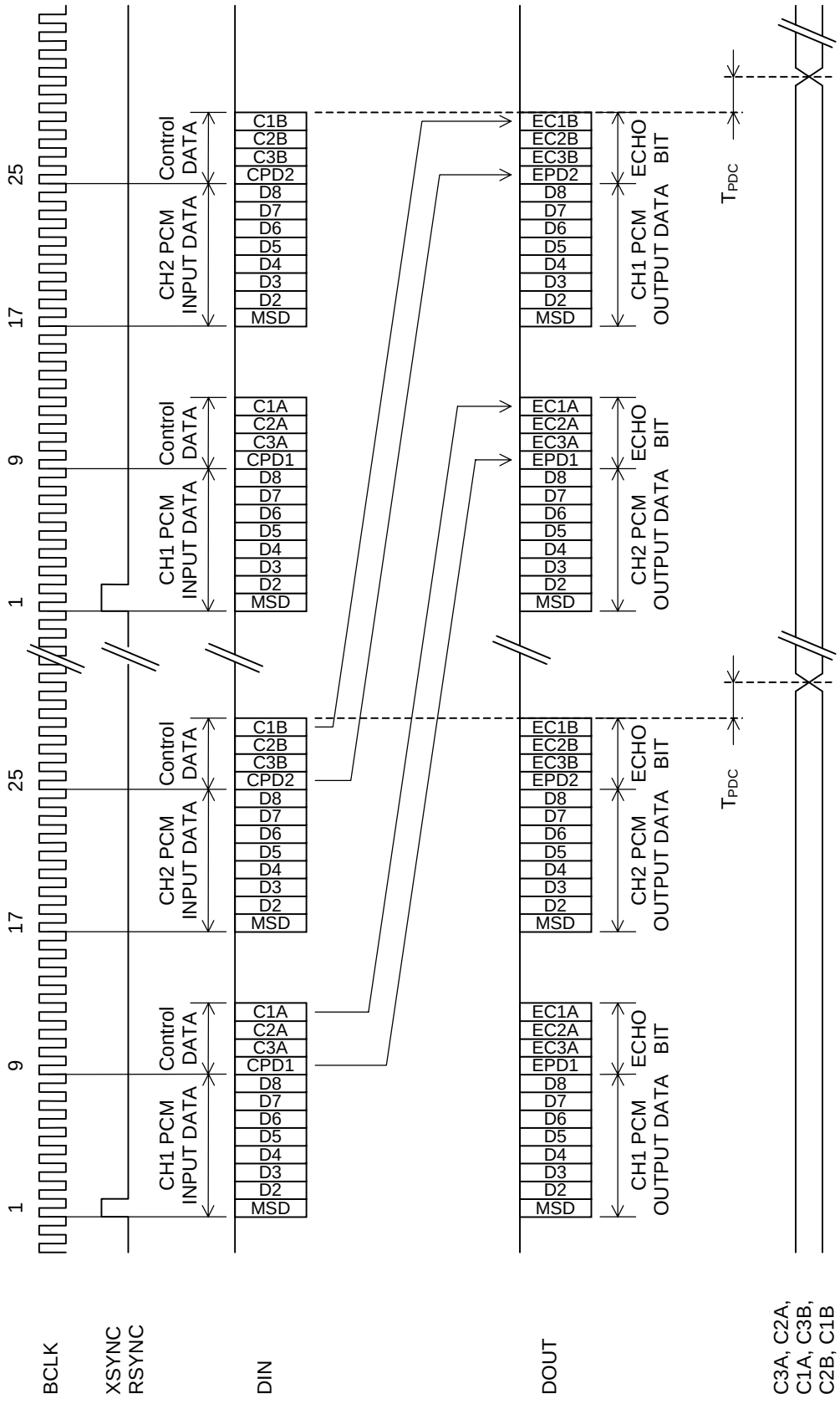



**Figure 5 Control Bit Timing and Echo Back Timing**

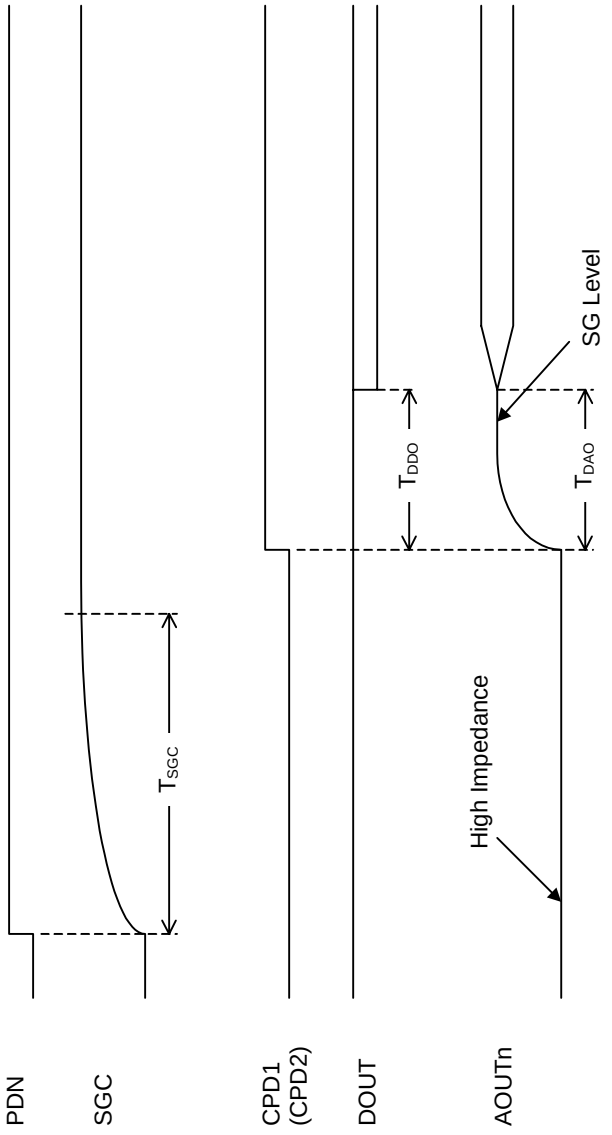


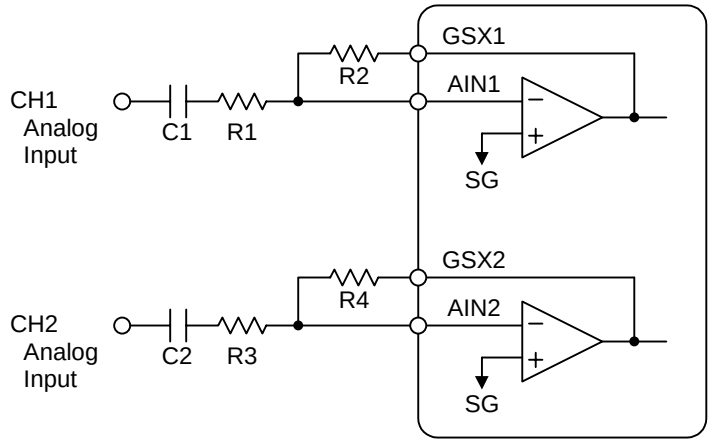

**Figure 6 SGC, DOUT and AOUT Output Timing**

## FUNCTIONAL DESCRIPTION

### Pin Functional Description

**AIN1, AIN2, GSX1, GSX2**

AIN1 and AIN2 are the transmit analog inputs for Channels 1 and 2.
GSX1 and GSX2 are the transmit level adjustments for Channels 1 and 2.
AIN1 and AIN2 are inverting inputs for the op-amp; GSX1 and GSX2 are connected to the output of the op-amp and are used to adjust the level, as shown below.
If AIN1 and AIN2 are not used, connect AIN1 to GSX1 and AIN2 to GSX2. During power saving and power down mode, the GSX1 and GSX2 outputs are at AG voltage.
In the case of the analog input 2.26 Vpp at GSX pin with digital output +3.17 dBm0 (μ-law).




CH1 Gain
Gain = R2/R1 ≤ 10
R1: Variable
R2 > 20 kΩ
C1 > 1/ (2 × 3.14 × 30 × R1)

CH2 Gain
Gain = R4/R3 ≤ 10
R3: Variable
R4 > 20 kΩ
C2 > 1/ (2 × 3.14 × 30 × R3)

**AOUT1, AOUT2**

AOUT1 is the receive analog output for Channel 1 and AOUT2 is used for Channel 2.
The output signal has an amplitude of 3.4Vpp above and below the signal ground voltage (SG).When the digital signal of +3.17 dBm0 is input to DIN, it can drive a load of 600Ω or more.
During power saving or power down mode, these outputs are at a high impedance.

**$V_{DD}$**

Power supply for +5 V.
Connect a bypass capacitor of 0.1 μF with excellent high frequency characteristics between this pin and the AG pin.
Although $V_{DD}$ pin 1 and $V_{DD}$ pin 15 are connected internally, these pins must be connected on the printed circuit board.

**AG**
Ground for the analog signal circuits.

**DG**
Ground for the digital signal circuits.
This ground is separate from the analog signal ground. The DG pin must be connected to the AG pin on the printed circuit board to make a common analog ground.

**SGC**
Used to generate the signal ground voltage level, by connecting a bypass capacitor. Connect a 0.1 μF capacitor with excellent high frequency characteristics between the AG pin and the SGC pin.
During power down mode, this outputs are at the voltage level of AG with about 50 kΩ impedance.

**MCK**
Master clock input.
The frequency must be 4.096 MHz.

**BCLK**
Shift clock signal input for the DIN and DOUT signals.
The frequency, equal to the data rate, is 256 k to 4096 kHz. This signal must be synchronized in phase with the MCK (generated from the same clock source as MCK). Figure 1 shows the phase difference of MCK and BCLK.

**RSYNC**
Receive synchronizing signal input.
Signals in the receive section are synchronized by this synchronizing signal. This signal must be synchronized in phase with the MCK (generated from the same clock source as MCK).

**XSYNC**
Transmit synchronizing signal input.
The PCM output signal from the DOUT pin is output in synchronization with this transmit synchronizing signal. This synchronizing signal synchronizes all timing signals of all section. This signal must be synchronized in phase with the MCK (generated from the same clock source as MCK).

**DIN**

DIN is a data input pin.

The voice band signal is converted to an analog signal in synchronization with the RSYNC signal and BCLK. The analog signal of channel 1 is output from AOUT1 pin and the analog signal of channel 2 is output from AOUT2 pin.

The 28 bit signal structure is shown in Figure 4. It consists of voice band PCM signals (8 bits each), the general-purpose latch signal (6 bits total), the power down control signal (1 bit per channel) and empty bits (4 bits). The signal is shifted at a falling edge of the BCLK signal and latched into the internal register when shifted by 28 bits. The start of the PCM data (Channel 1's MSD) is identified at the rising edge of RSYNC.

The general purpose latch signal (C3A, C2A, C1A, C3B, C2B, C1B) are output from six latch output pins.

When the CPD1 (bit of DIN) = "0", Channel 1 block is in a power down state. When the CPD2 (bit of DIN) = "0", Channel 2 block is in a power down state.

**DOUT**

DOUT is a data output pin.

The signal consist of a total of 28 bits containing the voice band PCM signals (each channel 8 bits), the echo bit (6 bits for latch signal and 2 bits for power down state indication), and empty bits (4 bits). The output cording format follows ITU-T recommendation on coding law.

The output signal is output from Channel 1's MSD bit in a sequential order, synchronizing with the rising edge of the BCLK signal. The first bit of DOUT may be output at the rising edge of the XSYNC signal, based on the timing between BCLK and XSYNC.

This pin is in a high impedance state during power down state.

A pull-up resistor must be connected to this pin because it is an open drain output.

**Table 1 The Output Cording Format**

| INPUT/OUTPUT Level | PCMIN/PCMOUT | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | μ-law | | | | | | | |
| | MSD | D2 | D3 | D4 | D5 | D6 | D7 | D8 |
| + Full scale | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| +0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| –0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| – Full scale | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**C1A, C2A, C3A, C1B, C2B, C3B**
General-purpose latched output signal.
C1A, C2A, C3A, C1B, C2B, C3B bits of DIN are latched using internal timing.
These outputs can drive a LSTTL/CMOS device without external resistor.

**PDN**
Power down control signal.
When PDN is at logic “0” level, both Channel 1 and Channel 2 circuits are in the power down state. Also, all internal latches are in initial state (logic “0” level).

**TEST1, TEST2, TEST3, TEST4, TEST5, TEST6**
These pins are used for device test.
These device test pin must be connected to the AG pin.

**Table 2 Condition of DOUT by the Power Control**

| PDN | CPD1 | CPD2 | CH1 PCM Data | CH2 PCM Data | CH1 Echo Bit | CH2 Echo Bit |
|---|---|---|---|---|---|---|
| 0 | 0/1 | 0/1 | H | H | H | H |
| 1 | 0 | 0 | 11111111 | 11111111 | Latched Data | Latched Data |
| 1 | 1 | 0 | Operate | 11111111 | | |
| 1 | 0 | 1 | 11111111 | Operate | | |
| 1 | 1 | 1 | Operate | Operate | | |

**Table 3 Condition of the Latched Output by the Power Control**

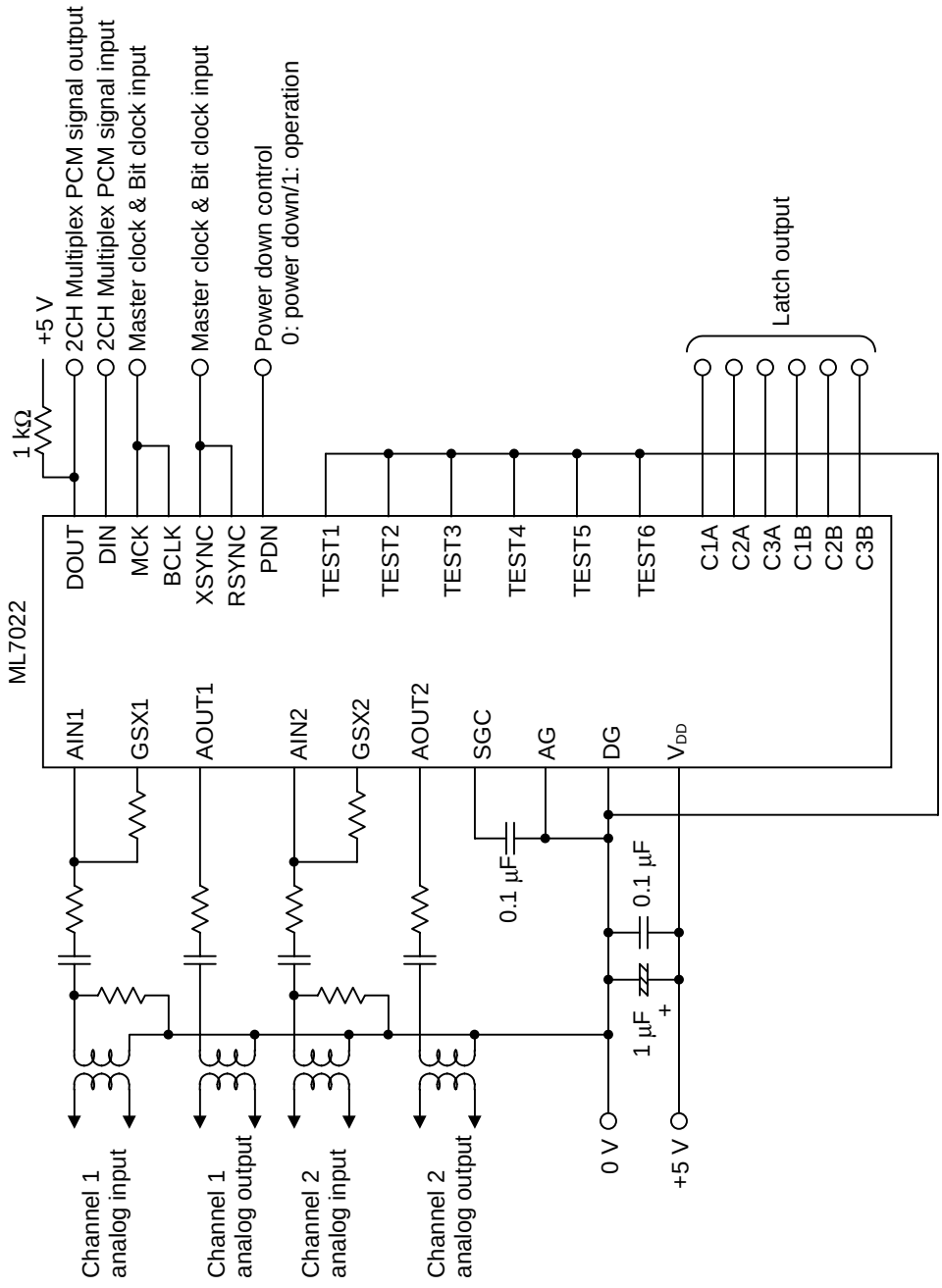
| PDN | CPD1 | CPD2 | LIN | C1A, C2A, C3A | C1B, C2B, C3B |
|---|---|---|---|---|---|
| 0 | 0/1 | 0/1 | 0 | L | L |
| 1 | 0/1 | 0/1 | | Latched Data | Latched Data |
| 0/1 | 0/1 | 0/1 | 1 | L | L |

**Table 4 Condition of the Analog Output by the Power Control**

| PDN | CPD1 | CPD2 | GSX1 | GSX2 | AOUT1 | AOUT2 | SGC |
|---|---|---|---|---|---|---|---|
| 0 | 0/1 | 0/1 | High Impedance | High Impedance | High Impedance | High Impedance | *5 |
| 1 | 0 | 0 | High Impedance | High Impedance | High Impedance | High Impedance | Operate |
| 1 | 1 | 0 | Operate | High Impedance | Operate | High Impedance | Operate |
| 1 | 0 | 1 | High Impedance | Operate | High Impedance | Operate | Operate |
| 1 | 1 | 1 | Operate | Operate | Operate | Operate | Operate |

*5 The voltage level of AG with about 50 kΩ

## APPLICATION CIRCUITS



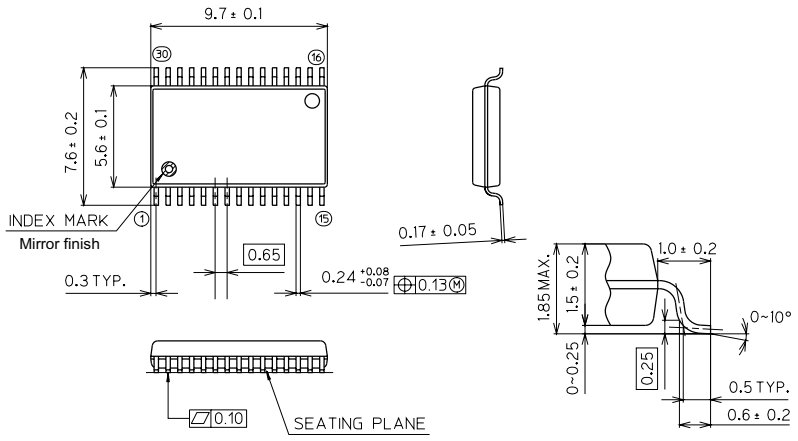
## RECOMMENDATIONS FOR ACTUAL DESIGN

- To assure specified electrical characteristics, use bypass capacitors with excellent high frequency characteristics for the power supply and keep them as close as possible to the device pins.
- Connect the AG pin and DG pin each other as closely as possible. Connect to the system ground with low impedance.
- Unless unavoidable, use short lead type socket.
- When mounted on a frame, use electromagnetic shielding, if any electromagnetic emission sources such as power supply transformers surround the device.
- Keep the voltage on the $V_{DD}$ pin not lower than –0.3 V even instantaneously to avoid latch-up phenomenon when turning the power on.
- Use a low noise power supply (having low level high frequency spike noise or pulse noise) to avoid erroneous operation and the degradation of the characteristics of these device.

## PACKAGE DIMENSIONS

(Unit: mm)

SSOP30-P-56-0.65-K




| | |
|---|---|
| Package material | Epoxy resin |
| Lead frame material | 42 alloy |
| Pin treatment | Solder plating (≥5µm) |
| Package weight (g) | 0.19 TYP. |
| Rev. No./Last Revised | 5/Dec. 5, 1996 |

Oki Electric Industry Co., Ltd.

Notes for Mounting the Surface Mount Type Package

The surface mount type packages are very susceptible to heat in reflow mounting and humidity absorbed in storage.
Therefore, before you perform reflow mounting, contact Oki's responsible sales person for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

NOTICE

1. The information contained herein can change without notice owing to product and/or technical improvements. Before using the product, please make sure that the information being referred to is up-to-date.

2. The outline of action and examples for application circuits described herein have been chosen as an explanation for the standard action and performance of the product. When planning to use the product, please ensure that the external conditions are reflected in the actual circuit, assembly, and program designs.

3. When designing your product, please use our product below the specified maximum ratings and within the specified operating ranges including, but not limited to, operating voltage, power dissipation, and operating temperature.

4. Oki assumes no responsibility or liability whatsoever for any failure or unusual or unexpected operation resulting from misuse, neglect, improper installation, repair, alteration or accident, improper handling, or unusual physical or electrical stress including, but not limited to, exposure to parameters beyond the specified maximum ratings or operation outside the specified operating range.

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