Integrated Device Technology Inc

FAST CMOS EEPROM 16K (2K x 8-BIT)

IDT78C16A

FEATURES:

- 5 volt only operation
- Fast access times
  - Military: 75ns (max.)
  - Commercial: 70ns (max.)
- On-chip timer
  - Automatic byte erase before write
  - Byte write 10ms max.
- $\overline{DATA}$ Polling—detection of write cycle completion
- Low-power CEMOS™ technology
  - 125mA active current
  - 0.9mA standby current (full CMOS)
- Data protection circuitry (V_{CC} lockout for V_{CC} < 3.8V) provides data integrity on power up/power down
- Minimum endurance of 10,000 write cycles per byte
- Endurance failure rate < 0.1% per 1000 cycles
- JEDEC approved byte-wide pinout
- 24-pin THINDIP (300 mil.), 24-pin DIP (600 mil.) and 32-pin LCC
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION:

The IDT78C16A is a 5 volt only 2K x 8 Electrically Erasable Programmable Read-Only Memory (EEPROM). This high-speed CEMOS ™ EEPROM is written on a byte basis and provides 16,384 bits of non-volatile data storage (data retention in excess of 100 years). Its fast read access allows zero wait state read cycles with high-performance microprocessors.

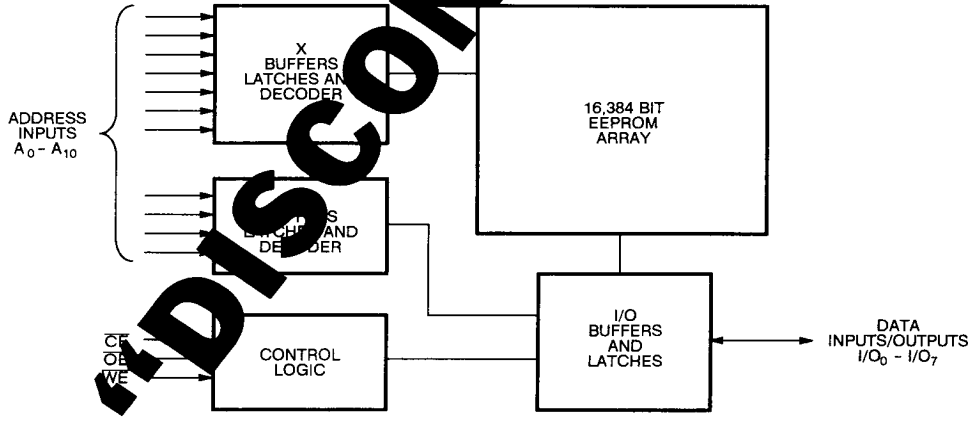
Writing is simplified on internal charge-pump and timer circuit which eliminates the need for special external programming voltage and write pulse shaping circuits. Byte erase before write occurs automatically and input buffers, latches and internal timer free the host system for other tasks during the write cycle. A $\overline{DATA}$ Polling mode provides a method for determining write cycle completion. The IDT78C16A also contains a dual voltage detection logic circuit which allows the device to be used in older applications without complicated external programming circuits.

The IDT78C16A is function- and pinout-compatible with the IDT6116 2K x 8 static RAM. It is ideal for systems requiring non-volatile, in-system data modifications.

Military grade product is manufactured in compliance to the latest revision of MIL-STD-883, Class B, making it ideally suited to military temperature applications demanding the highest level of performance and reliability.

DISCONTINUED

FUNCTIONAL BLOCK DIAGRAM



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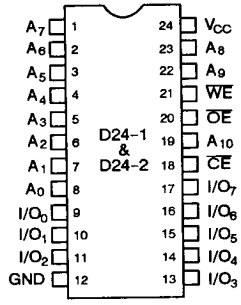
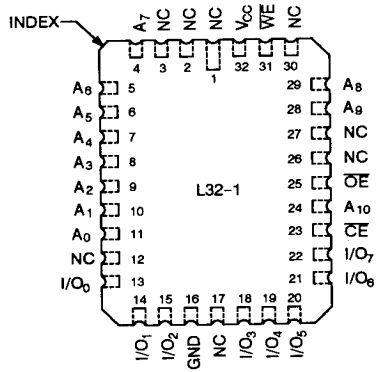
PIN CONFIGURATIONS



DIP
TOP VIEW



LCC
TOP VIEW

PIN NAMES

A_0 - A_3	Addresses-Column
A_4 - A_{10}	Addresses-Row
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
I/O_0 - I/O_7	Data Input (I_0 - I_7) during write; Data Output (O_0 - O_7) during read
V_{CC}	Power
GND	Ground

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DEVICE OPERATIONAL MODE [1]

MODE	PIN			$I/O_0 - I/O_7$
	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	
Read	V_{IL}	V_{IL}	V_{IH}	$Data_{OUT}$ ($O_0 - O_7$)
Byte Write	V_{IL}	V_{IH}	V_{IL}	$Data_{IN}$ ($I_0 - I_7$)
Standby	V_{IH}	Don't Care	Don't Care	High Z
Write Inhibit	Don't Care	V_{IL}	Don't Care	High Z
	Don't Care	Don't Care	V_{IH}	High Z

NOTE:
1. All control inputs are TTL-compatible.

READ MODE

Chip Enable ($\overline{CE}$) and Output Enable ($\overline{OE}$) must be logically active in order for data to be available at the outputs. After a selected byte address is stable, $\overline{CE}$ is taken to a TTL LOW (enabling chip). The Write Enable ($\overline{WE}$) pin should remain deselected (TTL HIGH) during the entire read cycle. Data is gated from the device outputs by selecting the $\overline{OE}$ pin (TTL LOW).

WRITE MODE

The IDT78C16A is programmed electrically in-circuit and does not require any external latching, erasing or timing. Writing to the IDT78C16A is as easy as writing to a static RAM. When a write cycle is initiated, the device automatically latches the address, data and control signals as it begins its write operation.

A write cycle is initiated when both $\overline{CE}$ and $\overline{WE}$ are LOW and $\overline{OE}$ is HIGH. The IDT78C16A supports both a $\overline{CE}$ and $\overline{WE}$ controlled write cycle. All inputs, except for data, are latched on the falling edge of either $\overline{CE}$ or $\overline{WE}$, whichever occurs last. Data is then latched in by the rising edge of either $\overline{CE}$ or $\overline{WE}$, whichever occurred first. An automatic byte erase of the existing data at the addressed location is performed before the new data byte is written. Once initiated, a byte write operation will automatically proceed to completion within 10ms.

STANDBY MODE

The IDT78C16A features a standby mode which reduces the maximum active current from 125mA to 20mA for TTL levels and to 0.9mA for CMOS levels. With $\overline{CE} \geq V_{IH}$ all outputs are in the high impedance state.

DATA PROTECTION

Nonvolatile data is protected from inadvertent writes in the following manner:

Power Up/Down

On-chip circuitry provides protection against false write during V_{CC} power up/down. The IDT78C16A features an internal sensing circuit that disables the internal programming circuit if $V_{CC} < 3.8V$. This prevents input signals at $\overline{CE}$, $\overline{WE}$ and $\overline{OE}$ from triggering a write cycle during a V_{CC} power up/down event.

Noise Protection

The IDT78C16A will typically reject write pulses that are less than 15ns. This prevents spurious noise from initiating a write cycle.

Write Inhibit

Holding either $\overline{OE}$ LOW, $\overline{WE}$ HIGH or $\overline{CE}$ HIGH during a power-on and power-off, will inhibit inadvertent writes.

$\overline{DATA}$ Polling

The IDT78C16A has a maximum write cycle time of 10ms; a write will always be completed in less than the maximum cycle time. Write cycle completion is readily determined via a simple software routine ($\overline{DATA}$ Polling) that performs a read operation while the device is in an automatic write mode. If a read command (addressed to the last byte written) is given while the IDT78C16A is still writing, the inverse of the most significant bit (I/O_7 pin) of the last byte written will be present. True data is not released until the write cycle is completed. Thus, a $\overline{DATA}$ polling monitor of the output (or periodic read of the last written byte) for true data can be used to detect early completion of a write cycle.

ENDURANCE

IDT's EEPROM technology employs the Fowler-Nordheim method of tunneling across a thin oxide. IDT78C16A EEPROMs are designed and tested for applications requiring extended endurance.

The endurance failure mechanism associated with EEPROMs results from the charge trapping in the thin tunneling dielectric. This failure is a function of the number of write cycles that each byte in the part has experienced. Trapped charges accumulate slowly with each write cycle, eventually becoming large enough to prevent reliable writing to the bit cell. Since some bits may be more sensitive than others, an endurance failure is typically a single bit failure (i.e. a failure of a single bit to properly write or retain data).

To test for endurance, sample devices are written 10,000 times at every byte location and checked for data retention capability. IDT's tests ensure that shipped devices will write a minimum of 10,000 times (at every byte location) with a maximum failure rate of 1%. This means that up to 1% of a sample of devices will fail to write or retain data after being written to 10,000 times. Those devices that do fail typically have a single bit(s) that fails to retain data after being written.

For more detailed information please refer to the *IDT Reliability Report on Endurance*.

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ABSOLUTE MAXIMUM RATINGS (1)

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +150	°C
P_T	Power Dissipation	1.0	1.0	W
I_{OUT}	DC Output Current	50	50	mA

NOTE:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ENDURANCE

PARAMETER	VALUE	UNIT
Minimum Endurance	10,000	Cycles/Byte

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

GRADE	AMBIENT TEMPERATURE	GND	V_{CC}
Military	-55°C to +125°C	0V	5.0V ± 10%
Commercial	0°C to +70°C	0V	5.0V ± 10%

RECOMMENDED DC OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
V_{IH}	Input High Voltage	2.2	3.5	6.0	V
V_{IL}	Input Low Voltage	-0.3	0.4	0.8	V
V_{WI}	Write Inhibit	3.8	–	–	V

CAPACITANCE (T_A = +25°C, f = 1.0MHz, V_{CC} = 5.0V)

SYMBOL	PARAMETER(1)	CONDITIONS	TYP.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	pF

NOTE:

1. This parameter is sampled and not 100% tested.

DC ELECTRICAL CHARACTERISTICS

Following Conditions Apply Unless Otherwise Specified

T_A = 0°C to +70°C — V_{CC} = 5.0V ± 10% (Commercial)
T_A = -55°C to +125°C — V_{CC} = 5.0V ± 10% (Military)
V_{LC} = 0.2V — V_{HC} = V_{CC} -0.2V
C_L = 30pF

SYMBOL	PARAMETER	TEST CONDITIONS	MIN.	MAX.	UNIT
$\|I_{LI}\|$	Input Leakage Current	V_{CC} = Max., V_{IN} = GND to V_{CC}	–	10	µA
$\|I_{LO}\|$	Output Leakage Current	$\overline{CE}$ = V_{IH} or $\overline{OE}$ = V_{IH}, $V_{I/O}$ = GND to V_{CC}	–	10	µA
I_{CC1}	Operating Power Supply Current V_{CC} = Max., f = 0	$\overline{CE}$ = V_{IL}, $I_{I/O}$ = 0mA	–	125	mA
I_{CC2}	Dynamic Operating Current V_{CC} = Max., f = f_{MAX}	$\overline{CE}$ = V_{IL}, $I_{I/O}$ = 0mA	–	125	mA
I_{SB}	Standby Power Supply Current (TTL Level)	$\overline{CE}$ ≥ V_{IH}, V_{CC} = Max., $I_{I/O}$ = 0mA, V_{IN} ≥ V_{IH} or 0 ≤ V_{IN} ≤ V_{IL}	–	20	mA
I_{SB1}	Full Standby Power Supply Current (CMOS Level)	$\overline{CE}$ ≥ V_{HC}, V_{CC} = Max., $I_{I/O}$ = 0mA, V_{IN} ≥ V_{CC} -0.2V or 0 ≤ V_{IN} ≤ 0.2V	–	0.9	mA
V_{OL}	Output Low Voltage	V_{CC} = Min., I_{OL} = 8mA	–	0.4	V
V_{OH}	Output High Voltage	V_{CC} = Min., I_{OH} = -2mA	2.4	–	V

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AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0V ±10%, C_L = 30pF, 0°C to +70°C)

SYMBOL	PARAMETER	COMMERCIAL 0°C to +70°C										UNIT
		78C16A70		78C16A90/100		78C16A120		78C16A150		78C16A200		
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
READ CYCLE												
t_{CE}	Chip Enable Access Time	–	70	–	90/100	–	120	–	150	–	200	ns
t_{AA}	Address Access Time	–	70	–	90/100	–	120	–	150	–	200	ns
t_{OE}	Output Enable to Output Valid	–	50	–	60/65	–	70	–	70	–	70	ns
t_{CLZ}	Chip Enable to Output in Low Z[1]	5	–	5	–	5	–	5	–	5	–	ns
t_{OLZ}	Output Enable to Output in Low Z[1]	5	–	5	–	5	–	5	–	5	–	ns
t_{CHZ}	Chip Disable to Output in High Z[1]	0	20	0	20	0	20	0	20	0	20	ns
t_{OHZ}	Output Disable to Output in High Z[1]	0	20	0	20	0	20	0	20	0	20	ns
t_{OH}	Output Hold from Address Change	5	–	5	–	5	–	5	–	5	–	ns

NOTE:
1. This parameter is guaranteed but not tested.

AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0V ±10%, C_L = 30pF, -55°C to +125°C)

SYMBOL	PARAMETER	MILITARY -55°C to +125°C										UNIT
		78C16A75		78C16A90/100		78C16A120/150		78C16A200/250		78C16A300/350		
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
READ CYCLE												
t_{CE}	Chip Enable Access Time	–	75	–	90/100	–	120/150	–	200/250	–	300/350	ns
t_{AA}	Address Access Time	–	75	–	90/100	–	120/50	–	200/250	–	300/350	ns
t_{OE}	Output Enable to Output Valid	–	50	–	60/65	–	70	–	70	–	70	ns
t_{CLZ}	Chip Enable to Output in Low Z[1]	5	–	5	–	5	–	5	–	5	–	ns
t_{OLZ}	Output Enable to Output in Low Z[1]	5	–	5	–	5	–	5	–	5	–	ns
t_{CHZ}	Chip Disable to Output in High Z[1]	0	30	0	30	0	30	0	30	0	30	ns
t_{OHZ}	Output Disable to Output in High Z[1]	0	30	0	30	0	30	0	30	0	30	ns
t_{OH}	Output Hold from Address Change	5	–	5	–	5	–	5	–	5	–	ns

NOTE:
1. This parameter is guaranteed but not tested.

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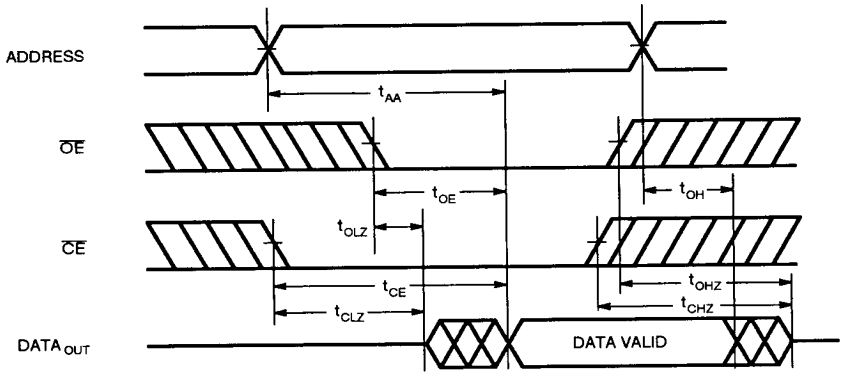
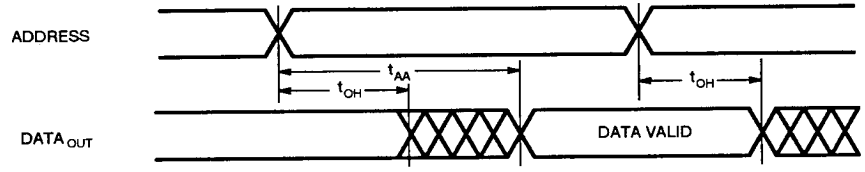
TIMING WAVEFORM OF READ CYCLE NO. 1[1]



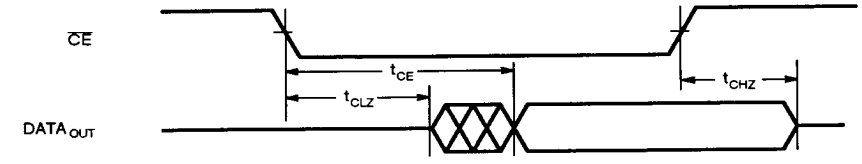
NOTE:
1. $\overline{WE}$ is HIGH for Read Cycle.

TIMING WAVEFORM OF READ CYCLE NO. 2[1]



NOTE:
1. $\overline{WE}$ is HIGH; $\overline{CE}$ = V_{IL}; $\overline{OE}$ = V_{IL}

TIMING WAVEFORM OF READ CYCLE NO. 3[1]



NOTE:
1. $\overline{WE}$ is HIGH; $\overline{OE}$ = V_{IL}; address valid prior to or coincident with $\overline{CE}$ transition LOW.

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AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0V ±10%, All Temperature Ranges; C_L = 30pF)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
WRITE CYCLE				
t_{AS}	Address Set-up Time	5	–	ns
t_{AH}	Address Hold Time	50	–	ns
t_{DS}	Data Set-up Time	20	–	ns
t_{DH}	Data Hold from Write Time	15	–	ns
t_{OES}	Output Enable Set-up Time	5	–	ns
t_{OEH}	Chip Enable Hold from Write Time	15	–	ns
t_{CES}	Chip Enable Set-up Time		–	ns
t_{CEH}	Chip Enable Hold Time	0	–	ns
t_{WP}	Write Pulse Width		–	ns
t_{WB}	Byte Write Cycle	–	10	ms
t_{DBV}	$\overline{DATA}$ Polling to $\overline{DATA}$ Valid		t_{OE}	
t_{WH}	Write Hold Time	15	–	ns
t_{DP}	End of Write Pulse to $\overline{DATA}$ Polling	15	–	ns
t_{WES}	Write Enable Set-up Time	0	–	ns
t_{WEH}	Write Enable Hold Time	0	–	ns
t_{DV}	Data Valid Time (1, 2)	–	1	µs

NOTES:
1. Data must be valid within 1µs maximum and must remain valid if t_{WP} is longer th µs.
2. This parameter is guaranteed but not tested

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V

"DISCONTINUED"

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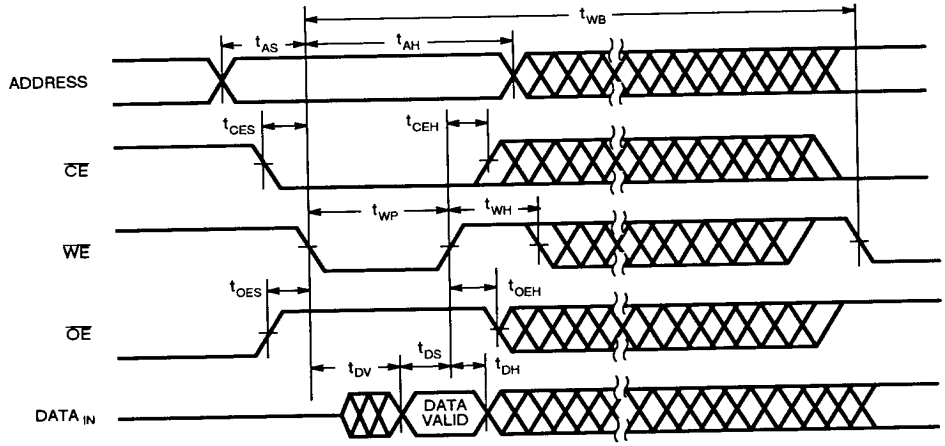
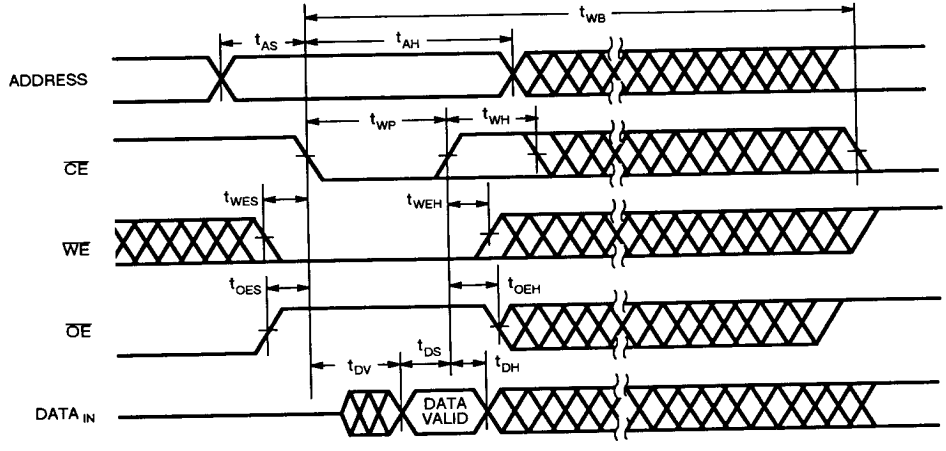
TIMING WAVEFORM OF WRITE CYCLE NO. 1, $\overline{WE}$ CONTROLLED



TIMING WAVEFORM OF WRITE CYCLE NO. 2, $\overline{CE}$ CONTROLLED



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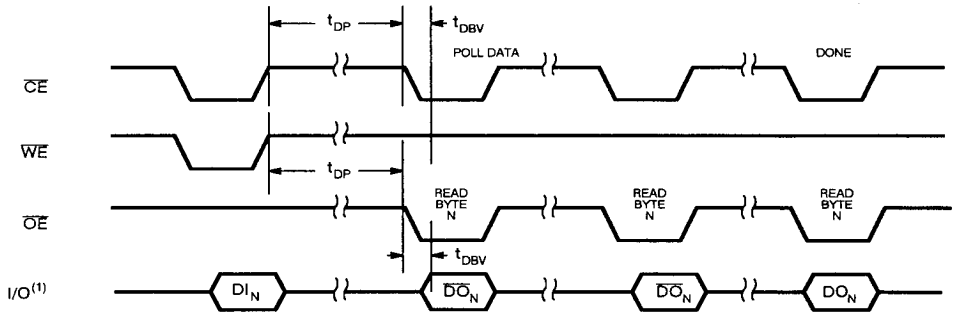
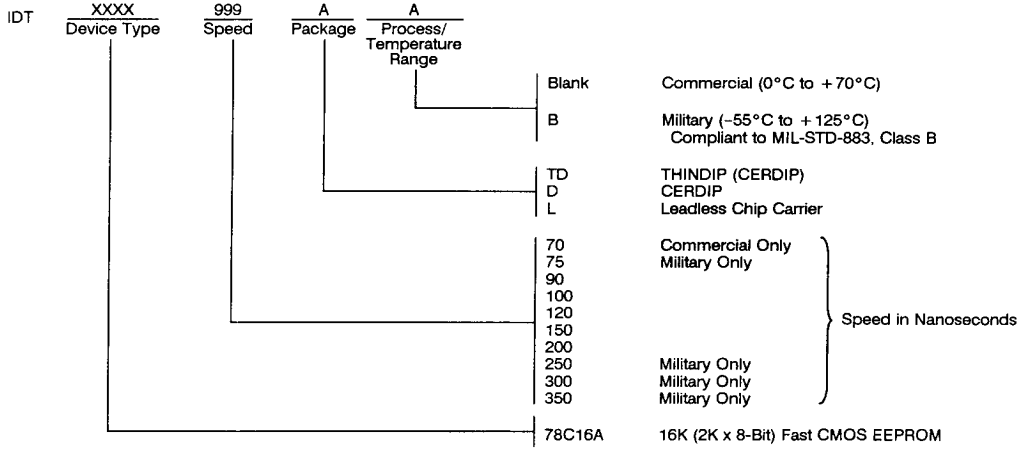
$\overline{\text{DATA}}$ POLLING



NOTE:
1. Most significant bit of the byte being written is inverted and available at I/O_7 if a Read command is issued. All other outputs are high impedance at this time. True data will not be released until the Write cycle is completed.

ORDERING INFORMATION



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