MP7643

4-Channel High-Speed Non-Inverting 15 MHz Input Bandwidth 8-Bit DACs with Output Buffers and Parallel Digital Data Port

Micro Power Systems

FEATURES

- **4 Independent 2-Quadrant Multiplying 8-Bit DACs with Output Amplifiers**
- **Dual Positive (+10 V and +5 V) Supplies or Dual (±5 V) Supplies Capability**
- **High Speed:**
  - **12.5 MHz Digital Clock Rate**
  - **V_{REF} to V_{OUT} Settling Time: 150ns to 8-bit (typ)**
  - **Voltage Reference Input Bandwidth: 15 MHz**
- **Very Low Noise Gain Control**
- **Low Power: 80mW**
- **Low AC Voltage Reference Feedthrough**
- **Excellent Channel-to-Channel Isolation**
- **DNL = ±0.5 LSB, INL = ±1 LSB (typ)**
- **DACs Matched to ±0.5% (typ)**
- **Low Harmonic Distortion: 0.25% typical with V_{REF} = 1 V p-p @ 1 MHz**
- **TTL/CMOS Compatible**
- **Latch-Up Free**
- **ESD Protection: 2000 V Minimum**
- **PDIP, SOIC & PLCC Packages Available**

APPLICATIONS

- **Direct High-Frequency Automatic Gain Control**
- **Video AGC & CCD Level AGC**
- **Convergence Adjustment for High-Resolution Monitors (Workstations)**
- **Multiplier Replacement**

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GENERAL DESCRIPTION

The MP7643 is ideal for digital gain control of high frequency analog signals such as video, composite video and CCD. The device includes 4-channels of high speed, high bandwidth, two quadrant multiplying, 8-bit accurate digital-to-analog converter. It includes an output drive buffer per channel capable of driving a ±1mA (typ) to a load. DNL of better than ±0.5 LSB is achieved with a channel-to-channel matching of typically 0.5%. Stability, matching, and precision of the DACs are achieved by using MPS' thin film technology. Excellent channel-to-channel isolation is also achieved with MPS' BiCMOS process which cannot be achieved using a typical CMOS technology.

An open loop architecture (patent pending) provides wide small signal bandwidth from V_{REF} to output up to 15 MHz (typ), fast output settling time of 150 ns, and excellent V_{REF} feedthrough isolation. In addition, low distortion in the order of 0.25% with a 1 V p-p, 1 MHz signal is achieved.

The combination of a constant input Z and the ability to vary V_{REFN} within V_{CC} –1.8 V to V_{EE} +1.5 V allows flexibility for optimum system design.

The MP7643 is fabricated on a junction isolated, high speed BiCMOS (BiCMOS IV™) process with thin film resistors. This process enables precision high speed analog/digital (mixed-mode) circuits to be fabricated on the same chip.

This device is latch-up free, and all inputs are protected to a minimum of 2000 V for ESD protection per MIL-STD-883.

Specified for operation over the commercial / industrial (–40 to +85°C) temperature range, the MP7643 is available in Plastic dual-in-line (PDIP), Surface Mount (SOIC), and Plastic leaded chip carrier (PLCC) packages.

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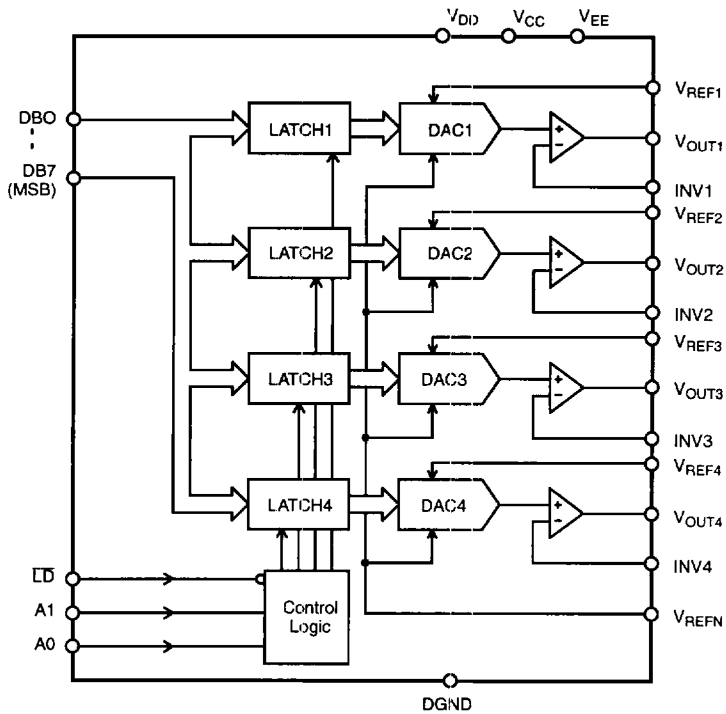
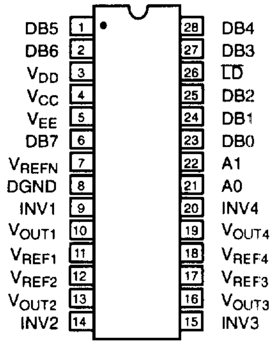
SIMPLIFIED BLOCK DIAGRAM



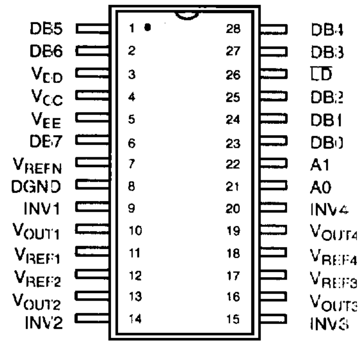
ORDERING INFORMATION

Package Type	Temperature Range	Part No.	INL (LSB)	DNL (LSB)	Gain Error (% FSR)
SOIC	–40 to +85°C	MP7643AS	±1	±0.5	±1.5
Plastic Dip	–40 to +85°C	MP7643AN	±1	±0.5	±1.5
PLCC	–40 to +85°C	MP7643AP	±1	±0.5	±1.5

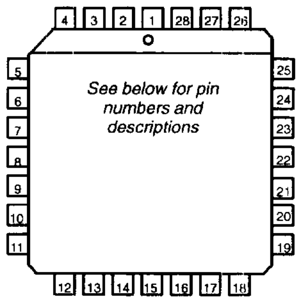
PIN CONFIGURATIONS



28 Pin PDIP (0.300")
NN28



28 Pin SOIC (EIAJ, 0.335")
R28



28 Pin PLCC
P28

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PIN OUT DEFINITIONS

PIN NO.	NAME	DESCRIPTION	PIN NO.	NAME	DESCRIPTION
1	DB5	Data Input Bit 5	15	INV3	Inverting Input 3
2	DB6	Data Input Bit 6	16	V_{OUT3}	DAC 3 Output
3	V_{DD}	Digital Positive Supply	17	V_{REF3}	DAC 3 Positive Reference Input
4	V_{CC}	Analog Positive Supply	18	V_{REF4}	DAC 4 Positive Reference Input
5	V_{EE}	Analog Negative Supply	19	V_{OUT4}	DAC 4 Output
6	DB7	Data Input Bit 7	20	INV4	Inverting Input 4
7	V_{REFN}	Negative Reference Input	21	A0	DAC Address Bit 0
8	DGND	Digital Ground	22	A1	DAC Address Bit 1
9	INV1	Inverting Input 1	23	DB0	Data Input Bit 0
10	V_{OUT1}	DAC 1 Output	24	DB1	Data Input Bit 1
11	V_{REF1}	DAC 1 Positive Reference Input	25	DB2	Data Input Bit 2
12	V_{REF2}	DAC 2 Positive Reference Input	26	$\overline{LD}$	Load Data to Selected DAC
13	V_{OUT2}	DAC 2 Output	27	DB3	Data Input Bit 3
14	INV2	Inverting Input 2	28	DB4	Data Input Bit 4

Planned

ELECTRICAL CHARACTERISTICS TABLE FOR DUAL SUPPLIES

Unless Otherwise Noted: V_{DD} = 5 V, V_{CC} = +5 V, V_{EE} = –5 V, V_{REF} = 3 V and –3 V, T = 25°C, Output Load = No Resistive Load, V_{REFN} = DGND = 0 V

Parameter	Symbol	25°C Min	25°C Typ	25°C Max	Tmin to Tmax Min	Tmin to Tmax Max	Units	Test Conditions/Comments
DC CHARACTERISTICS								
Resolution (All Grades)	N	8					Bits	
Differential Non-Linearity	DNL		±0.5				LSB	
Integral Non-Linearity	INL		±1				LSB	
Monotonicity			Guaranteed					
Gain Error	GE		±1.5				% FSR	FSR = Full Scale Range (1)
Zero Scale Offset	Z_{OFS}		±20				mV	
Output Drive Capability	I_O		±1				mA	
REFERENCE/INV INPUTS								
Impedance of V_{REF}	REF	4	6	8			kΩ	
Voltage Range	V_{RR} Pos.		V_{CC} –1.8				V	V_{REF} Max Swing is
	V_{RR} Neg.		V_{EE} +1.5				V	V_{REFN} ±3 V
INV DC Voltage Range	V_{RR} Pos.		V_O				V	
	V_{RR} Neg.		V_{EE} +1				V	
DYNAMIC CHARACTERISTICS (2)								R_L = 5 k, C_L = 20 pF
Input to Output Bandwidth			15				MHz	V_R = 1.6 V p-p, R_L = 5k to V_{EE}
Input to Output Settling Time (5)			150				ns	V_R = 1.6 V p-p, R_L = 5k to V_{EE}
Small Signal Voltage Reference Input to Output Bandwidth	ft_r		15				MHz	V_{OUT}=50mV p-p above code 16
Small Signal Voltage Reference Input to Output Bandwidth	ft_r		15				MHz	V_{OUT}=50mV p-p for all codes
Voltage Settling from V_{REF} to V_{DAC} Out	t_{sr}		300				ns	V_R=0 to V_R = 3V Step (6) to 1 LSB
Voltage Settling from Digital Code to V_{DAC} Out	t_{sd}		300				ns	ZS to FS to 1 LSB
V_{REF} Feedthrough	F_{DT}		TBD				dB	Codes=0 @ 1 MHz
Group Delay	GD		TBD				ns	
Harmonic Distortion	T_{HD}		TBD				%	V_{REF}=1MHz Sine 3V p-p
Channel-to-Channel Crosstalk	C_T		TBD				dB	@ 1 MHz, single channel
Digital Feedthrough	Q		TBD				nVS	CLK to V_{OUT}
Power Supply Rejection Ratio	PSRR		TBD				%/%	ΔV=±5%
POWER CONSUMPTION								
Positive Supply Current	I_{CC}		8				mA	V_{REF} = 0 V
Negative Supply Current	I_{EE}		8				mA	V_{REF} = 0 V
Power Dissipation	P_{DISS}		80				mW	V_{REF} = 0 V, Codes = all 1
DIGITAL INPUT CHACTERISTICS								
Logic High (3)	V_{IH}	2.4					V	
Logic Low (3)	V_{IL}			0.8			V	
Input Current	I_L			±10			µA	
Input Capacitance (2)	C_L		8				pF	

ELECTRICAL CHARACTERISTICS TABLE

Description	Symbol	25°C Min	25°C Typ	25°C Max	Tmin to Tmax Min	Tmin to Tmax Max	Units	Conditions
DIGITAL TIMING SPECIFICATIONS (2, 4)								
Address to $\overline{LD}$ Setup	t_{AS}		70				ns	
Address to $\overline{LD}$ Hold	t_{AH}		0				ns	
Data to $\overline{LD}$ Setup	t_{DS}		70				ns	
Data to $\overline{LD}$ Hold	t_{DH}		0				ns	
$\overline{LD}$ Pulse Width	t_{LD}		70				ns	
$\overline{PRESET}$ Pulse Width	t_{PR}		60				ns	

NOTES

(1) Full Scale Range (FSR) is 3V.
(2) Guaranteed but not production tested.
(3) Digital input levels should not go below ground or exceed the positive supply voltage, otherwise damage may occur.
(4) *See Figure 1.*
(5) For reference input pulse: $t_R = t_F \geq 100$ ns.

Specifications are subject to change without notice

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ABSOLUTE MAXIMUM RATINGS (1, 2) (TA = +25°C unless otherwise noted)

V_{CC} to V_{REFN} .... +6.5 V
V_{EE} to V_{REFN} .... –6.5 V
V_{CC} to DGND .... +13.0 V
V_{EE} to DGND .... –6.5 V
V_{REF} 1-4 to DGND, V_{REFN} .... V_{CC} to V_{EE}
V_{OUT} 1-4 to DGND, V_{REFN} .... V_{CC} to V_{EE}
Digital Input & Output Voltage to DGND –0.5 to V_{DD} +0.5 V

Operating Temperature Range
Extended Industrial .... -40°C to +85°C
Maximum Junction Temperature .... -65°C to 150°C
Storage Temperature .... 150°C
Lead Temperature (Soldering, 10 sec) .... +300°C
Package Power Dissipation Rating @ 75°C
PDIP, SOIC, PLCC 1050mW
Derates above 75°C .... 14mW/°C

NOTES:

(1) Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation at or above this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.
(2) Any input pin which can see a value outside the absolute maximum ratings should be protected by Schottky diode clamps (HP5082-2835) from input pin to the supplies. *All inputs have protection diodes* which will protect the device from short transients outside the supplies of less than 100mA for less than 100μs.

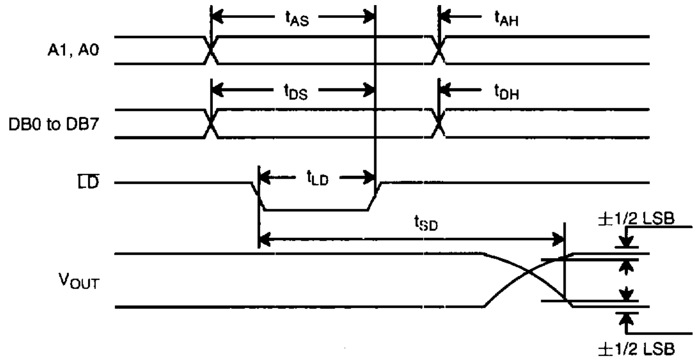

Figure 1. Timing Diagram

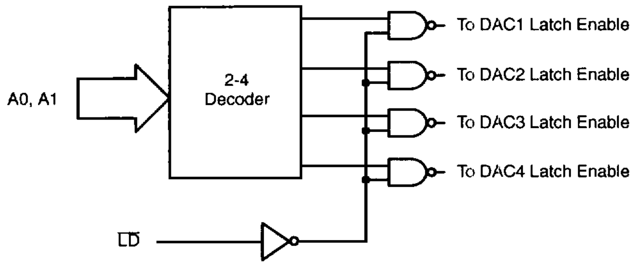

Figure 2. Input Control Logic (Simplified) Block Diagram

$\overline{LD}$	A1	A0	Operation
L	L	L	DAC1 Transparent
↑	L	L	DAC1 Latched
L	L	H	DAC2 Transparent
↑	L	H	DAC2 Latched
L	H	L	DAC3 Transparent
↑	H	L	DAC3 Latched
L	H	H	DAC4 Transparent
↑	H	H	DAC4 Latched
H	X	X	No Operation

Table 1. Truth Table

D7 MSB	D6	D5	D4	D3	D2	D1	D0 LSB	DAC Output Voltage $V_{OI} = V_{REFN} + (V_{RI} - AGND)\left(\frac{D}{256}\right)$
0	0	0	0	0	0	0	0	V_{REFN}
0	0	0	0	0	0	0	1	$(V_{RI} - V_{REFN})\left(\frac{1}{256}\right) + V_{REFN}$
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
1	1	1	1	1	1	1	0	$(V_{RI} - V_{REFN})\left(\frac{254}{256}\right) + V_{REFN}$
1	1	1	1	1	1	1	1	$(V_{RI} - V_{REFN})\left(\frac{255}{256}\right) + V_{REFN}$

Table 2. DAC Transfer Function
Analog Output vs. Digital Code (With V_{REF} Shorted to INV)

THEORY OF OPERATION

The MP7643 is a 4-channel multiplying D/A converter that incorporates a novel open loop architecture invented by MPS. The design produces the wider bandwidth, faster settling time, more constant group delay, and a lower noise operation compared to the conventional R-2R based architectures. This device is particularly useful in applications where multipliers are used to perform the gain adjustment function for high frequency analog signal conditioning. Multipliers produce higher noise and offset for low gain operation. This design allows for digital control of gain with constant and very low noise from the low gain through high gain ranges of operation.

Linearity Characteristics

Each DAC achieves DNL $\leq \pm 0.5$ LSB (typ), INL $\leq \pm 1$ LSB (typ), and gain error $\leq \pm 1.5\%$. Since all 4 channel D/A converters are fabricated on the same IC, the linearity matching and gain matching of $\pm 0.5\%$ (typ) is achieved.

AC and Transient Settling Characteristics

The novel subranging architecture delivers a 15 MHz (typ.) –3 dB bandwidth. With all codes = 1 and a 1.6 V step impulse at V_{REF}(1-4), the analog output settles to 8 bits of accuracy in typically 150 ns (with R_L = 5k to V_{EE}). Also with V_{REF} = 3 V or –3 V and a FS to ZS or ZS to FS code change, the respective analog output settles to 8 bits typically in 300 ns. Note that the AC performance specifications also match to within $\pm 0.5\%$ (typ.) between all 4 channels. The above AC and transient performance is achieved with each channel consuming only 20 mW (typ.) with either ± 5 V or 0 V to 10 V supplies.

Digital Interface

The MP7643 allows direct interface to most microprocessor buses without additional I/O circuitry. *Figure 1.* and *Figure 2.* describe the operation, specification and interface characteristics of the logic port.

The address bits A0 and A1 determine which D/A channel is selected. When $\overline{LD}$ input is low the respective latch of the D/A is enabled (digital input data becomes transparent to the latch and the selected DAC channel), and digital data is loaded into the selected DAC.

Power Supplies and Voltage Reference DC Voltage Ranges

For the single supply operation, V_{CC} = +10 V, V_{DD} = +5 V, and V_{EE} = GND = 0 V. The V_{OUT} 1-4 and V_{REF} 1-4 range would be V_{CC} –1.8 V (10 – 1.8 = 8.2 V) to V_{EE} +1.5 V (0 + 1.5 = 1.5 V). V_{REFN} is the equivalent of AGND for this DAC. In this mode V_{REFN} can be set at (V_{CC} + V_{EE})/2 = (10 + 0)/2 = 5 V. V_{REFN} DC range can, however, be set from V_{EE} +1.5 = 1.5 V to V_{CC} – 1.5 = 8.2 V. Refer to *Table 2.* for the relationship equations.

For the dual supply operation, V_{CC} = +5 V, V_{DD} = +5, and V_{EE} = –5 V. The V_{OUT} 1-4 and V_{REF} 1-4 range would be V_{CC} –1.8 V (5 V –1.8 = 3.2 V) to V_{EE} +1.5 V (–5 + 1.5 = –3.5 V). In this mode V_{REFN} can be set to (V_{CC} + V_{EE})/2 = (5 – 5)/2 = 0 V. However, V_{REFN} DC range can be set from V_{EE} +1.5 V = 3.5 V to V_{CC} –1.8 = +3.2 V. Refer to *Table 2.* for the relationship equations.

About the INV Input and its DC Voltage Range

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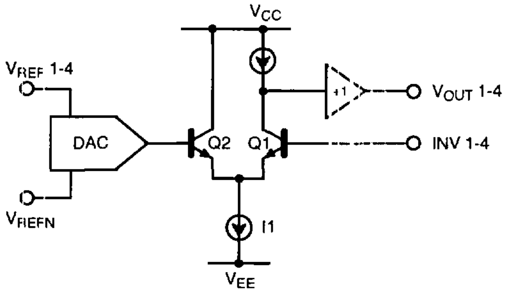

Figure 3. Simplified Block Diagram

As noted in the specification table, the max DC value of the INV input pin is V_O. *Figure 3.* shows a simplified block diagram of the internal circuitry around INV. If V_{INV} exceeds V_O, Q1 will saturate and the amp and consequently the DAC becomes non-functional.

The min DC range of INV is limited to V_{be} (Q1) and V_{CE} (sat) of I_1. Therefore, INV (min-DC) = V_{EE} +1 V.