Preliminary Data Sheet
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microelectronics group

Lucent Technologies
Bell Labs Innovations

ALA110 VHF Semicustom Linear Array

Features

- High-speed CBIC process
  10.2 GHz NPN, 4.3 GHz PNP
- Optimized for small-scale, high-performance applications
- Symmetrical layout to reduce thermal effects
- Optional thin-film (Ta_2N) resistors
- Electrically trimmable, resistor melt-back links
- Optional on-chip ESD protection
- Adjacent scaled transistors for bandgap reference biasing
- Unique epi areas to allow for independent tub biasing for high PSRR applications
- Quick design turnaround (typically 6 to 8 weeks)
- Proven reliability

Applications

- VHF operational amplifiers (650 MHz)
- Buffers/video drivers (900 MHz)
- Comparators (<1 ns)
- Track and hold amplifiers (0.01% settling in 15 ns)
- Pin electronics (2500 V/μs)
- RF amplifiers
- Analog multipliers/mixers
- Optical data link drivers/receivers (600 Mbits/s)

Description

The ALA110 Semicustom Linear Array is an integrated circuit consisting of vertical NPN and PNP transistors, programmable capacitors, implanted boron resistors, resistor melt-back links, and optional thin-film resistors. The ALA110 Linear Array is fabricated in a complementary bipolar integrated circuit (CBIC-V) process that offers the advantages of similar NPN and PNP transistor characteristics at very high speeds. Peak f_T values of 10.2 GHz for the NPN and 4.3 GHz for the PNP transistors (V_{CE} = 3 V, I_C = 4 mA for the NPN and 3 mA for the PNP) and a high-current drive capability (7.2 mA for the NPN and PNP 6X transistors) are unique to this technology.

Two levels of metallization are available for component interconnection. During layout, designers can interconnect components by drawing wiring runs on predefined layout sheets. The designer can completely customize the bottom-metal, via hole, top-metal, and STIC (thin-film resistor) levels. The bottom-metal and top-metal levels have the same low sheet resistance of 0.04 Ω/sq. and a maximum current density of 2 mA/μm of metal width. The standard 5 μm bottom-metal and 10 μm top-metal linewidths are capable of handling 10 mA and 20 mA dc current, respectively. For cases where high current capacity or low interconnect resistance is required, the standard metal linewidths can be increased.

The ALA110 Linear Array has symmetrically located components to minimize layout parasitics and temperature gradients, in addition to intentionally scaled adjacent transistors for bandgap reference biasing. The ALA110 Linear Array also has eight unique epi areas containing both resistors and PNP transistors to allow for independent tub biasing for high PSRR applications. The array has a small die area of 4.08 mm² with 16 I/Os and is optimized for the design of a single high-performance circuit. These features allow circuit implementation on this array to have the performance approaching that of a full-custom design.

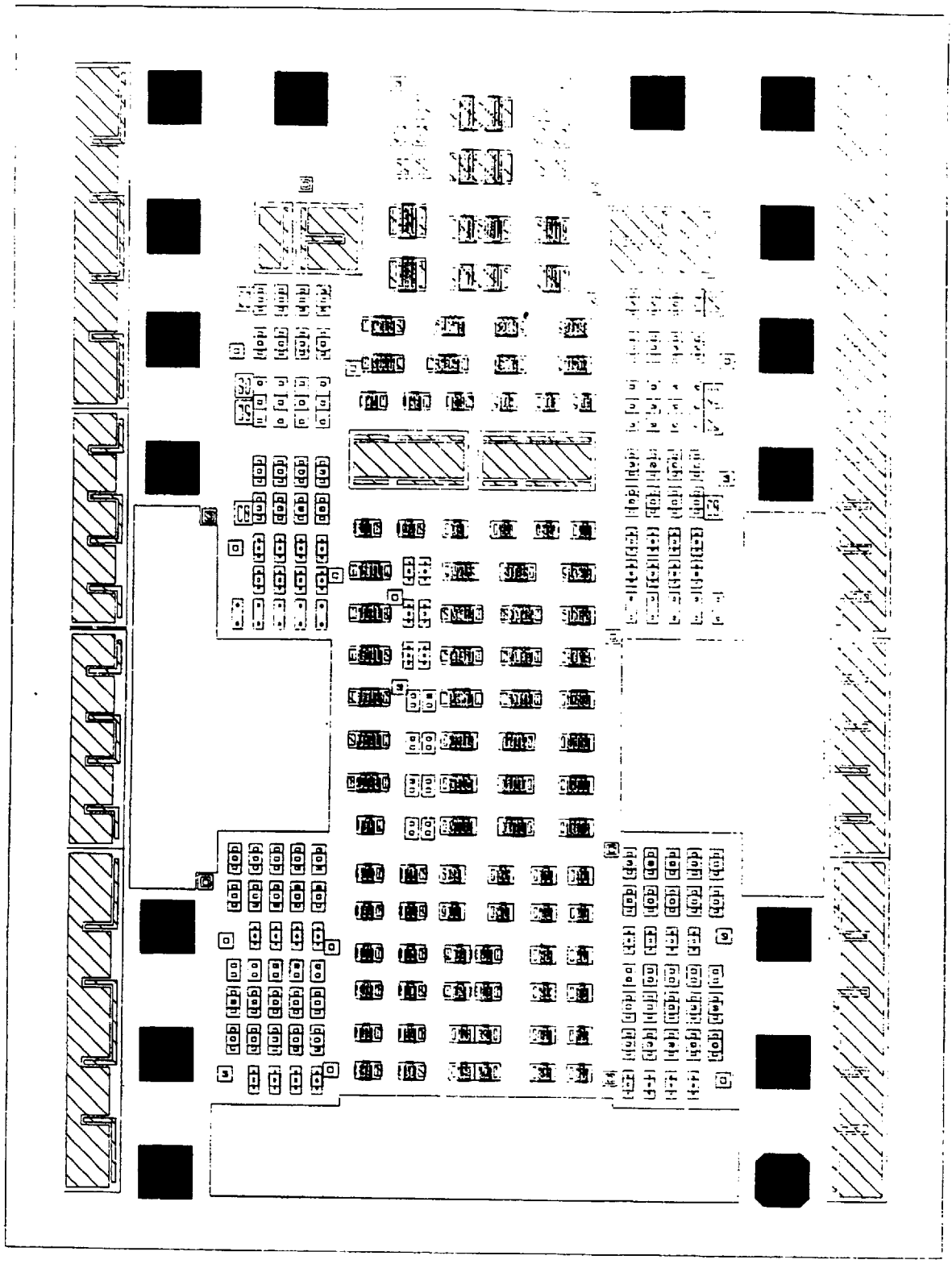


Figure 1. ALA110 Linear Array Die Layout

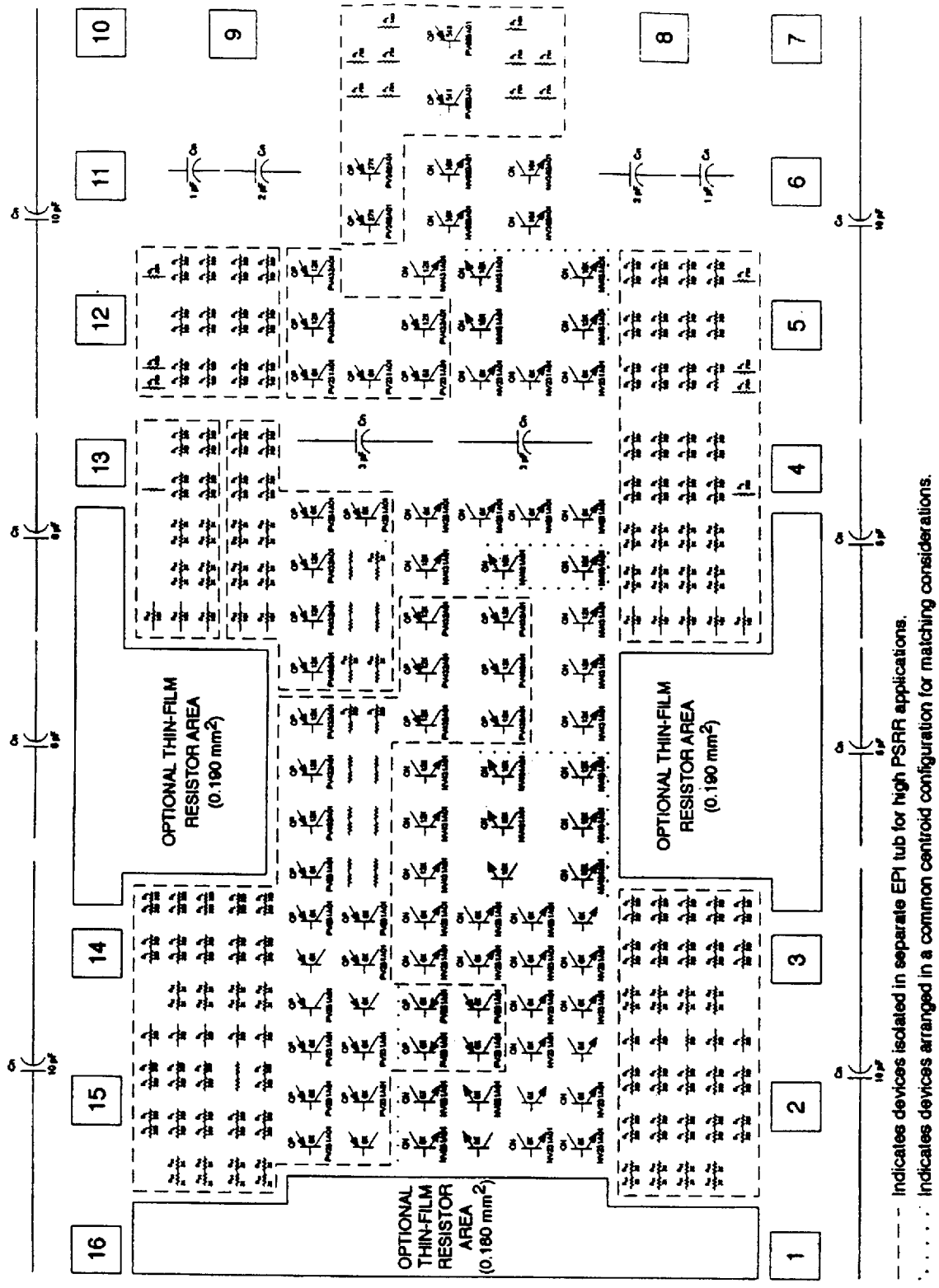


Figure 2. ALA110 Linear Array Die Schematic

Electrical Characteristics (T_A = 25 °C)

Table 1. NPN dc Parameters NV231A01 (6X)

Symbol	Measurement/Condition	Min	Typ	Max	Unit
h_{FE}*	I_C = 1 mA, V_{CB} = 2 V	50	118	—	—
f_T	I_C = 4.0 mA, V_{CE} = 3 V	8.0	10.2	—	GHz
V_A	I_C = 1 mA, V_{CE} = 2 V, 4 V	12.0	27.0	—	V
V_{CE} (sat)	I_C = 1 mA, I_B = 100 µA	—	86	180	mV
V_{BE}†	I_E = −1 mA, V_{CB} = 2 V	740	780	810	mV
BV_{CEX}	I_C = 100 µA, I_B = 0.1 µA	6.0	11.5	—	V
BV_{CBO}	I_C = 1 µA	6.0	19.0	—	V
BV_{CIO}	I_C = 1 µA	25.0	45.0	—	V
BV_{EBO}‡	I_E = 10 µA	2.0	—	—	V
BV_{EBS}‡	I_E = 1 µA	0.2	—	—	V
80% β Range	V_{CB} = 2 V	0.05	1.00	2.00	mA
80% f_T Range	V_{CE} = 3 V	1.8	4.7	7.5	mA
Max dc Current	V_{CE} = 3 V	—	—	7.2	mA
C_{JE}	V_{BE} = 0	—	0.12	—	pF
C_{JC}	V_{BC} = 0	—	0.08	—	pF
C_{JS}	V_{CS} = 0	—	0.10	—	pF
Size	—	—	—	32.5 x 47.5	(µm x µm)

Table 2. PNP dc Parameters PV231A01 (6X)

Symbol	Measurement/Condition	Min	Typ	Max	Unit
h_{FE}*	I_C = −1 mA, V_{CB} = −2 V	25	45	—	—
f_T	I_C = −3.0 mA, V_{CE} = −3 V	3.0	4.3	—	GHz
V_A	I_C = −1 mA, V_{CE} = −2 V, −4 V	6.0	11.0	—	V
V_{CE} (sat)	I_C = −1 mA, I_B = −100 µA	—	−188	−360	mV
V_{BE}†	I_E = 1 mA, V_{CB} = −2 V	−750	−792	−830	mV
BV_{CEX}	I_C = −100 µA, I_B = −0.1 µA	6.0	15.0	—	V
BV_{CBO}	I_C = −1 µA	8.0	22.0	—	V
BV_{CIO}	I_C = −1 µA	11.0	17.0	—	V
BV_{EBO}‡	I_E = −10 µA	−3.5	—	—	V
BV_{EBS}‡	I_E = −1 µA	0.1	—	—	V
80% β Range	V_{CB} = 2 V	0.04	1.00	2.00	mA
80% f_T Range	V_{CE} = 3 V	1.1	2.7	4.2	mA
Max dc Current	V_{CE} = 3 V	—	—	7.2	mA
C_{JE}	V_{BE} = 0	—	0.12	—	pF
C_{JC}	V_{BC} = 0	—	0.13	—	pF
C_{JS}	V_{CS} = 0	—	0.51	—	pF
Size	—	—	—	32.5 x 47.5	(µm x µm)

* h_{FE} matching of adjacent transistors of the same type is within ±5%.
† V_{BE} matching of adjacent transistors of the same type is within ±2.5 mV.
‡ Breakdown of the emitter-based junction will cause serious performance degradation. Precautions should be taken to avoid operation in or near breakdown.

Metallization Data

Table 3. Metallization Current Density

Metal	Min Width	Min Spacing	Thickness	Max Current Density
Bottom Metal	5 μm	5 μm	1.35 μm	2 mA/μm of Width
Top Metal	10 μm	10 μm	1.80 μm	2 mA/μm of Width
Via	—	—	—	30 mA each
Ti-Pt Link	6 μm	—	—	0.2 mA/μm of Width

Table 4. Metallization Parasitics

Parasitic	BOTMET		TOPMET		Units
	Typ	Max	Typ	Max	
Resistance	0.040	0.055	0.040	0.055	Ω/sq.
Capacitance Over epi to Silicon*	0.36	—	0.29	—	pF
Capacitance Outside epi to Silicon*	0.13	—	0.16	—	pF
Parallel Path Capacitance*	0.02	—	0.03	—	pF
Inductance*	1.30	—	1.16	—	nH
Bonding Pad Capacitance to Substrate	—	—	0.16	—	pF
Via	0.0015	—	—	—	Ω
Ti-Pt Link	—	—	3.3	4.0	Ω

* For a path 1000 μm long and 5 μm wide (BOTMET) or 10 μm wide (TOPMET).

Transistor Data (T_A = 25 °C)

Transistor Name*	Type	Emitter Stripes†	Qty	Scale	Current Range (mA)				
					80% Beta		80% fT		dc
					Min	Max	Min	Max	Max
NV231A01	NPN	2	27	6X	0.05	2.00	1.80	7.50	7.20
NV431A01	NPN	4	20	12X	0.10	4.00	3.60	15.00	14.40
NV362A01	NPN	3	2	18X	0.15	6.00	5.40	22.50	15.00‡
NV663A01	NPN	6	2	36X	0.30	12.00	10.80	45.00	30.00‡
PV231A01	PNP	2	22	6X	0.04	2.00	1.10	4.20	7.20
PV432A01	PNP	4	15	12X	0.07	4.00	2.20	8.50	14.40
PV392A01	PNP	3	2	27X	0.16	9.10	5.00	19.20	15.00‡
PV693A01	PNP	6	2	54X	0.33	18.00	9.90	38.20	30.00‡

* An explanation of the transistor name coding scheme is given on the last page of this data sheet.
† Device emitter area can be scaled by the number of emitter stripes connected. For example, the NV231A01 device can be reduced to 1/2 of its scale by connecting only one emitter stripe. Unconnected emitter stripes must be shorted to the base.
‡ Denotes maximum currents are limited by metallization.

Resistor Data (T_A = 25 °C)

Value (Ω)	Type*	Sheet Res. (Ω/sq.)	Width (μm)	Tol (%)	TCR (ppm/ °C)	Qty
25	BI	80	24	±25	+1340	16
50	BI	80	24	±20	+1340	2
200	BI	80	5	±25	+1340	154
500	BI	80	5	±25	+1340	16
2K	BI	1880	5	±25	+1769	64
10K	BI	1880	5	±25	+1769	10

* Denotes an implanted boron resistor. Matching of adjacent resistors of the same sheet resistance and width is within ±1%.

STIC Resistor Data (T_A = 25 °C)

Silicon tantalum integrated circuit (STIC) technology allows for the fabrication of both active silicon devices and trimmable resistors on the same die. The tantalum resistors have a low temperature coefficient and can be laser-trimmed by the user to achieve very high-precision circuitry. The use of this option requires one additional mask level.

Sheet resistivity: 300 Ω/sq. (−20% to +30% Tol)
TCI: −200 ppm/ °C
Max. current density: 40 μA/μm
Total available thin-film resistor area: 0.560 mm^2

Resistor Summary

Parameter	Resistor Types			Units
	RVL	RVH	STIC	
Sheet Resistance	80	1880	300	Ω/sq.
Mismatch	±1*	±1*	±1.5†	%
Voltage Coefficient	Negligible	0.4	Negligible	%/V
1st Temperature Coefficient TC1	1.340E-03	1.769E-03	−200E-06	°C^1
2nd Temperature Coefficient TC2	1.0E-06	5.638E-06	—	°C^2

* For similar size resistors located near each other.
† For untrimmed resistors of similar size located near each other.

MNOS Capacitor Data (T_A = 25 °C)

Table 5. Capacitor Totals

Type	Value (pF)	Tol (%)	Qty
Programmable	1	±25	2
Programmable	2	±25	2
Programmable	3	±25	2
Programmable	6	±25	4
Programmable	10	±25	4

Table 6. Capacitor Type Parameters

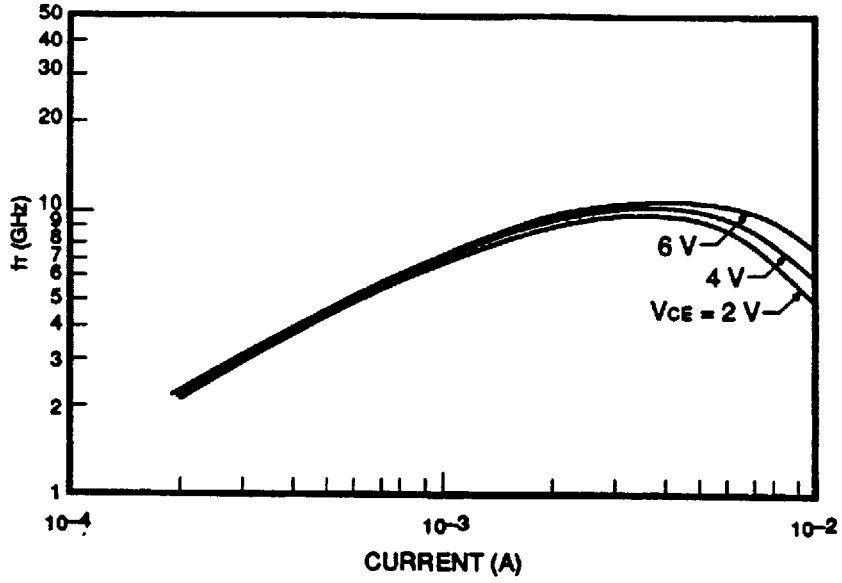
Parameter	Capacitor Types		Units
	MNOS	MOM	
Capacitance Density	2.22E-04	4.4E-05	pF/μm^2
Area/pF	4,503	22,660	μm^2/pF
Absolute Tolerance	±25	±35	%
Minimum Value	0.55	0.005	pF

Metal On Metal (MOM) Capacitors

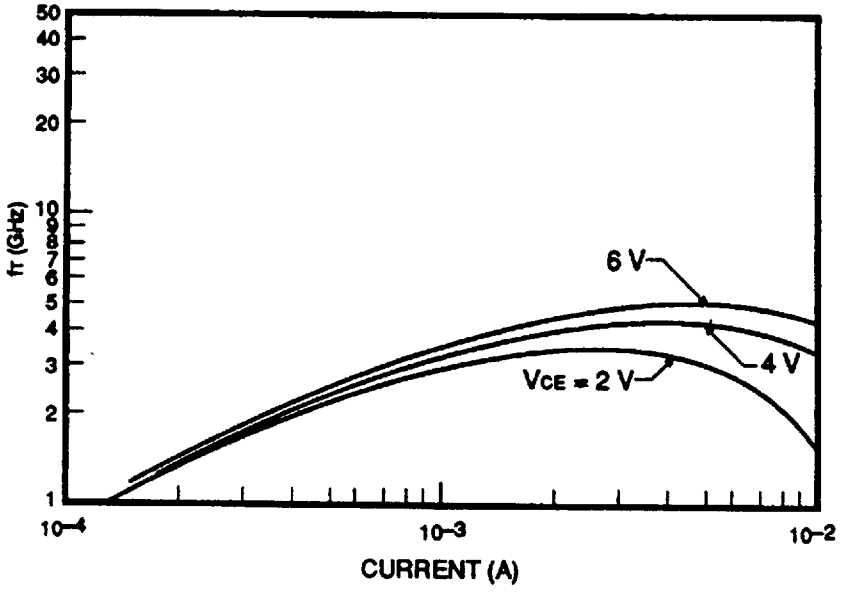
For Capacitor values less than 0.55 pF, use TOPMET to BOTMET, Metal-On-Metal (MOM) capacitors.
MOM capacitance density, 4.410E-05 pF/μm^2
MOM capacitance tolerance, ±35%
i.e., A 0.75 pF MOM capacitor would require a 100 μm X 170 μm TOPMET/BOTMET overlap area.
Locate MOM capacitors in STIC area.

Typical Device Characteristics

Unity Gain Frequency Response (NV231A01)

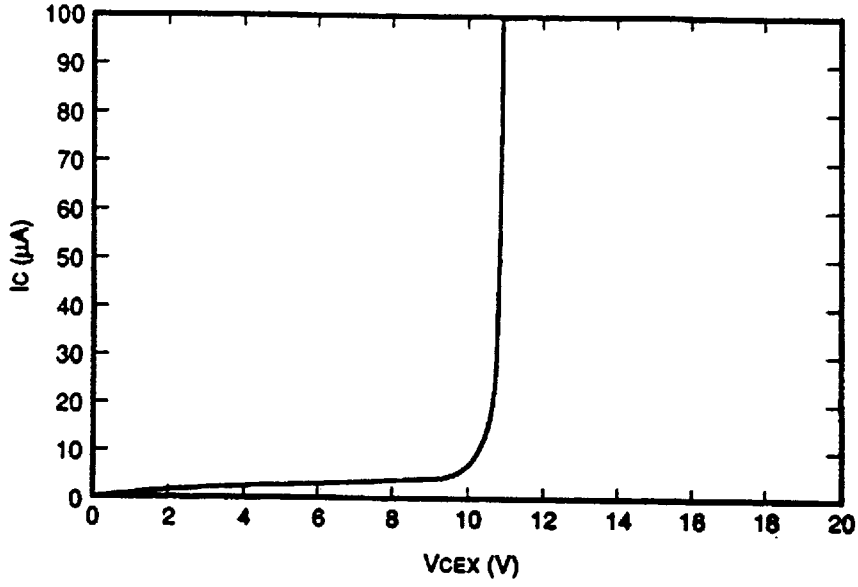


Unity Gain Frequency Response (PV231A01)

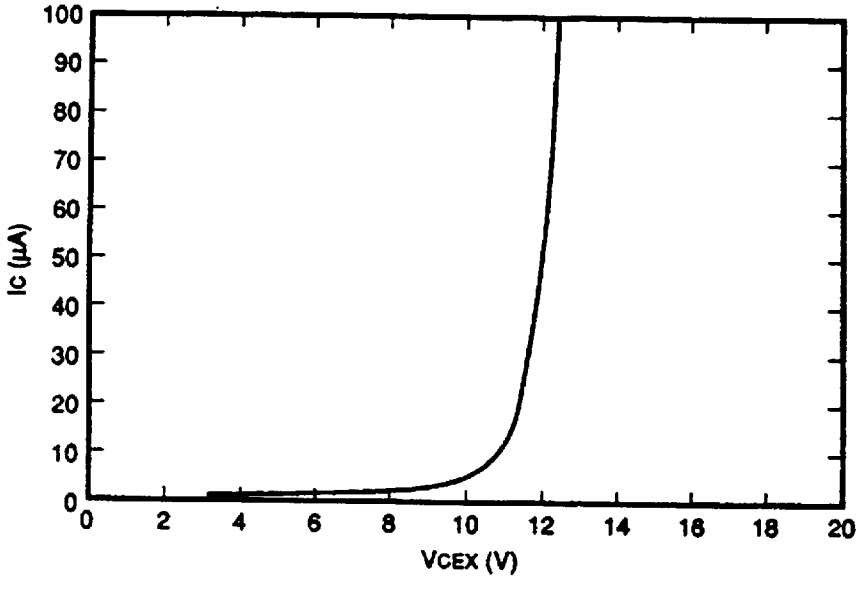


Typical Device Characteristics (continued)

Breakdown Characteristics (NV231A01)

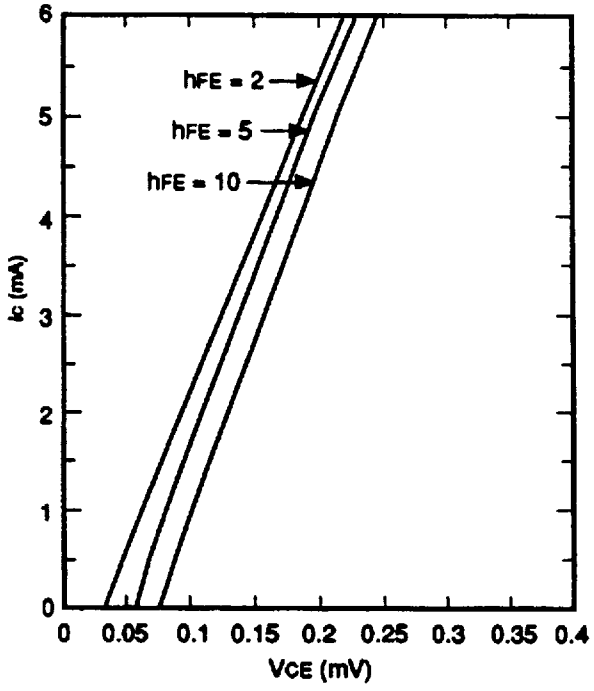


Breakdown Characteristics (PV231A01)

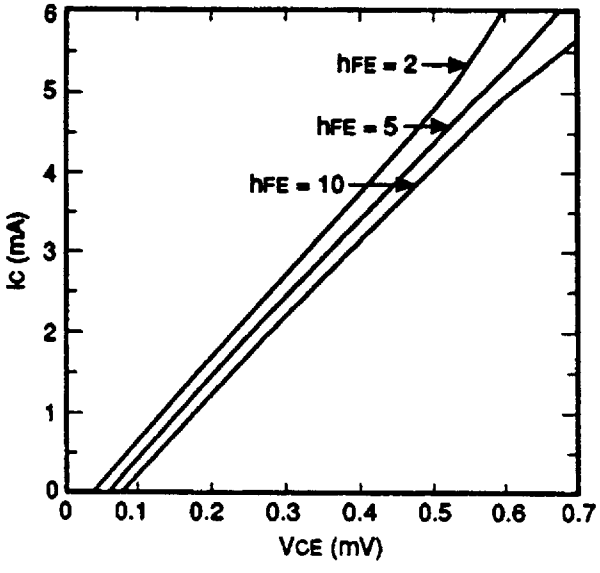


Typical Device Characteristics (continued)

Current vs. Saturation Voltage (NV231A01)

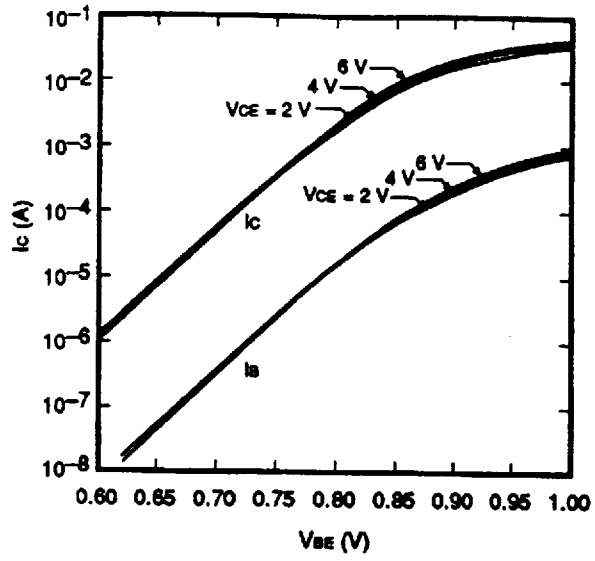


Current vs. Saturation Voltage (PV231A01)

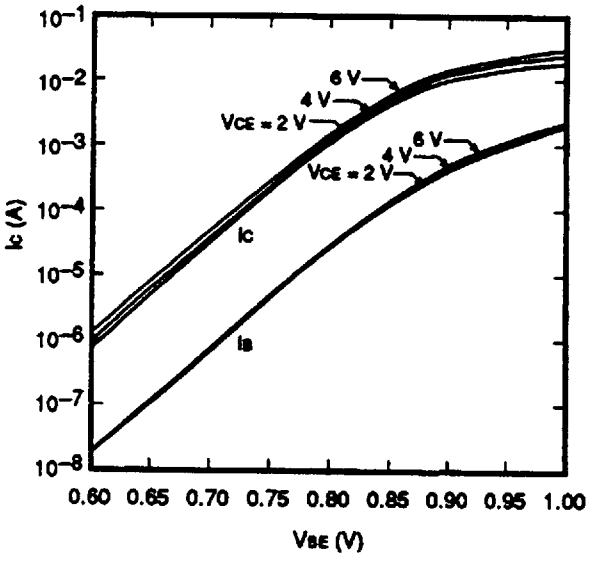


Typical Device Characteristics (continued)

Current vs. Voltage Characteristics (NV231A01)

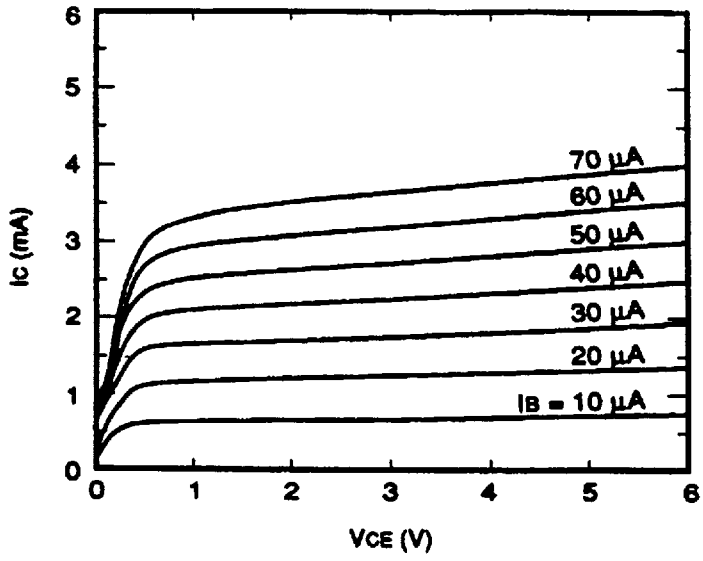


Current vs. Voltage Characteristics (PV231A01)

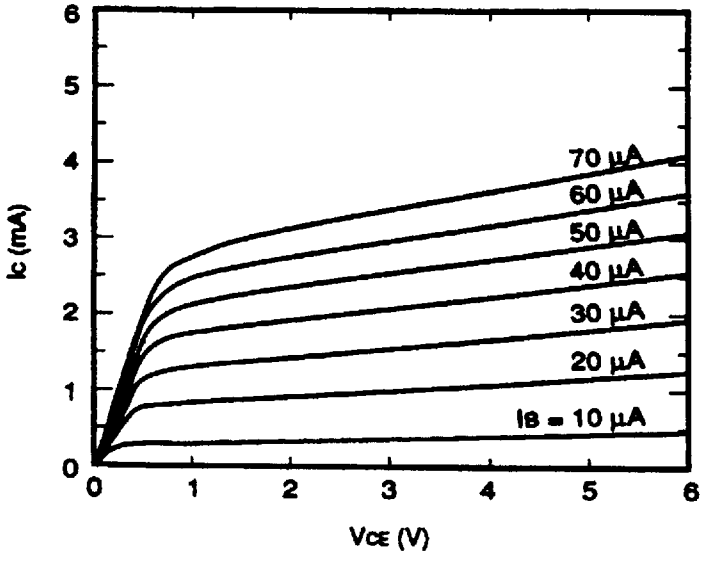


Typical Device Characteristics (continued)

Output Voltage Characteristics (NV231A01)

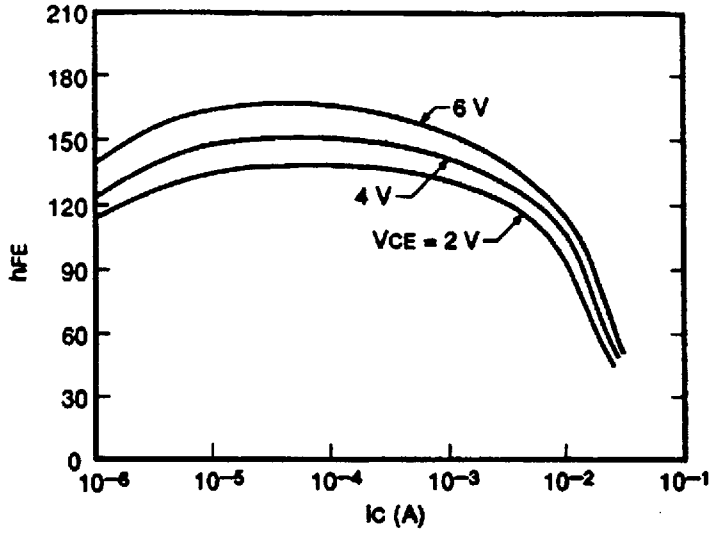


Output Voltage Characteristics (PV231A01)

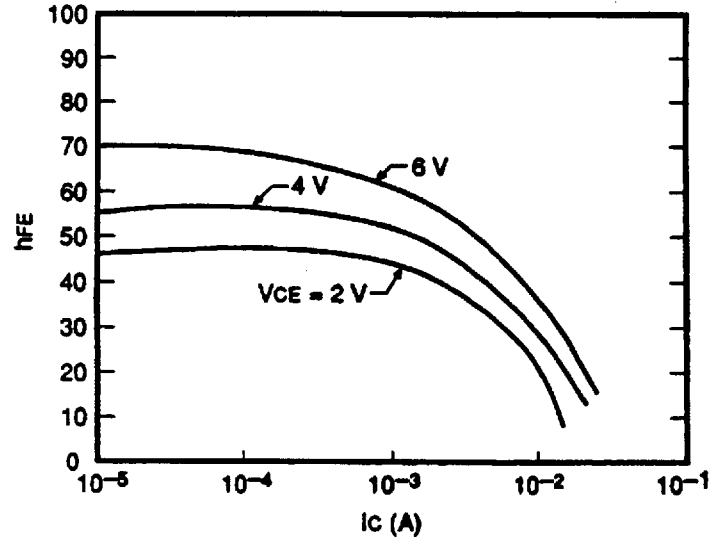


Typical Device Characteristics (continued)

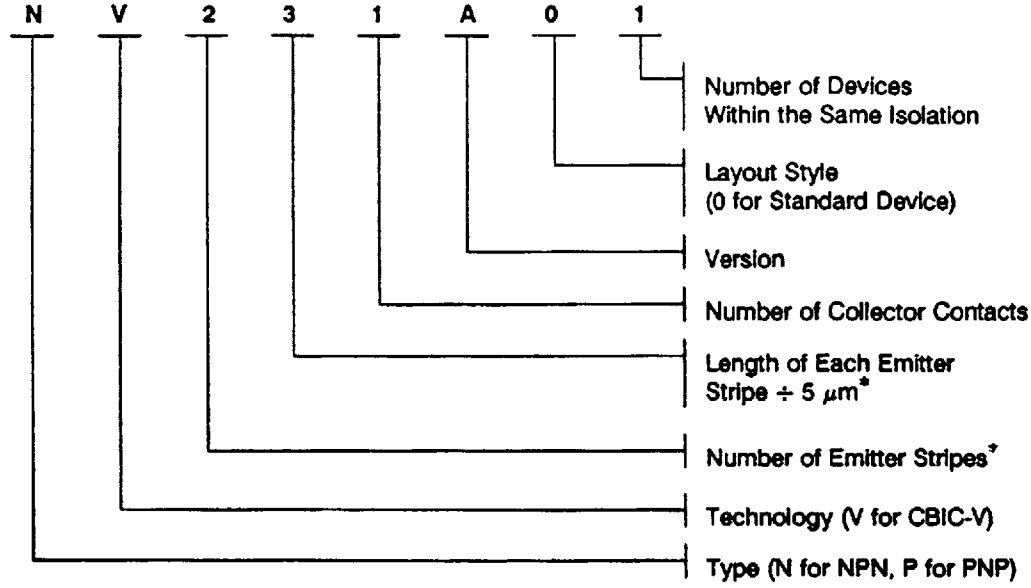
Current Gain Characteristics (NV231A01)



Current Gain Characteristics (PV231A01)



Transistor Name Coding Scheme — CBIC-V



* Integers greater than 9 are represented by alpha characters, such as A = 10, B = 11, C = 12, etc.

Examples:

PV432A01 — A PNP transistor in the CBIC-V technology with four emitter stripes, 15 μm in length, and two collector contacts. The layout architecture is one PV432A device in a single isolation.

NV663A01 — An NPN transistor in the CBIC-V technology with six emitter stripes, each stripe is 30 μm in length, and three collector contacts. The layout architecture is one NV663A device in a single isolation.