T-46.23-10 ADVANCED INFORMATION CY7C1001 CY7C1002

256K x 4 Static R/W RAM with Separate I/O

Features

- High speed
- $t_{AA} = 15 \text{ ns}$
- Transparent write (7C1001)
- CMOS for optimum speed/power
- Low active power
- --- 800 mW
- Low standby power
 250 mW
- Low data-retention power
- -- 100 µW at 2.0V
- Automatic power-down when deselected
- TTL-compatible inputs and outputs

Functional Description

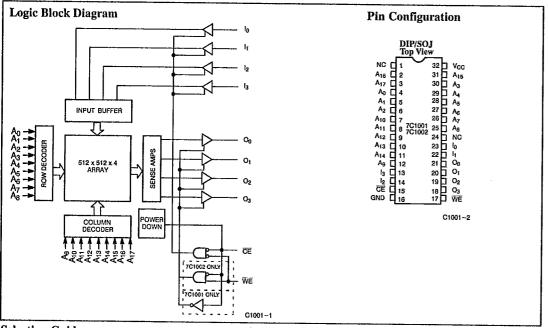
The CY7C1001 and CY7C1002 are highperformance CMOS static RAMs organized as 262,144 x 4 bits with separate I/O. Easy memory expansion is provided by active LOW chip enable ($\overline{\text{CE}}$) and three-state drivers. They have an automatic powerdown feature, reducing the power consumption by more than 65% when deselected.

Writing to the device is accomplished by taking both chip enable (\overline{CE}) and write enable (\overline{WE}) inputs LOW. Data on the four input pins (I_0 through I_3) is written into the memory location specified on the address pins (A_0 through A_{17}).

Reading the device is accomplished by taking chip enable ($\overline{\text{CE}}$) LOW while write enable ($\overline{\text{WE}}$) remains HIGH. Under these conditions, the contents of the memory location specified on the address pins will appear on the four data output pins (O_0 through O_3).

The data output pins on the CY7C1001 and the CY7C1002 are placed in a high-impedance state when the device is deselected (\overline{CE} HIGH). The CY7C1002's outputs are also placed in a high-impedance state during a write operation (\overline{CE} and \overline{WE} LOW). In a write operation on the CY7C1001, the output pins will track the inputs after a specified delay.

The CY7C1001 and CY7C1002 are available in standard 300-mil-wide DIPs and SOJs.



Selection Guide

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Maximum Access Time (ns)		15	20	25
Maximum Operating Current	Commercial	145	145	145
	Military		150	150
Maximum Standby Current (mA)	Commercial	45	45	45
	Military		50	50

Document #: 38-00200