UTOPIAFIFO™ 1 TO 4 (128 X 9 X 4) DEMULTIPLEXER-FIFO

IDT77301

Features:

- Data transfers on fixed cell sizes
- Programmable cell size
- One input port to four output ports
- Four Independent output 128 x 9 FIFO Queues
- Selectable eighteen bit or nine bit input bus
- Selectable eight/nine bit or four bit output buses
- Programmable chip Identification
- "UtopiaTx" level 2 compliant input interface signaling
- "UtopiaTx" level 1 compliant output interface signaling
- Separate clocks for input and output
- Selectable In-band or Out-band routing
- Multicast capability
- Data clock rates to 62.5 MHz, 10ns access time
- Building Block Implementation allows up to 32 output channels with a 18, 36 or 64-bit input bus
- Four 562 Mbps output channels can be derived from a single 1.1256 Gbps input channel with no additional glue logic
- 100-pin TQPF package

General Description

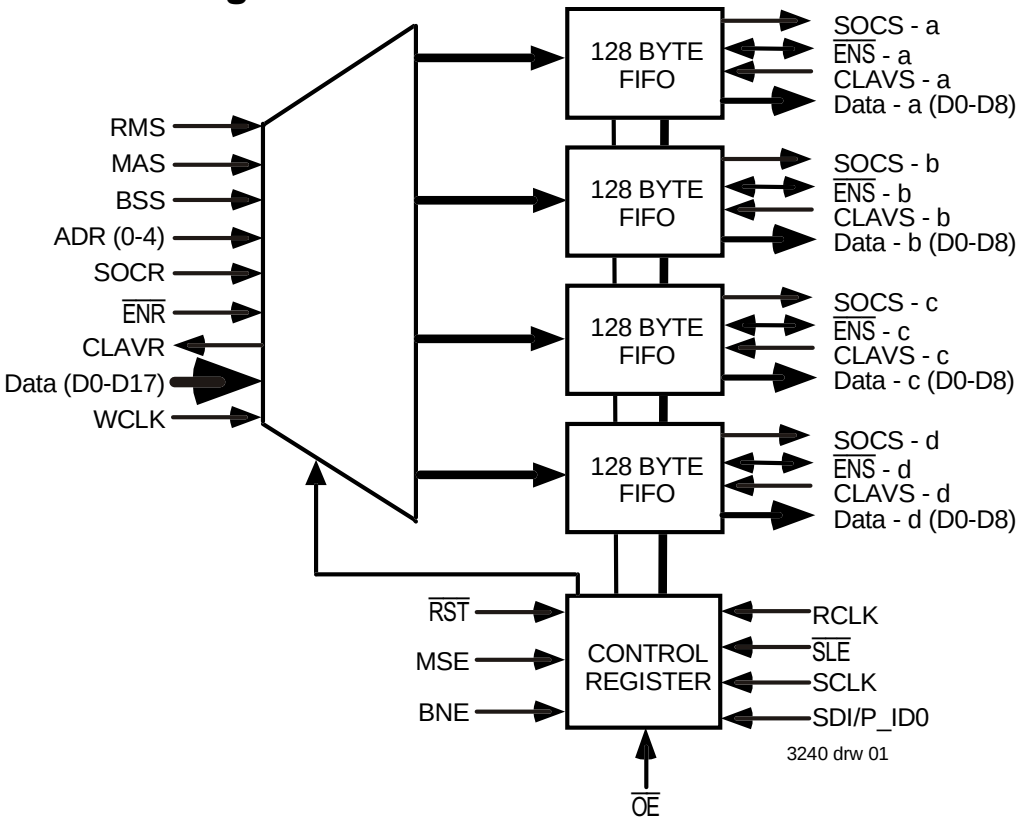
The IDT77301 UtopiaFIFO is a high-speed, low power single input port supplying four demultiplexing FIFO output ports. Each of the four output synchronous (clocked) FIFOs are 64 words (128 bytes) in depth. Data is written to the input port in "cells" (fixed length data packets). The cell size is programmable from 16 bytes to 128 bytes.

The input port can be configured to support 9-bit or 18-bit wide data buses. (Multiple 77301's can be configured to handle 32 and 64-bit buses with no additional logic.)

There are four routing methods that can be used to transfer data to the 77301. Two methods use out-band routing for the port selection, which requires use of the Address Location bus. The remaining two methods support in-band routing, which uses the Address Location bus in conjunction with the Data bus for port selection. Utopia 2 signaling supports single cell transfers to single output ports, but the 77301 also offers a proprietary multicasting protocol. Multicasting enables a single cell to be transferred simultaneously to multiple selected output ports.

The four output ports can be configured as 9-bit or 4-bit wide data buses. (18-bit wide buses can be supported with multiple 77301's with no

Functional Block Diagram



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additional logic required.) Utopia 1 signalling protocol is supported for these ports. Data can be read from each FIFO output port independently.

Separate input and output port clocks are provided and can be operated up to 62.5 MHz. This provides the user with 1.125Gbps composite bandwidth on the input port and 562Mbps bandwidth on each output port.

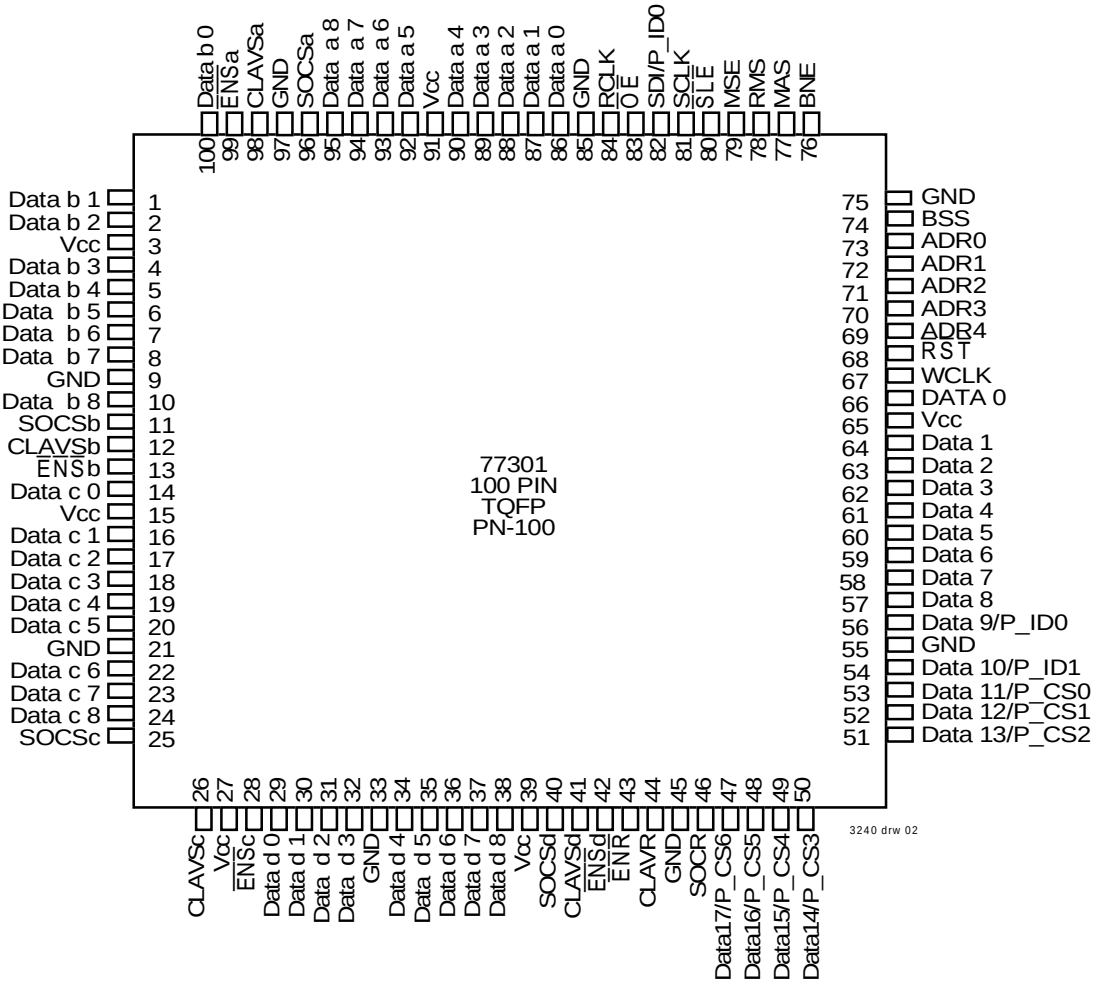
Each 77301 has a unique programmable chip identification register. Multiple UtopiaFIFOs with programmed chip identification can be utilized to direct a 9, 18, 36 or 64-bit bus to as many as 31 output ports.

The principle application for the 77301 is in ATM networking based systems, but can be used in any cell based data or telecommunications application requiring the separation of independent data streams from a single input channel.

Functional Description

The signaling mode of operation is Utopia Transmit (UtopiaTx). With UtopiaTx, data transfer is initiated by the device able to receive a cell by asserting the TxCLAV (cell space available, CLAVR for the input port of the 77301). The device sending data responds, if a cell is available for transfer, by asserting the enable, TxENB ($\overline{ENR}$ and $\overline{ENS}$ for the 77301). During the first byte transfer the TxSOC is asserted to identify the beginning of the cell transfer. Successive clocks transfer the cell until the last data transfer. The transfer can only be interrupted by the transmitting agent by deasserting the TxENB signal. Once reasserted, the process will continue. Upon completion of the last byte transfer, the condition for additional transfers is determined by the TxCLAV and TxENB as before. This is described in greater detail in the Utopia ATM-PHY Level 2 version 1 Document.

Pin Confiturations



Pin Description

Symbol	Name	I/O	Description
1-2, 4-8, 10, 100	DATA-b	O	Data bus output for FIFO-b. Master Mode with BNE HIGH: output is a 9-bit word. Master Mode with BNE LOW: data bus output is a data nibble (Q0-Q3); Q4-Q6 data lines unused; data out Q7 is an output enable control signal to the slave device; Q8 is an output of bit 9/18 valid during the low and high nibble transfer. Slave Mode with BNE LOW: data bus output is a data nibble (Q0-Q3); Q4-Q7 lines unused; Q8 is an output of D8/D17 valid during the low and high nibble transfer.
11	SOCS-b	O	Start Of Cell (FIFO-b). Output from UtopiaFIFO. Active on first byte of data transfer. SOCS deasserts for all remaining byte transfers.
12	CLAVS-b	I	Cell Available (FIFO-b). CLAVS notifies the UtopiaFIFO port a cell transfer can be initiated by the port.
13	$\overline{\text{ENS}}$-b	I/O	Enable (FIFO-b). Master Mode: $\overline{\text{ENS}}$ is an active low output. When asserted, a data transfer will take place on the current clock cycle. Slave Mode: $\overline{\text{ENS}}$ is an input which causes the fifo port to update a data nibble (Q0-3) on the output bus on the next read clock edge.
14, 16-20, 22-24	DATA-c	O	Data bus output for FIFO-c. Master Mode with BNE HIGH: output is a 9-bit word. Master Mode with BNE LOW: data bus output is a data nibble (Q0-Q-3); Q4-Q6 data lines unused; data out Q7 is an output enable control signal to the slave device; Q8 is an output of bit 9/18 valid during the low and high nibble transfer. Slave Mode with BNE LOW: data bus output is a data nibble (Q1-Q3); Q4-Q7 lines unused; Q8 is an output of D8/D17 valid during the low and high nibble transfer.
25	SOCS-c	O	Start Of Cell (FIFO-c). Output from UtopiaFIFO. Active on first byte of data transfer. SOCS deasserts for all remaining byte transfers.
26	CLAVS-c	I	Cell Available (FIFO-c) CLAVS notifies the UtopiaFIFO port a cell transfer can be initiated by the port.
28	$\overline{\text{ENS}}$-c	I/O	Enable (FIFO-c). Master Mode: $\overline{\text{ENS}}$ is an active low output. When asserted, a data transfer will take place on the current clock cycle. Slave Mode: $\overline{\text{ENS}}$ is an input which causes the fifo port to update a data nibble (Q0-3) on the output bus on the next read clock edge.
29-32, 34-38	DATA-d	O	Data bus output for FIFO-d. Master Mode with BNE HIGH: output is a 9-bit word. Master Mode with BNE LOW: data bus output is a data nibble (Q0-Q3); Q4-Q6 data lines unused; data out Q7 is an output enable control signal to the slave device; Q8 is an output of bit 9/18 valid during the low and high nibble transfer. Slave Mode with BNE LOW; data bus output is a data nibble (Q0-Q3); Q4-Q7 lines unused; Q8 is an output of D8/D17 valid during the low and high nibble transfer.
40	SOCS-d	O	Start Of Cell (FIFO-d). Output from UtopiaFIFO. Active on first byte of data transfer. SOCS deasserts for all remaining byte transfers.
41	CLAVS-d	I	Cell Available (FIFO-d). CLAVS notifies the UtopiaFIFO port a cell transfer can be initiated by the port.
42	$\overline{\text{ENS}}$-d	I/O	Enable (FIFO-d). Master Mode: $\overline{\text{ENS}}$ is an active low output. When asserted, a data transfer will take place on the current clock cycle. Slave Mode: $\overline{\text{ENS}}$ is an input which causes the fifo port to update a data nibble (Q0-3) on the output bus on the next read clock edge.
43	$\overline{\text{ENR}}$	I	Input port write enable. Each data write requires $\overline{\text{ENR}}$ assertion.
44	CLAVR	O	Input port Cell space Available. Notifies the controlling agent the FIFO(s) selected by the address bus can accept a complete cell.
46	SOCR	I	Input port Start of Cell. Assertion: first work is currently on bus.
47-53	Data 17-11/ P_CS 6-0	I	BSS low (18-Bit bus): Data bus input Data 11-Data 17 BSS high (9-bit bus): Input port for loading programmable registers.

3240 tbl 01

Pin Description

Symbol	Name	I/O	Description
54, 56	Data 9-10 / P_ID 0-1	I	18-Bit bus: Data bus input 9-bit bus: Parallel programmable register load (ID0, ID1)
57-64, 66	Data 0-8	I	Data bus input
68	$\overline{RST}$	I	Reset. Clears all FIFO memory locations, cell size read/write pointers.
69-73	ADR0-4	I	Address Location(s). Provide cell destination and multicast addresses. Singlecast Operation: for out-band routing, address location is loaded from incoming Utopia Level 2 compliant address lines; for in-band routing, address location is derived from data lines D0-D17 (see Table 1a). Multicast Operation for out-band routing, the ADR0-3 signals (ADR4 is not used) act as enables which select the desired output FIFO combination (see Table 1b); for in-band routing, the output FIFO combindation is derived from the data lines D0-D17.
74	BSS	I	Bus Size Select. BSS HIGH, the input bus is set to 9-bits (D0-D8) and D9-D17 determine cell size and chip ID. BSS LOW, the input bus is 18-bits.
67	WCLK	I	Input port Data write clock.
76	BNE	I	Byte Nibble Enable. BNE HIGH, output ports are byte wide data buses. BNE LOW, output data is in 4-bit "nibble" increments using Q0-Q3. This mode supports wide input data bus applications of 32 to 72-bit widths.
77	MAS	I	Multicast/Address Select. Determines single or multicast input mode. Selecting MAS HIGH sets the device to multicast mode with ADR0-3 as enables. MAS LOW the device is set to single destination mode with ADR0-4 lines as address lines.
78	RMS	I	Routing Method Select. With RMS HIGH, In-band Routing is selected. With RMS LOW, Out-band Routing is selected.
79	MSE	I	Master Slave Enable. With MSE set HIGH, device is set as a master; with MSE LOW, device is set as a slave.
80	$\overline{SLE}$	I	Serial Load Enable.
81	SCLK	I	Serial Load Clock.
82	SDI/P_ID0	I	BSS low, Serial data load. BSS high Serial input port for loading programmable registers.
83	$\overline{OE}$	I	Output Enable. Tri-States all data output buses.
84	RCLK	I	Data read clock.
86-90, 92-95	DATA-a	O	Data bus output for FIFO-a. Master Mode with BNE HIGH: output is a 9-bit word. Master Mode with BNE LOW: data bus output is a data nibble (Q0-Q3); Q4-Q6 data lines unused; data out Q7 is an output enable control signal to the slave device; Q8 is an output of bit 9/18 valid during the low and high nibble transfer. Slave Mode with BNE LOW: data bus output is a data nibble (Q0-Q3); Q4-Q7 lines unused; Q8 is an output of D8/D17 valid during the low and high nibble transfer.
96	SOCS-1	O	Start Of Cell (FIFO-a) output from UtopiaFIFO. Active on first byte of data transfer. SOCS deasserts for all remaining byte transfers.
98	CLAVS-a	I	Cell Available (FIFO-a). CLAVS notifies the UtopiaFIFO port. A cell transfer can be initiated by the port.
99	$\overline{ENS}$-s	I/O	Enable (FIFO-a). Master Mode: $\overline{ENS}$ is an active low output. When asserted, a data transfer will take place on the current clock cycle. Slave Mode: $\overline{ENS}$ is an input which causes the fifo port to update a data nibble (Q0-3) on the output bus on the next read clock edge.
	GND	—	Logic and supply ground pins 9, 21, 33, 45, 55, 75, 85 and 97.
	V_{CC}	—	Logic and supply V_{CC} pins 3, 15, 27, 39, 65, and 91.

3240 tbl 02

Absolute Maximum Ratings

Symbol	Rating	Commercial	Industrial	Unit
V_{TERM}	Terminal Voltage with respect to ground	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-40 to +85	C
T-Bias	Temperature under Bias	-55 to +155	-55 to +155	C
T-STG	Storage Temperature	-55 to +155	-55 to +155	C
I_{OUT}	DC Output Current	50	50	mA

3240 tbl 03

Recommended DC Operating Conditions

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Commercial Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage Commercial	2.0	—	V_{CC}+0.3	V
V_{IL}	Input Low Voltage Commercial	-0.3	—	0.8	V

3240 tbl 04

DC Electrical Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Unit
I_{LI}	Input Leakage Current	-1	—	1	µA
I_{LO}	Output Leakage Current	-10	—	10	µA
V_{OH}	Output Logic "1" Voltage, I_{OH}=-4mA@2.4V	2.4	—	—	V
V_{OL}	Output Logic "0" Voltage I_{OL}=+4mA@0.4V	—	—	0.4	V
I_{CC1}	Input Low Voltage Commercial	—	—	150	mA

3240 tbl 05

Capacitance

Symbol	Parameter	Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN}=0V	10	pF
C_{OUT}	Output Capacitance	V_{OUT}=0V	10	pF

3240 tbl 06

Current

Symbol	Parameter	Conditions	Max.	Unit
I_{CC}-Active	Active Power Supply Current @ 20 MHz	$\overline{OE}$ = High	45	mA
I_{CC}-DC	DC Power Supply	$\overline{OE}$ = High	30	mA

3240 tbl 07

AC Test Conditions

Input Pulse Levels	0 to 3.0V
Input Rise/Fall Times	2ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
AC Test Load	See Figure 1

3240 tbl 08

AC Test Load

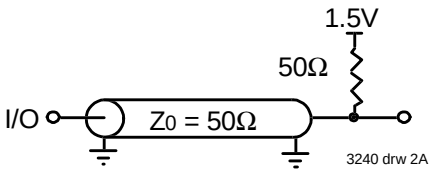


Figure 1: AC Test Load

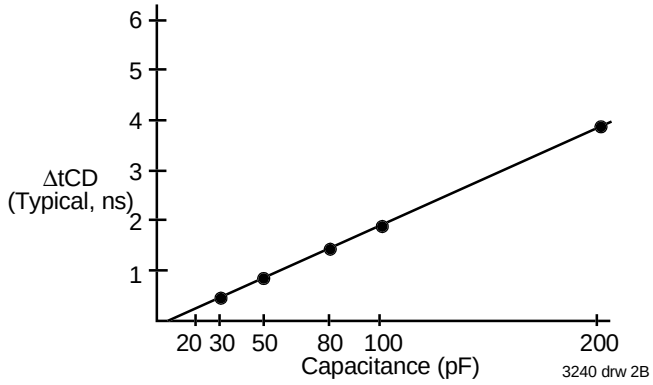


Figure 2: Lumped Capacitive Load, Typical Derating

AC Electrical Characteristics[1, 3]

(Commerical: Vcc = 5V ± 10%, TA = 0°C to 70°C; Industrial: Vcc= 5V ± 10%, TA = -40°C to 85°C)

TX/RX Mode		Commercial		Industrial		
		77301L12		77301L12		
Symbol	Parameter	Min.	Max.	Min.	Max.	Unit
f_S	Clock Cycle Frequency	—	62.5	—	62.5	MHz
t_A	Data Access Time	2	10	2	10	ns
t_{CLK}	Clock Cycle Time	16	—	16	—	ns
t_{CLKH}	Clock High Time	7	—	7	—	ns
t_{CLKL}	Clock Low Time	7	—	7	—	ns
t_{RS}	Reset Pulse Width[1]	12	—	12	—	ns
t_{RSS}	Reset Set-up Time	12	—	12	—	ns
t_{RSR}	Reset Recovery Time	10	—	10	—	ns
t_{PRS}	Reset to Output Time	—	8	—	8	ns
t_{CLAVS}	Cell Available Set-up Time, CLAVS to RCLK	4.5	—	6	—	ns
t_{CLAVH}	Cell Available Hold Time, RCLK to CLAVS	0	—	0	—	ns
t_{ENRS}	Enable Set-up Time, $\overline{ENR}$ to WCLK	5.5	—	6	—	ns
t_{ENRH}	Enable Hold Time, WCLK to $\overline{ENR}$	0	—	0	—	ns
t_{ENSS}	Enable Set-up Time, $\overline{ENS}$ to WCLK	4.5	—	4.5	—	ns
t_{ENSH}	Enable Hold Time, WCLK to $\overline{ENS}$	0	—	0	—	ns
t_{SLES}	Serial Load Set-up Time, SLE to SCLK	6	—	6	—	ns
t_{SLEH}	Serial Load Hold Time, SCLK to SLE	0	—	0	—	ns
t_{ADRS}	Address Set-up Time to WCLK	6	—	6.5	—	ns
t_{ADRH}	Address Hold Time, WCLK to Address	0	—	0	—	ns
t_{SKEW1}	Skew Time between RCLK and WCLK[2]	11	—	11	—	ns
t_{SKEW2}	Skew Time between WCLK and RCLK[2]	11	—	11	—	ns
t_{DS}	Data Set-up Time, Data to WCLK	5	—	5	—	ns
t_{DH}	Data Hold Time, WCLK to DATA	0	—	0	—	ns
t_{SOCRS}	SOCR Set-up Time, SOCR to WCLK	5.5	—	5.5	—	ns
t_{SOCRH}	SOCR Hold Time, WCLK to SOCR	0	—	0	—	ns
t_{PSOC}	RCLK to SOCS	—	10	—	10	ns
t_{PCLAVR}	WCLK to CLAVR	—	10	—	10	ns
t_{PENS}	RCLK to $\overline{ENS}$	—	10	—	10	ns
t_{OE}	$\overline{OE}$ to Qn Valid	1	10	1	10	ns
t_{OHZ}	$\overline{OE}$ to Qn in High Z[2]	—	10	—	10	ns
t_{OLZ}	$\overline{OE}$ to Qn in Low Z[2]	0	—	0	—	ns

3240 tbl 09

NOTES:
1. Pulse widths less than minimum values are not allowed.
2. Values guaranteed by design, not currently tested.
3. The IDT77301 timing specs are not equal to those of the IDT77305.

Table 1a: FIFO Address Allocation for Singlecast Mode

Device ID	ADR(4:0)
0	000xx
1	001xx
2	010xx
3	011xx
4	100xx
5	101xx
6	110xx
7	111xx

FIFO port	ADR(4:0)
A	xxx00
B	xxx01
C	xxx10
D	xxx11

x = Don't Care

3240 tbl 10

Table 1b: FIFO Address Allocation for Multicast Mode

FIFO(s) Selected	ADR3	ADR2	ADR1	ADR0
No Selection	0	0	0	0
A	0	0	0	1
B	0	0	1	0
C	0	1	0	0
D	1	0	0	0
A,B	0	0	1	1
A,C	0	1	0	1
A,D	1	0	0	1
B,C	0	1	1	0
B,D	1	0	1	0
C,D	1	1	0	0
A,B,C	0	1	1	1
A,B,D	1	0	1	1
A,C,D	1	1	0	1
B,C,D	1	1	1	0
A,B,C,D	1	1	1	1

3240 tbl 11

Selection of a particular implementation for the input port and output ports are easily made by configuring the following signals:

INPUT PORT CONFIGURATION

RMS (Routing Method Select) "1" in band routing; "0" out band routing

MAS (Multicast Address Select) "1" enable multicast; "0" enable single cast

BSS (Bus Size Select) "1" enable 9-bit bus; "0" enable 18-bit bus

OUTPUT PORT CONFIGURATION

MSE (Master/Slave Enable) "1" enable master mode; "0" enable slave mode

BNE (Byte/Nibble Enable) "1" enable byte mode; "0" enable nibble mode

ROUTING METHOD SELECT (RMS)

The output FIFO cell destination is set with the Routing Method Select (RMS) pin to either in-band or out-band routing. When using in-band routing (RMS=1), refer to Figure 2a, the first 9 or 18-bit word, indicated by SOCR, contains the 4-bit address of the output FIFO port. When using out-band routing (RMS=0), refer to Figure 2b, a 5-bit output FIFO port address is placed on the ADR(4:0) address bus. In both cases, the address is loaded into the 77301 on its ADR(4:0) address bus.

MULTICAST/ADDRESS SELECT (MAS)

The Multicast/Address Select (MAS) pin determines which routing method is to be used. In Multicast mode (MAS=1) an incoming cell can be sent to any combination of output FIFO port(s). When using out-band routing (RMS=0) the 4-bit output FIFO address is placed directly on the ADR(3:0) bus. Address line ADR4 is not used. Multicast output FIFO address selection is described in Table 1b.

In Singlecast mode (MAS=0) an incoming cell can be sent to one output FIFO port. The first two bits, ADR0 and ADR1, select the output FIFO port, while the upper three bits ADR2, ADR3 and ADR4 select the appropriate 77301 according to its Device ID. ADR(4:0) equal to 11111 is reserved for a Null PHY port. No PHY port will respond to this address. Refer to Table 1b for output FIFO address selection.

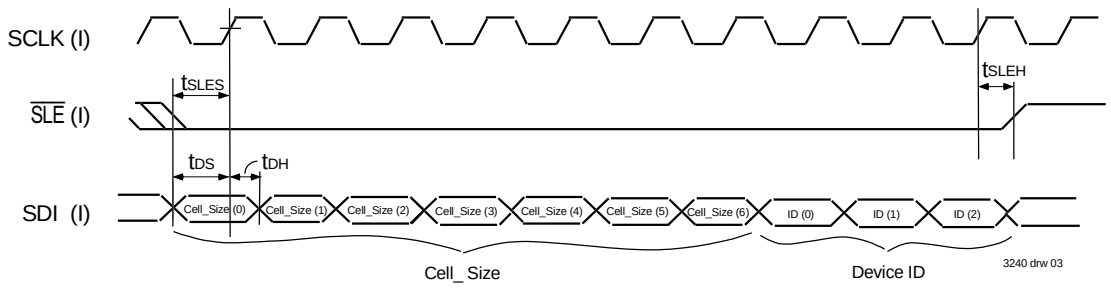
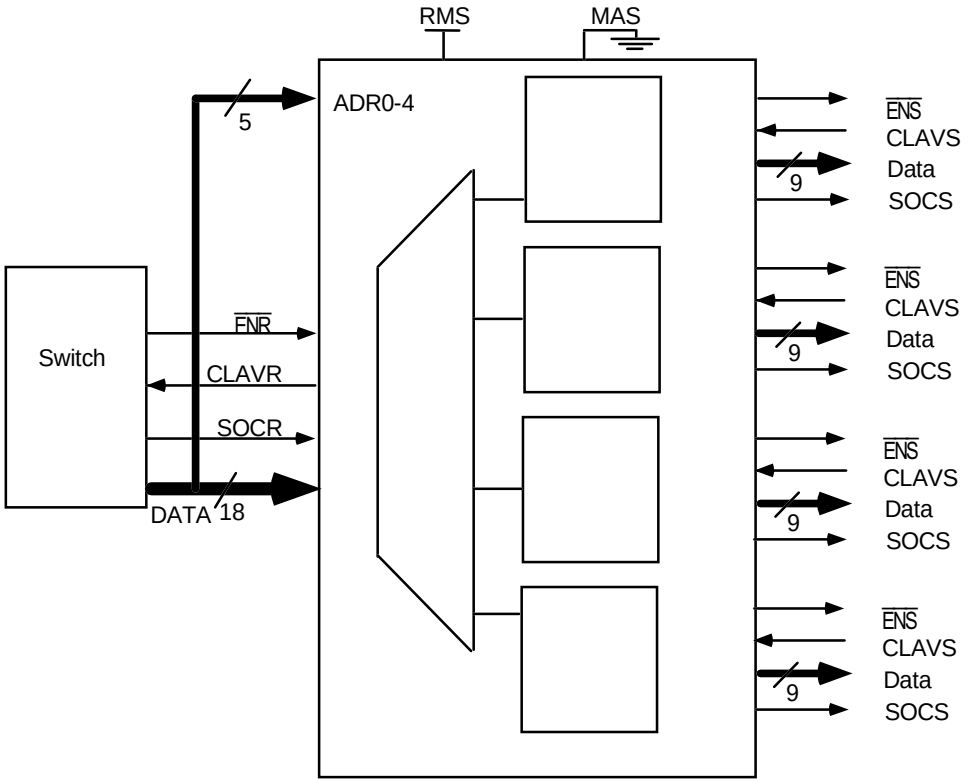
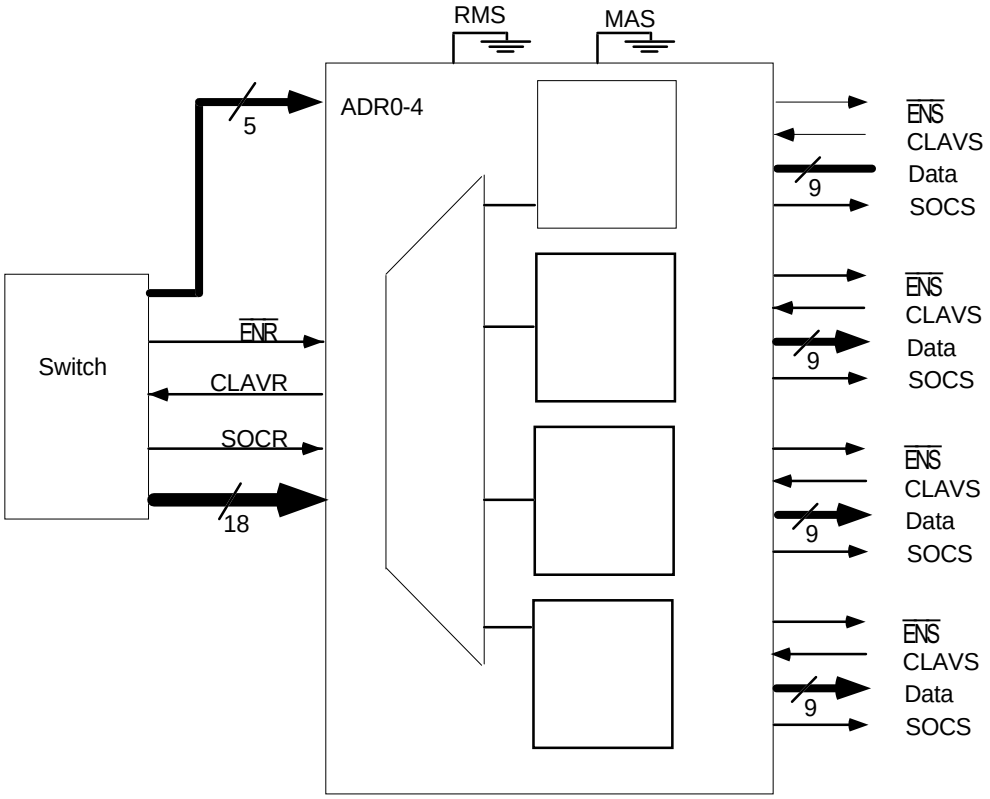


Figure 1: Serial Loading of Cell Size and Device ID (x18 bit Mode)



3240 drw 04

Figure 2a. In-Band Routing, Single Device Implementation



3240 drw 05

Figure 2b. Out-Band Routing, Single Device Implementation

Cell Size Programming

Data is transferred in "cells"; for ATM, cell size is 53/54 bytes on an 8/16-bit bus. The UtopiaFIFO can be programmed through the cell size selection registers to any number of bytes between 16 and 128. Programing is accomplished through a serial load port when the BSS is low (18 bit input data bus) and parallel loading when BSS is high (9 bit input data bus) using the spare input data pins.

Use the Serial Load Enable ($\overline{SLE}$), Serial Clock (SCLK) and the Serial Data Load (SDI) pins to serially program the cell size and the device ID. After Reset the ten bits are loaded to program the cell size and device ID. The first seven bits program the cell size, with the first bit being the LSB. The last three bits program the device ID, with the first of these three bits being the LSB. For a cell size of 128 bytes set all seven cell size bits to zero. You must set all ten bits when programing this register, even though the singlecast mode does not require a device ID. The device ID is the PHY port group as defined in the Utopia level 2 version 1 document. Refer to Figure 1 for cell size timing diagram.

BSS

To set the Utopia FIFO input bus width to 9-bits, set Bus Size Select (BSS) HIGH. In this mode SDI along with inputs D9 to D17, are used to hardwire program the chip ID and cell size values directly (serial loading disabled).

For odd byte cell sizes (in 18-bit input mode), the UtopiaFIFO will internally write a dummy byte into the last byte position. Upon reading the cell, this last byte is ignored; hence, this temporary byte stuffing is transparent to the user. This does however, add to the memory utilization and reduces the total number of bytes available by one for each cell the FIFO is capable of handling.

Control signals for the input data transfer side consists of CLAVR, $\overline{ENR}$, and SOCR (see Table 2). Prior to cell transfer, the controlling agent (data source for transmit mode) is notified a cell transfer can take place to the UtopiaFIFO through the assertion of the CLAVR signal. Each word transfer of a cell is completed by assertion of $\overline{ENR}$, which is supplied by the controlling agent. During the first data word transfer, the data source asserts SOCR to mark the beginning of the cell. Data transfer continues until the cell transfer is completed. When the cell size is reached, further writes are blocked until new $\overline{ENR}$ and SOCR signals are received and a complete cell can be accepted. The particular FIFO receiving data is selected by the ADR0-4 lines; if available memory to store a complete cell exists, the CLAVR signal is asserted.

In multicast mode, cell transfer will occur only when all chosen FIFO destinations have space for a complete cell. If any destination cannot take a cell, the UtopiaFIFO will set CLAVR LOW. Once all destinations are available, CLAVR will be asserted.

With UtopiaTx mode (Figure 3), the CLAVR signal is an output from the UtopiaFIFO telling the sending (controlling) agent that a complete cell can be accepted by the selected FIFOs. The controlling agent asserts $\overline{ENR}$ to the UtopiaFIFO and data is written to the selected FIFO on the same clock edge. As required by the Utopia protocol specifications, the CLAVR will go LOW at least four clock cycles prior to the last word transfer if the UtopiaFIFO cannot accept another cell.

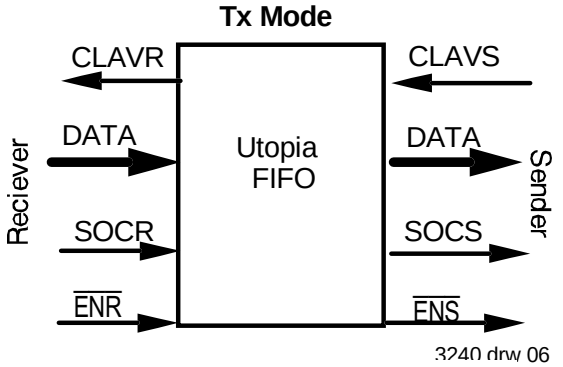


Figure 3. Signal and Data I/O Directions for Tx Mode

Table 2: Pin I/O status for receiver (input) side Signals (Tx Mode)

	Receiver (Input) I/O TX
CLAVR	O
$\overline{ENR}$	I
SOCR	I
Data	I
Clock	I
ADR0-4	I

3240 tbl 12

Table 3: Output Side of UtopiaFIFO

Output Pin	Tx Mode I/O
$\overline{ENR}$	O
CLAVS	I
SOCR	O
Data	O

3240 tbl 13

OUTPUT CONFIGURATION

The I/O status of the output pins are listed in Table 3. In UtopiaTX mode, the CLAVS is an input to the UtopiaFIFO signaling a complete cell can be transferred. As the controlling agent, the UtopiaFIFO asserts an output signal, $\overline{ENS}$, to transfer data on the same rising clock edge. SOCS is asserted for the first output byte only.

For operation in master mode with 9-bit output, operation is the same as in the Utopia Level I specification. Once a CLAVS signal is asserted to a selected output FIFO location, if a complete cell is available to be

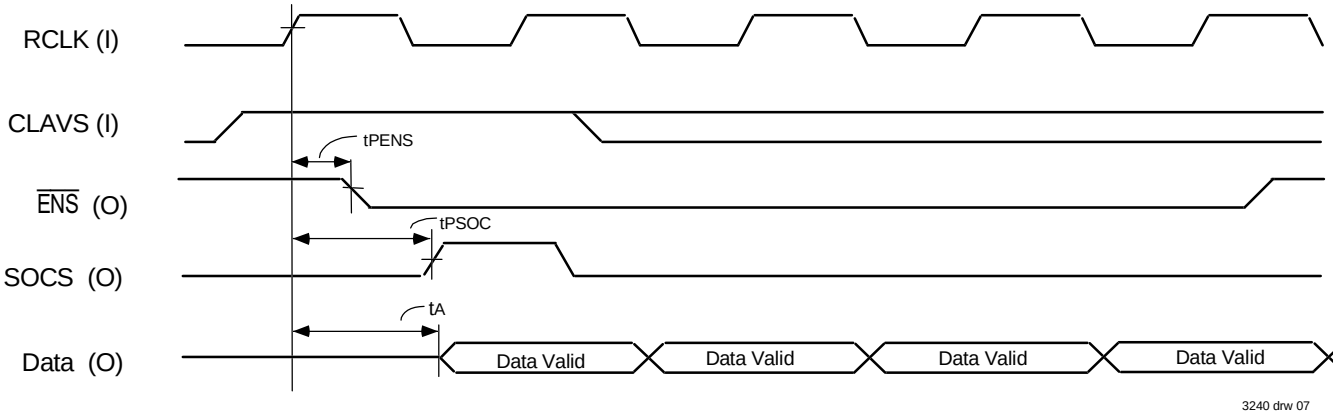


Figure 4. UtopiaFIFO Tx Mode Output Waveforms

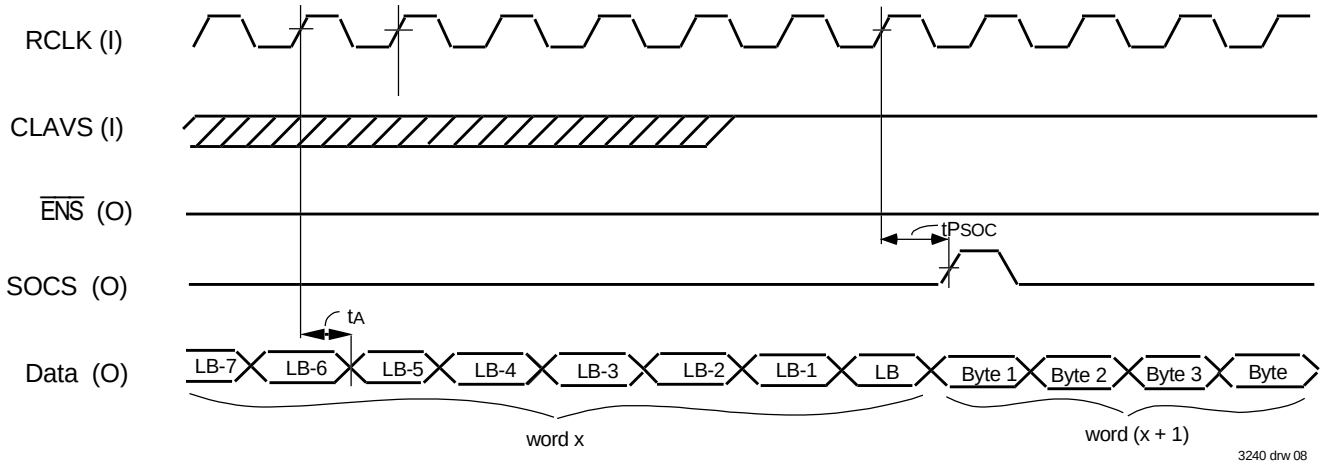


Figure 5. UtopiaFIFO Tx Mode Output Waveforms (Continuous Cell Transfers)

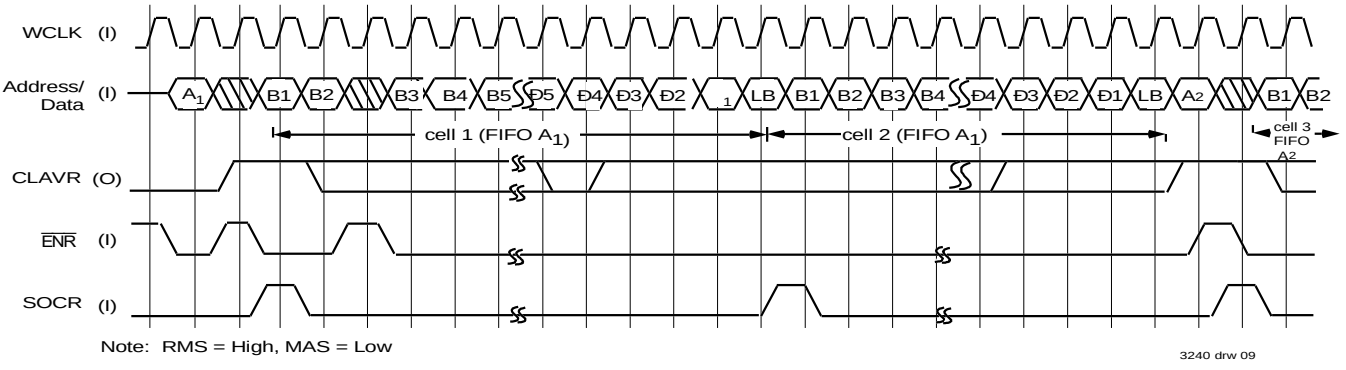


Figure 6. In-Band Routing, Singlecast Timing

transferred, $\overline{ENS}$ is asserted, data is placed on the bus and SOCS is set HIGH for the first 9-bit word transfer. $\overline{ENS}$ will remain LOW and data transfer will continue until the entire cell is sent (see Figure 4). If during cell transfer, CLAVS de-asserts, transfer continues. Continuous cell transfer with no latency is possible. If CLAVS asserts prior to the last 9-bit word transfer, and a complete cell can be sent, $\overline{ENS}$ remains LOW and the next cell is sent. SOCS will assert during the first word transfer (see Figure 5).

Three additional control signals provide added device functionality. The global reset ($\overline{RST}$) pin clears all register values. The Master Slave Enable (MSE) and Byte Nibble Enable (BNE) pins are used in the building block implementation with an input bus of 32 or 64-bits where up to 32 separate UtopiaFIFOs can be utilized. These pins allow the elimination of glue logic in the building block mode and ensure synchronization of cells on the output data bus.

The following sections describe in detail the input side timing and data/signal connections for various combinations. The first four sections describe operations for a single UtopiaFIFO implementation: In-Band Routing-Single and Multicast; Out-Band Routing-Single and Multicast. The next four sections describe usage in a building block implementation (up to eight independent devices): In-Band Routing-Single and Multicast; Out-Band Routing-Single and Multicast. A final section describes operations for a 36-bit input bus connected to a maximum of 16 UtopiaFIFOs.

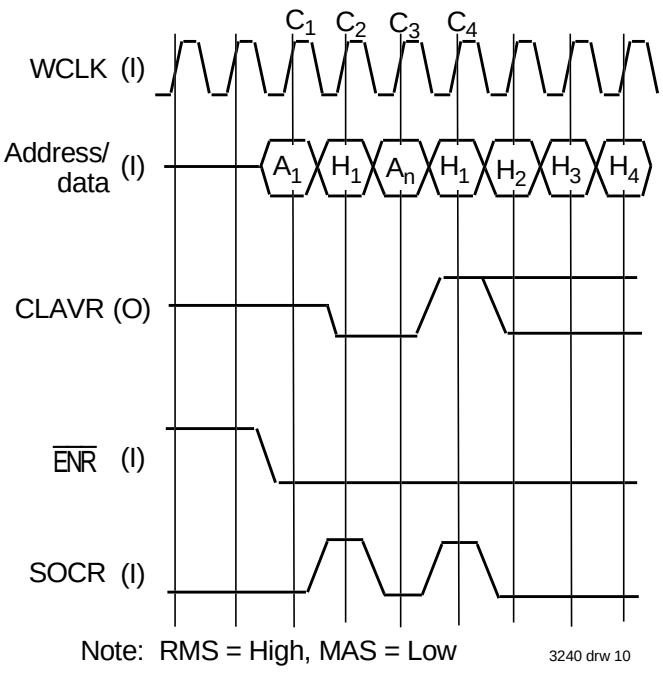


Figure 7. Receive Polling FIFO Full

Single Device Implementation

IN-BAND ROUTING

SINGLE FIFO DESTINATION (NO MULTICAST)

Single FIFO destination timing is described by Figure 6. Figure 2a shows the data/signal connections.

Configuration: RMS = "1" indicates in-band routing.
MAS = "0" indicates singlecast mode.
BSS = "X" either 9 or 18 bit operation

With no current cell transfer, CLAVR and SOCR are LOW, the address/data bus is tri-stated, and $\overline{ENR}$ is HIGH. To select a FIFO destination, $\overline{ENR}$ is asserted and the desired address is placed on the bus. With SOCR LOW and no current data transfer, the UtopiaFIFO recognizes this word as an address and the value is latched in the address line registers (and not written as data). On the next cycle, the sender may automatically load the first data word on the address/data bus and assert SOCR. At this clock cycle, if CLAVR is asserted, then a complete cell can be accepted, and data is automatically written into the FIFO.

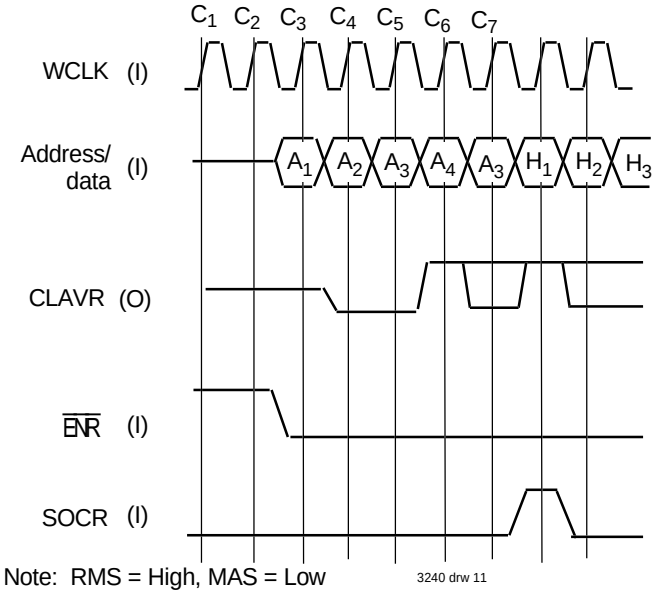


Figure 8. Receive Polling FIFO Not Full

If the selected FIFO cannot accept a complete cell, CLAVR goes LOW and the data and SOCR signal are ignored (see Figure 7). At clock cycle C2, the sender recognizes a LOW CLAVR. On clock C3, the sender places a second (or the same) address on the address/data bus. On clock C4, the sender again places data on the bus with a HIGH SOCR. At C4, the sender recognizes a HIGH CLAVR and "knows" the data and SOCR signals were loaded. On subsequent cycles, the remaining data is placed on the bus with an asserted $\overline{ENR}$. As in figure 6.0, if an interruption takes place through $\overline{ENR}$ de-assertion, no data is transferred on that clock. Once

$\overline{ENR}$ is again asserted, the next data byte will be placed in the appropriate place in memory (no bad data or address will be written).

If desired, the sender can wait until a HIGH CLAVR signal before placing data on the bus; this allows the sender to "poll" different address's on every clock cycle (see figure 8). For cases where an address may not be available for several cycles, this allows a quicker determination of an available address. A different address can be polled every clock versus one every other clock for the prior case. However, there is added latency once an address is found with an available cell space. Two additional cycles are needed (C4 and C5) between the address with space available and actual loading of data (on C6). Once a cell transfer is started (assertion of SOCR), all data on the address/data bus will be recognized as data, not as an address. Any assertion of SOCR prior to cell transfer completion results in an error condition (see cell length error recovery).

Once the current cell transfer is complete, the next cell transfer to the same FIFO destination can occur with no delay if CLAVR is HIGH before the next clock cycle's rising edge (Clock Cx). No new address is placed on the bus. A LOW $\overline{ENR}$ combined with a HIGH CLAVR and newly asserted SOCR indicates the first word of the next cell. The word is written as data.

If CLAVR is LOW at the end of current cell transfer, the UtopiaFIFO will interpret the next word as an address. With a LOW CLAVR, an asserted SOCR on the data on the bus will be ignored.

If the same FIFO is to be selected but has no space available, CLAVR is LOW. The sender evaluates CLAVR on the cycle after the last word transfer. The UtopiaFIFO flexibility allows for several possible timing schemes. Figure 9 shows the switch loading the first byte of the next cell before the CLAVR signal is known. At C3, data byte H1 is ignored as CLAVR is LOW. Clocks C4 and C5 show the switch waiting until CLAVR asserts. At C5, CLAVR is recognized by the switch and places data on the bus and an asserted SOCR at C6. An alternative is for the switch to immediately place a new address on the bus after cell transfer (clocks C9, C10, C11). At clock C10, available address A2 is recognized and on C12, A2 is placed on the bus. On clock C13, the SOCR is asserted with the start of a new cell; with a HIGH CLAVR, this new data will be accepted.

If a new address is selected, a one cycle delay occurs before the next cell can be sent. After the current cell transfer is completed, the SOCR and $\overline{ENR}$ stay LOW. CLAVR is a don't care. With a LOW SOCR, asserted $\overline{ENR}$, and no cell transfer taking place, the UtopiaFIFO determines a new address location is on the address/data bus. The UtopiaFIFO reads this address location and determines if a complete cell can be accepted. If a new cell can be written, CLAVR is asserted by the following cycle. By holding $\overline{ENR}$ LOW, valid data can be placed on the bus and SOCR is asserted on the same cycle. The UtopiaFIFO will recognize the new data and write to the selected FIFO location.

MULTICAST OPERATION

The UtopiaFIFO can operate in in-band routing mode using the multicast format. The address timing is shown in Figure 10.

Configuration: RMS = "1" indicates in-band routing.
MAS = "1" indicates multicast mode.
BSS = "X" either 9 or 18 bit operation

The UtopiaFIFO will read the address inputs as a series of enables. In this mode, ADR0-3 selects FIFOs A through D respectfully. Address ADR4 is a don't care. Any combination of 4 output destinations can be selected in single device operation (or up to 31 destinations in building block mode). The address read timing is similar to the nonmulticast operation. Table 1 shows the combination of output FIFO destinations depending on the address enables loaded.

In the multicast mode the UtopiaFIFO will not load input data unless all selected FIFO destinations have room for a complete cell. If one or more FIFOs do not have space for a cell, the CLAVR signal will stay LOW and data will not be loaded. Once all selected FIFOs have space, the CLAVR will assert and the upstream system will load data to the UtopiaFIFO by asserting $\overline{ENR}$. SOCR will assert for first word written. Internally, the UtopiaFIFO loads the same cell and SOCR signal into all selected FIFO destinations. If all selected FIFOs cannot accept an additional cell, the CLAVR must go LOW before the fourth from last word transfer takes place. If all selected FIFOs can accept a cell, continuous multicasting can take place to the same selected group of FIFOs (the CLAVR signal must assert prior to last word transfer). With $\overline{ENR}$ asserted, a new cell will transfer with SOCR asserted on the first word.

The timing diagrams 6 and 7 also apply to the multicast mode. The only difference is that a series of enables are used in place of a single address.

If a different set of destination FIFOs is desired, upon current cell transfer completion, the SOCR stays LOW. Continuous assertion of $\overline{ENR}$, with no new SOCR, notifies the UtopiaFIFO that new address' are being loaded.

Dynamic single/multicast location capability is not allowed. To switch from single to multicast requires a reset operation.

OUT-BAND ROUTING
SINGLE FIFO DESTINATION (NO MULTICAST)

Configuration: RMS = "0" indicates out-band routing.
MAS = "0" indicates singlecast Mode.
BSS = "X" either 9 or 18 bit operation.

In this mode the UtopiaFIFO is fully Utopia Level II compliant. The timing sequence is shown in Figure 11. The data and signal connections are shown in Figure 2b. In this approach, the FIFO address' are separate from the data path. No words will be written from the data bus to the address pins ADR(0-4). With no current cell transfer: the CLAVR and SOCR signals are tri-state; the $\overline{ENR}$ is de-asserted and no valid data is on the bus. To "select" a FIFO, a two-clock polling cycle is used. An address is loaded into the ADR0-4 pins with $\overline{ENR}$ de-asserted. On the next clock cycle, the CLAVR asserts if the selected location can accept an entire cell. At this point, an invalid address is placed on the address bus. On the next clock cycle, the CLAVR goes tri-state due to the previous invalid data. The upstream system knows it can ship a complete cell due to the prior HIGH CLAVR signal and places the valid location on the address bus a second time. Then the $\overline{ENR}$ is asserted while CLAVR asserts. SOCR asserts (for first word written) and data is placed on the bus. For each subsequent $\overline{ENR}$ assertion, data is transferred until the cell transfer is completed.

If during cell transfer, $\overline{ENR}$ is de-asserted, data is invalid and the FIFO address on the data bus is not selected (even if it has been previously polled

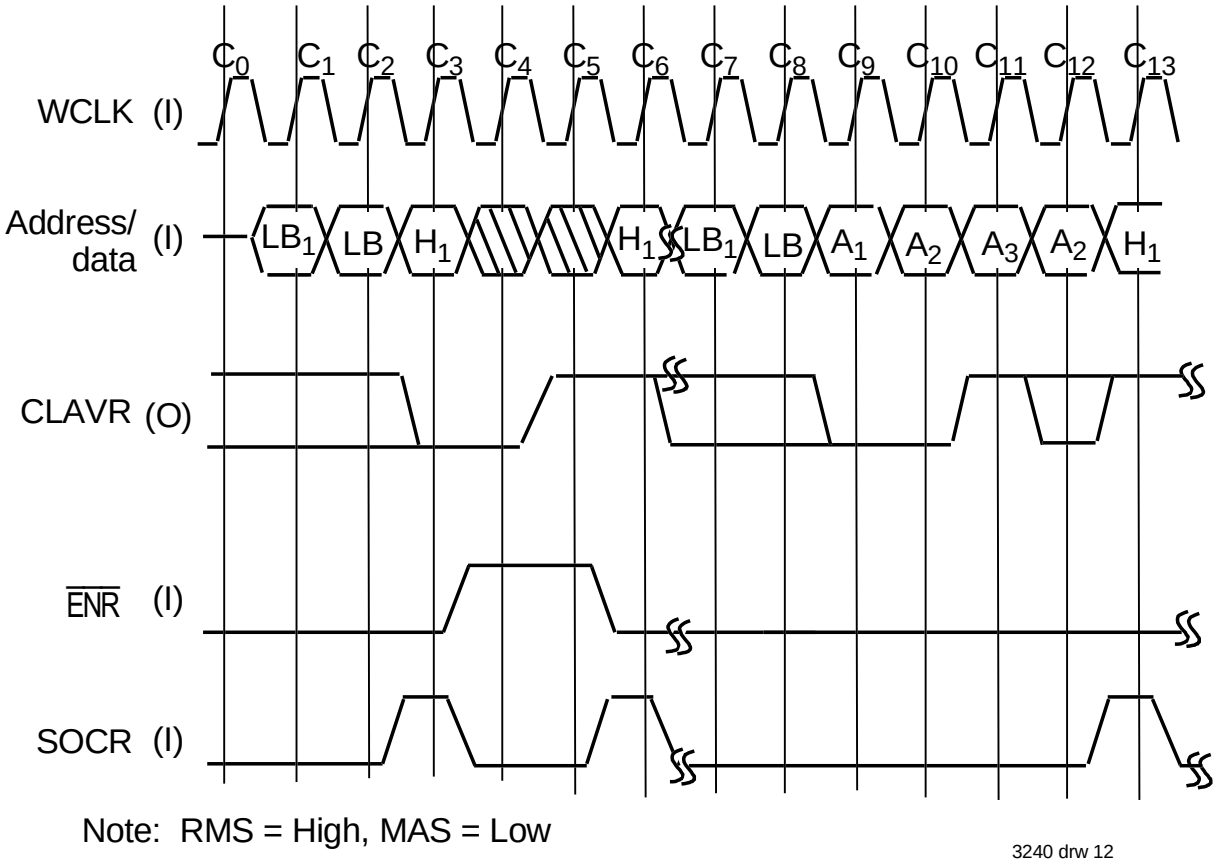


Figure 9. Switch Loading

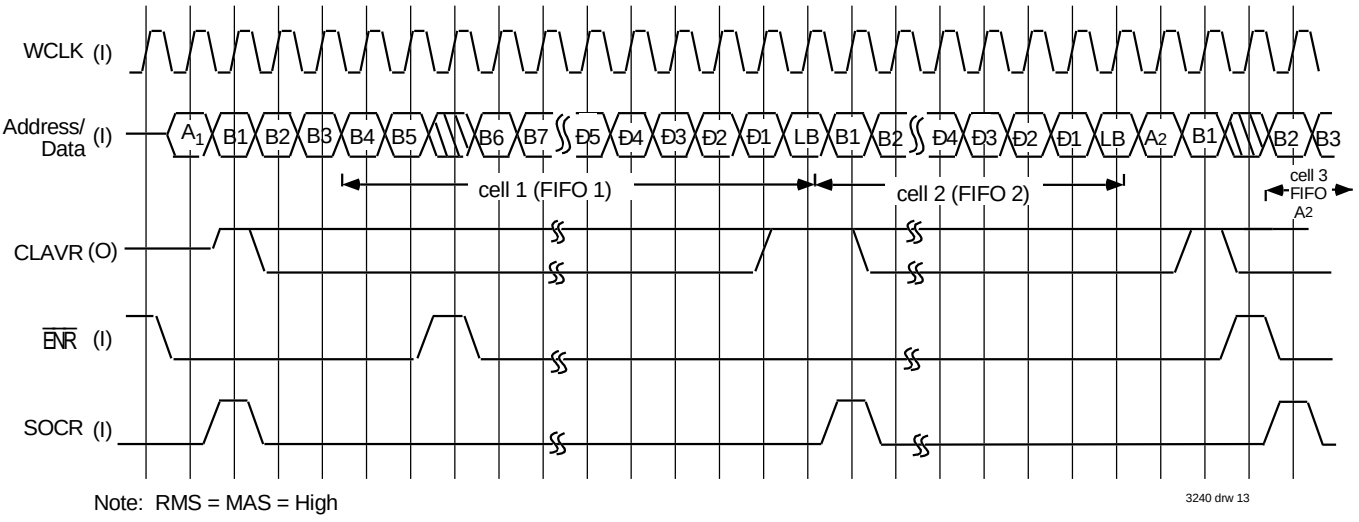


Figure 10. In-Band Routing, Multicast Mode

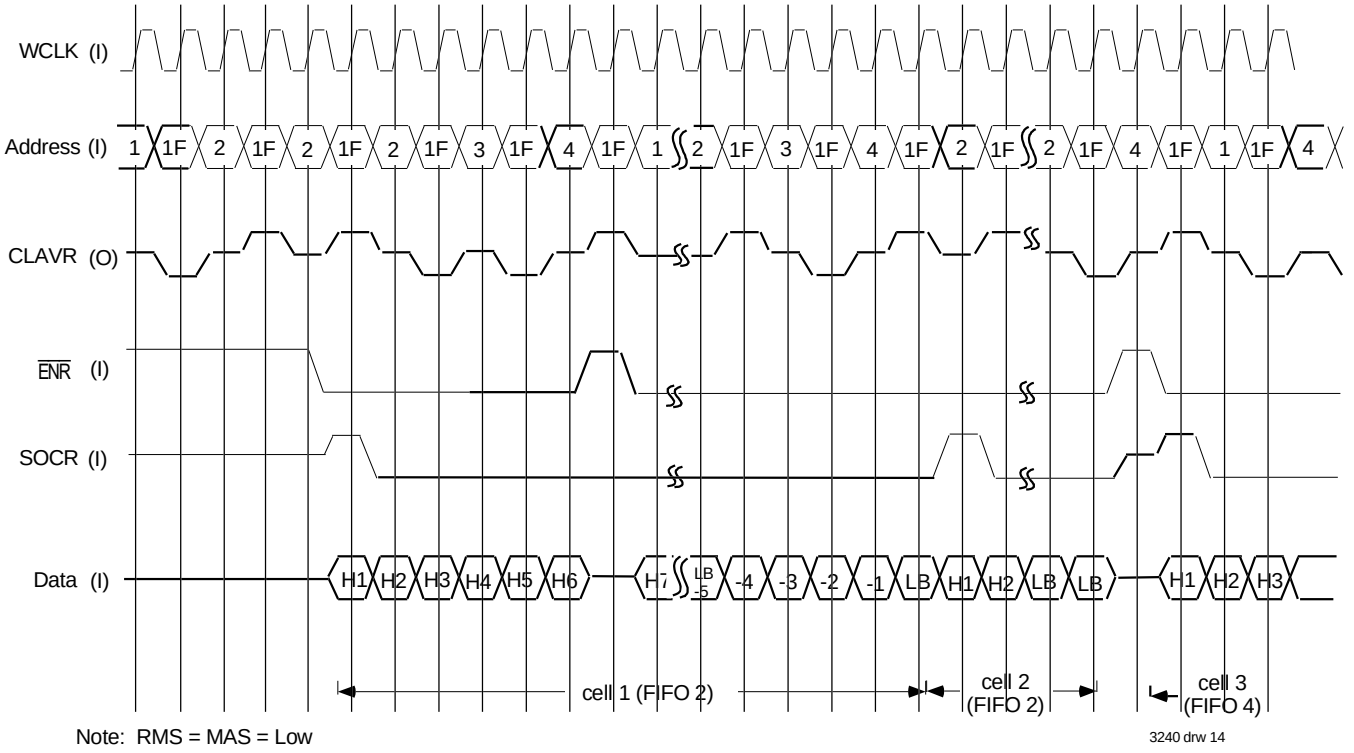


Figure 11. Out-Band Routing, Singlecast Mode

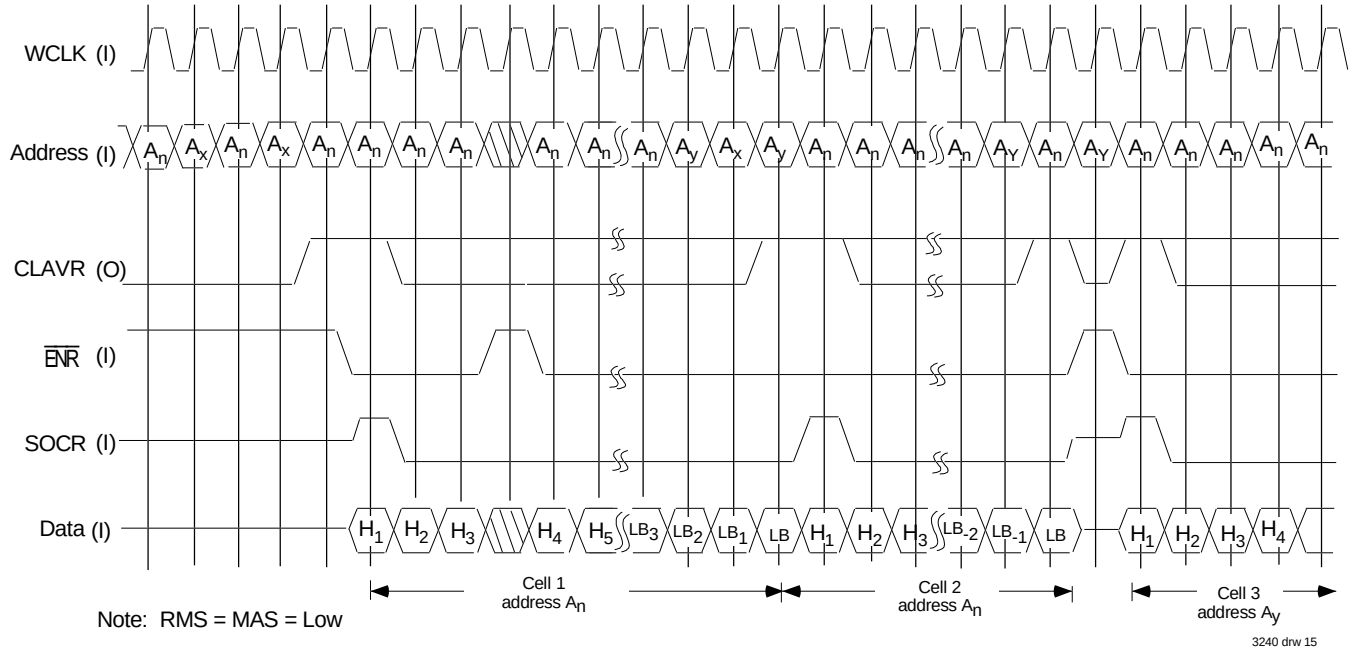


Figure 12. One Cycle Addressing

and is available.) A new FIFO location can only be selected after current cell transfer is complete.

During cell transfer, FIFO "polling" can take place. At any time when the $\overline{ENR}$ is asserted, if a valid address is placed on the address bus, the CLAVR signal will notify the upstream system if the polled address can take a cell. As delineated in the Utopia Level II specifications, a valid address may only be placed on the bus every other cycle. After the invalid address cycle, the CLAVR will always go tri-state. This polling will not affect current cell transfer or the FIFO selected for the next cell transfer.

Figure 11 shows polling can take place while the current FIFO is transferring data; the current FIFO can remain as the "selected" FIFO for a continuous cell transfer. If the next (different) FIFO destination has been polled and has space available, cell transfer will have a one cycle delay. To select a new location, the $\overline{ENR}$ must de-assert while the new address is on the address bus. After the last word of the first cell transfer, the SOCR tri-states and $\overline{ENR}$ de-asserts. At this time the new address (previously polled and determined to have space available) is placed on the address bus. At this time the CLAVR is tri-state from the previous invalid address. On the following cycle, CLAVR, $\overline{ENR}$, and SOCR all assert and data is written into the FIFO. An invalid address is then placed on the address bus. On subsequent clocks with $\overline{ENR}$ asserted, data is placed on the bus until cell transfer is complete. If the next FIFO destination is the same as the prior address, and is known to have a cell available from prior polling, continuous cell transfer can take place.

While the previous operation, as shown in Figure 11, conforms to Utopia Level II specifications, the UtopiaFIFO is capable of faster data transfer which is not Utopia II compliant but, nonetheless, may be desired. Figure 12 shows a "one-cycle" addressing scheme where a null address (1F) need not be placed between valid addresses. In this implementation the latency from address with an available cell space to data transfer is reduced from three to two cycles. While polling new FIFO destinations, a new address can be polled every cycle; this doubles how quickly the switch can determine the next destination availability and reduces potential "wait states".

MULTICAST OPERATION

Configuration: RMS = "0" indicates out-band routing.
MAS = "1" indicates multicast mode.
BSS = "X" either 9 or 18-bit operation

In this mode the address lines are read by the UtopiaFIFO as a series of Enable signals (no longer Utopia Specification Level II compliant). The input timing is shown in Figure 13. The least four significant bits (A0-A3) are read (A4 is DC). These four inputs will allow any combination of the four output FIFOs to receive the next cell. Table 1 delineates the output FIFO combination for each Enable signal A0-A3 combination. The device will only accept data when all selected FIFOs have a cell available. If one or more FIFOs do not have a complete cell size available, the CLAVR signal will remain LOW.

FIFO "polling" can occur in this mode. As with the single destination mode described above, the next Multicast FIFO Combination Enables can be placed on the address bus. Upon receiving a HIGH CLAVR, $\overline{ENR}$ asserts, data is written into the FIFO and SOCR is set HIGH for the first word written. Subsequent $\overline{ENR}$ assertions will load the remaining words of the cell into the FIFO's. If CLAVR is HIGH prior to the last word written, and the next set of cell destinations is the same, continuous cell transfer can occur. The $\overline{ENR}$ stays LOW and the SOCR asserts for the first word of the next cell. The new SOCR signal indicates data is on the bus.

After the cell is transferred, if a new set of FIFO destinations is to be selected, the SOCR tri-states while $\overline{ENR}$ is de-asserted. A combination of a tri-stated SOCR and HIGH $\overline{ENR}$ indicates a new set of enables is on the address bus. Due to prior polling of this combination, the switch knows the set of FIFO destinations are available. If no prior polling, the switch will need to go through the "two-cycle" polling scheme described earlier (until all destinations can accept a complete cell). On the next clock cycle, SOCR goes HIGH to indicate the start of a new cell (clock Cx). $\overline{ENR}$ is asserted and data placed on the data bus. Changing the set of FIFO destinations during multicast results in only a one clock cycle delay if the new locations are available.

Building Block Implementation

IN-BAND ROUTING
SINGLE FIFO DESTINATION (NO MULTICAST)

Configuration: RMS = "1" indicates in-band routing.
MAS = "0" indicates singlecast mode.
BSS = "0" 18 bit operation

Figure 14 shows the data and signal pin connections for an 18-bit address/data bus connected to 8 UtopiaFIFO devices. Timing is the same as in Figure 6. In this implementation the data bus and SOCR are connected to all UtopiaFIFOs. There is one common $\overline{ENR}$ and separate CLAVR signals for each Utopia FIFO. The CLAVR signals are connected with a pull down resistor. The upstream "switch" loads the address into the selected UtopiaFIFO through the appropriate $\overline{ENR}$ and CLAVR signals. The non-selected UtopiaFIFOs have a tri-stated CLAVR. Initially, no device has an address in its address register. CLAVR is tri-stated and SOCR is LOW. $\overline{ENR}$ is de-asserted. With SOCR LOW and $\overline{ENR}$ asserted, with no current data transfer, the selected UtopiaFIFO will proceed to load the address into its register and evaluate CLAVR. When a complete cell can be written, the CLAVR is set HIGH.

The upstream system will evaluate the CLAVR. With a HIGH CLAVR, and $\overline{ENR}$ LOW, data is written into the FIFO with SOCR HIGH for the first word written into the FIFO. Subsequent $\overline{ENR}$ assertions will load the remaining words of the cell into the FIFO. If CLAVR is HIGH prior to the last word written, and the next cell destination is the same, continuous cell transfer can occur. The $\overline{ENR}$ stays LOW and the SOCR signal indicates data, not an address, is on the bus. After the cell is transferred, if a new FIFO is to be selected (same or different UtopiaFIFO), the SOCR stays LOW while $\overline{ENR}$ is asserted. Once the newly selected FIFO can accept a cell,

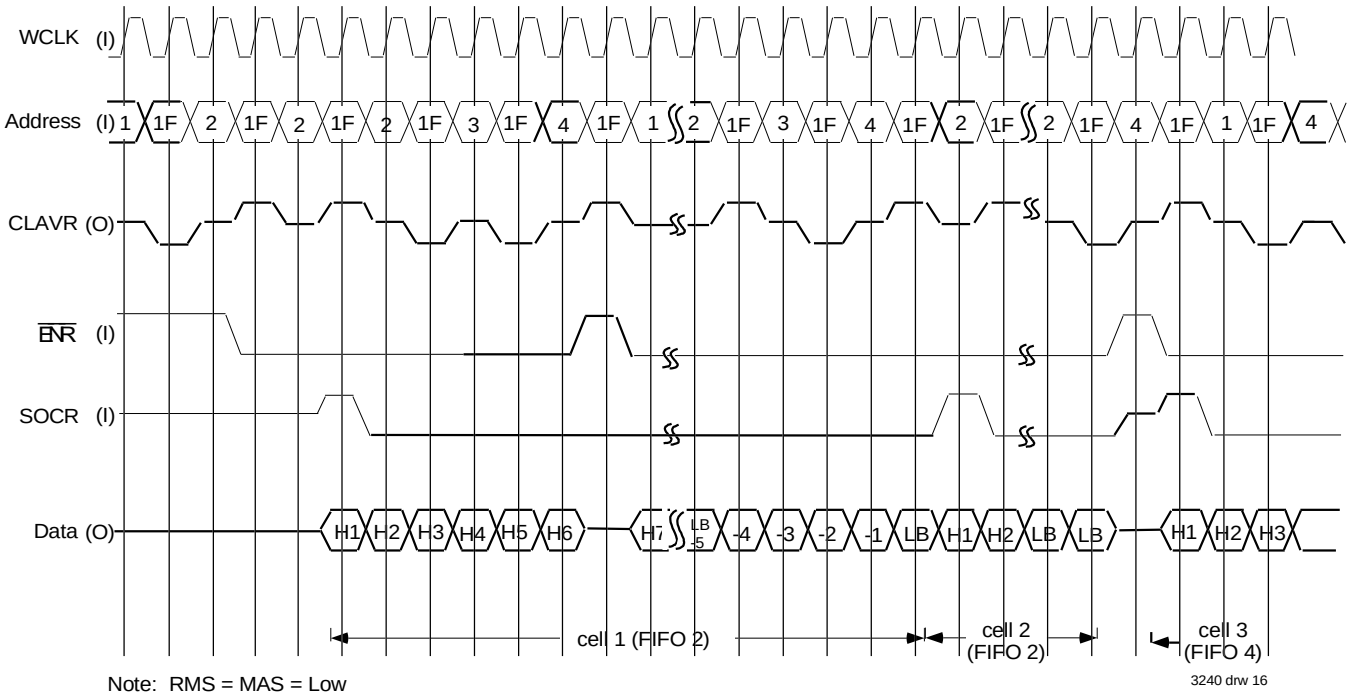


Figure 13. Out-Band Routing, Multicast Mode

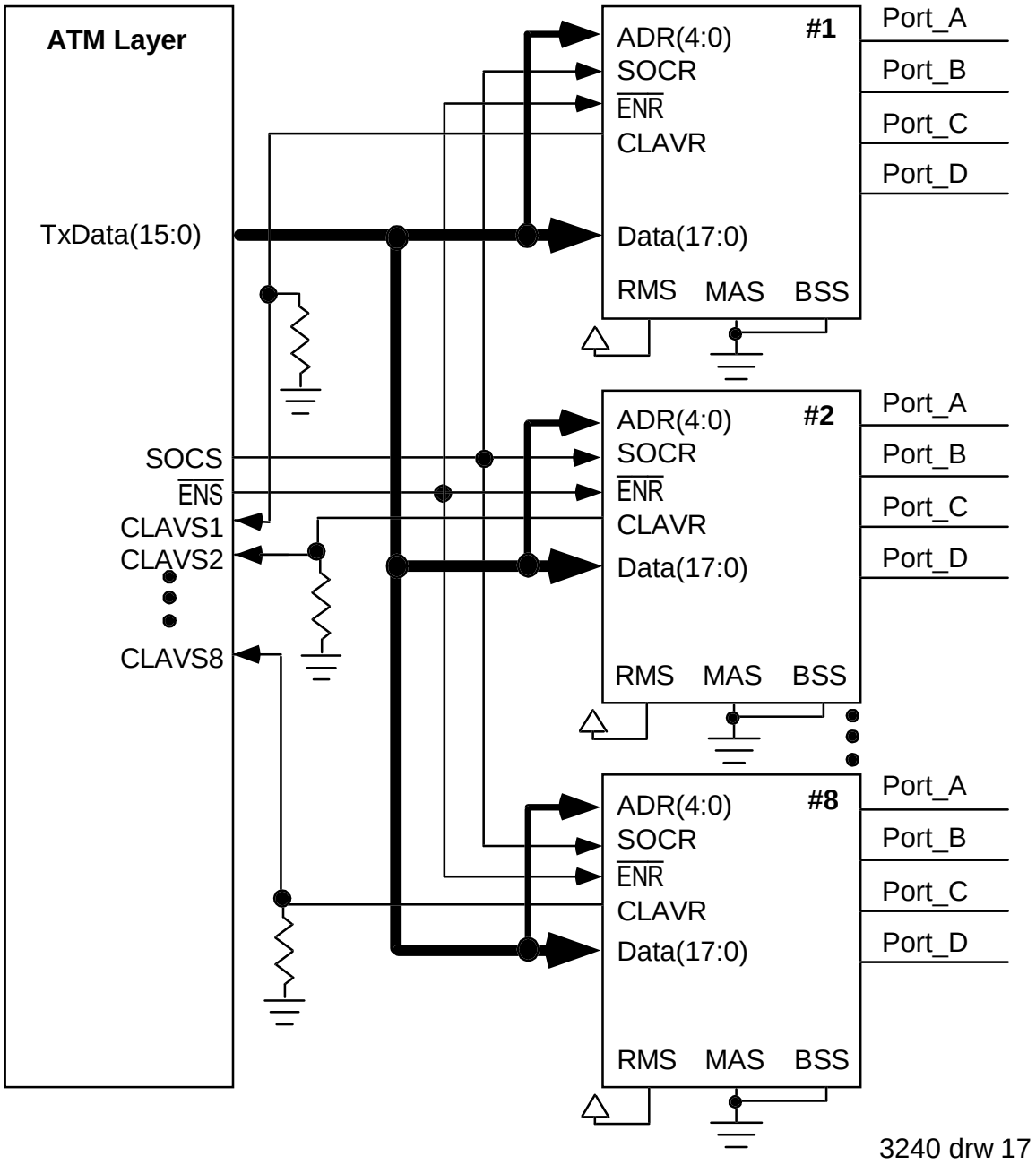


Figure 14. In-Band Routing, Building Block Mode (Singlecast)

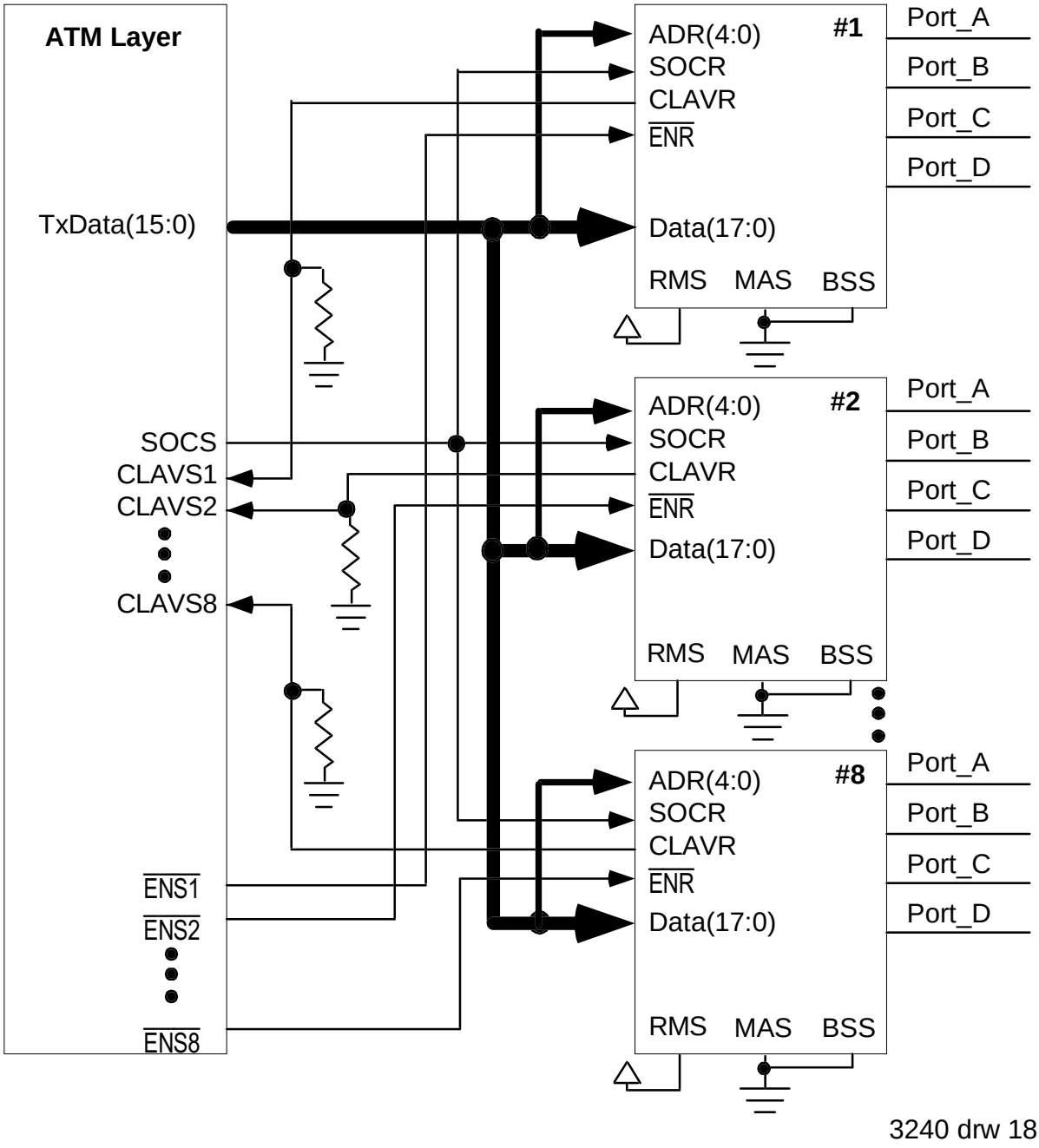


Figure 15. In-Band Routing, Building Block Mode (Multicast System)

the CLAVR is asserted. On the next clock cycle, SOCR goes HIGH to indicate the start of the next cell. Changing FIFO destinations result in only a one clock cycle delay.

MULTICAST OPERATION

Configuration: RMS = "1" indicates in-band routing.
MAS = "1" indicates multicast mode.
BSS = "0" 18 bit operation

Operation in this mode is similar to single device mode. Data/signal connections are shown in Figure 15 and timing is shown in Figure10. In this implementation, these are separate $\overline{ENR}$ signals. With SOCR and $\overline{ENR}$ inactive and no current cell transfer, asserting $\overline{ENR}$ notifies each device the current word is an address. For selected devices, those with cell space available in all FIFOs have a HIGH CLAVR. If one or more selected FIFOs in a given UtopiaFIFO do not have room, CLAVR is set LOW.

As shown in Figure 10, and described above, continuous cell transfer can occur with the same combination of FIFO destinations. With a change in FIFO destinations, only a minimum of one cycle delay will occur.

OUT-BAND ROUTING
SINGLE DEVICE DESTINATION (NO MULTICAST)

Configuration: RMS = "0" indicates out-band routing.
MAS = "0" indicates no multicast mode.
BSS = "0" 18 bit operation

To select from up to eight UtopiaFIFOs, connect address/data lines as shown in Figure 16. There is one $\overline{ENR}$ and multiple CLAVR signals (one per each UtopiaFIFO). The address bus is common to all UtopiaFIFOs. The timing is the same as in Figure 11. Once the current cell transfer is completed, a new $\overline{ENR}$ signal and address will switch data transfer to the new destination. By changing destinations, there is a one cycle delay as $\overline{ENR}$ must be de-asserted to select the new location. The address is loaded on a de-asserted $\overline{ENR}$ signal. If the selected device has space for an entire cell, it asserts CLAVR HIGH. All non-selected devices CLAVR signals are tri-stated. When the selected FIFO has a complete cell available, the asserted CLAVR informs the upstream system it can send data. On the next clock cycle, $\overline{ENR}$ asserts and data is placed on the data bus and SOCR is asserted for the first word of data.

"Polling" of new address locations can occur during the current cell transfer. However, only one Utopia FIFO device can be polled at a time as the address bus is common to all devices. To "poll" non-selected devices will require separate $\overline{ENR}$ signals (one per Utopia FIFO) as well as separate CLAVR lines to the switch.

MULTICAST OPERATION

Configuration: RMS = "0" indicates out-band routing.
MAS = "1" indicates multicast mode.
BSS = "0" 18 bit operation

In this case any combination of the four output FIFOs can receive the same cell and the combination can vary among the individual Utopia devices. Figure 17 shows the data/address connections. In this mode RMS and MAS are both set LOW. The timing is the same for the single device implementation. Each UtopiaFIFO, in turn, has the FIFO multicast destination(s) loaded in the address registers; the CLAVR signal is evaluated for cell availability. Once all desired location CLAVR signals are known and all locations are available, the switch can send data to all UtopiaFIFOs. Data is transferred upon assertion of $\overline{ENR}$ (only to those selected devices) and SOCR with the data on the address bus. At the end of a given cell transfer, if the same set of destinations are used, continuous transfer with no latency, can take place. For a new set of cell destinations, there is a one cycle delay for each selected UtopiaFIFO; if for example, four of the eight devices involve cell destinations, each device must be programmed separately. A set of address enables are loaded into each device on a asserted $\overline{ENR}$ value. Each device evaluates the availability of the selected FIFO(s) and sends an appropriate CLAVR signal.

Polling of all UtopiaFIFOs (both selected and non-selected) during cell transfer can take place. For those non-selected UtopiaFIFOs, a LOW $\overline{ENR}$ signal with a new address combination, with SOCR LOW will be evaluated and CLAVR set accordingly. As a current cell transfer is taking place, no new asserted SOCR (common to all devices) will occur. The absence of a HIGH SOCR notifies the device not to load data. For the currently selected UtopiaFIFOs, if the address is changed to poll a new combination, the current cell

destination(s) will not be altered. If the next cell destination(s) are the same as the current one, this polling address will not change these destination(s); thus, continuous cell transfer can still occur despite the on-going polling.

BUILDING BLOCK IMPLEMENTATION:
36-BIT INPUT BUS

Input data buses greater than 18-bits can be utilized with the UtopiaFIFO. Figure 18 shows how to direct a 36-bit bus to multiple UtopiaFIFOs (multicast mode). For each of the UtopiaFIFO destinations, two devices are used. The 36-bit bus is split up into 8 4-bit streams plus parity bits. As shown in Figure 20, the data bits D0-D3 remain in these positions. Data bits D4-D7 become D18-21, parity bit D8 remains in D8, etc. The "new" bits D0-D17 are directed to the UtopiaFIFO "Bank A" which is set as a master. The "new" bits D18-D35 are directed to the UtopiaFIFO "Bank B" which is set as a slave. This rearranging of data assures that upon reading of the output

data that the data will be in order. The SOCR signal is directed to all UtopiaFIFOs and there are separate $\overline{ENR}$ and CLAVR signals for each pair of UtopiaFIFOs. For a singlecast destination, the implementations can be simplified (Figure 20). Here only one $\overline{ENR}$ is used and all CLAVR signals tied together with a pull down register.

Upon writing the 36-bit data bus into the two banks of UtopiaFIFOs, the first byte of the cell will load its lower bits to the master (low nibble position) and the upper bits into the slave (lower nibble position). On the same cycle the second byte of data will load in the same way except the nibbles will be placed in the high nibble positions. The first and second bytes parity bit is also written. Still on the same cycle, this procedure is repeated for the third and forth bytes (and their respective parity bits).

To read data from the two banks of UtopiaFIFOs, one device is set as the Master (MSE HIGH) and the other bank is set as a slave (MSE LOW). The output from each device is set to "nibble mode" by setting BNE LOW. The 8-bit output bus sent to the downstream system (Utopia Level I compliant) is composed of a 4-bit "nibble" (Q0-3) from each bank plus the "optional" parity (Q8) bit (see Figure 21). The output data bits Q4-6 are left open. The Q7 data bit from each of the master device output FIFOs is an output which feeds into the respective slave FIFO's $\overline{ENS}$ signal (which in slave mode is an input signal). The CLAVS signal from the downstream system is directed to both master and slave devices. The $\overline{ENS}$ and SOCS from the master device are outputs to the downstream system. The SOCS from the slave is left open.

With this configuration, output data from both UtopiaFIFOs will be synchronized. Figure 22 shows the output timing. Once the downstream system can accept a complete cell, CLAVS is asserted to both master and slave devices. The master device recognizes CLAVS and once it has a complete cell available to send, it asserts Q7 LOW. Q7 (master) is feed into the slave $\overline{ENS}$ pin; only in the slave mode is the $\overline{ENS}$ an input. The master device will wait one clock cycle, then asserts $\overline{ENS}$ and loads the first nibble in Q0-3. SOCS (master) is asserted during this first data nibble of the cell. The slave, recognizes a HIGH Q7 from the master, and loads its first nibble of data on the next clock cycle. The "optional" parity bit (Q8) will be placed on Q8 in an alternating fashion starting with the master. The use of an external quick switch will prevent Q8 bus contention between master and slave. The Q7 bit and $\overline{ENS}$ signal from the master will stay asserted during the transfer of the current cell. Nibbles from both devices are placed on the data bus. The parity bit alternates between the two devices until cell transfer completion.

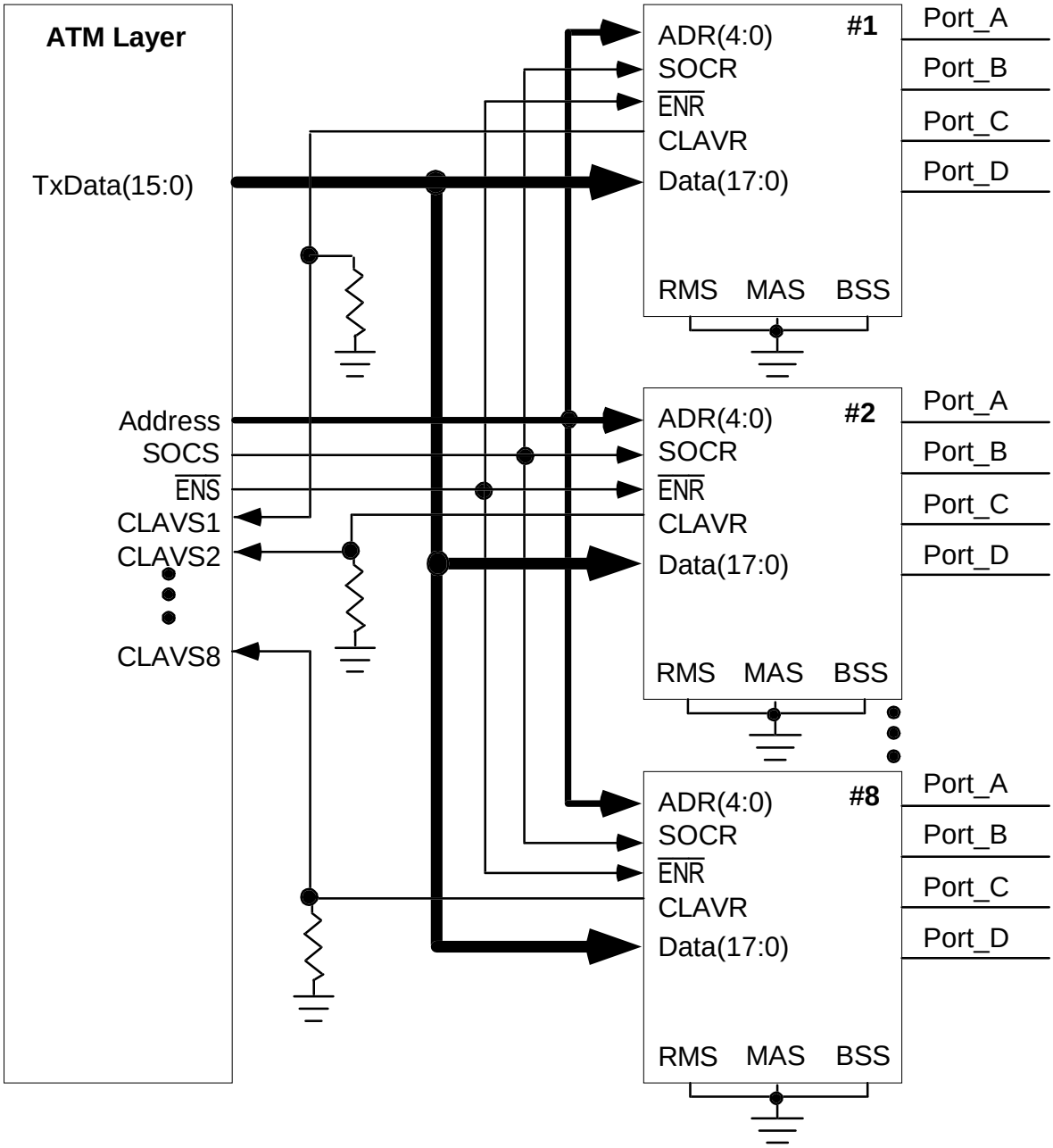
Once cell transfer is complete, a new cell, if available, can be transferred in a continuous fashion. For this constant transfer of data, the CLAVS signal must be asserted no later than the second to last byte to be read. The CLAVS will be evaluated at this point; if HIGH, the master will determine if a second complete cell is available. If a complete cell is present, Q7 (master) will remain LOW and on the following cycle will place data on the Q0-3 data bus with $\overline{ENS}$ asserted and SOCS HIGH for the first nibble. The slave will evaluate Q7 (master) and place the first nibble of the second cell on the bus on the following cycle.

Once CLAVS is HIGH, $\overline{ENS}$ (master) will not de-assert until a given cell is transferred. $\overline{ENS}$ will remain asserted until either no new asserted CLAVS signal or no new complete cell available. During a cell transfer and prior to the second to last byte transfer, the CLAVS signal is a don't care.

For input buses larger than 32-bit, multiple banks of UtopiaFIFO s can be utilized. For a 64-bit input bus, one device is set as a master and three set as slaves with the appropriate direction of the data bus on the input side. The UtopiaFIFOs have the current drive capabilities to drive several slave devices.

CELL LENGTH ERROR RECOVERY

After the start of cell signal (SOCR) is received, future SOCR assertions prior to the end of current cell transfers are ignored. A counter keeps track of byte transfers. If a "short cell" occurs (where a SOCR signal is received prior to the end of cell transfer) the new SOCR is ignored and the data from the next incoming cell is loaded into the existing "short cell" until it is filled to normal cell size. Any additional bytes from the incoming cell are ignored. The short cell is padded by the data from the second cell and the remainder of the second cell is discarded. Recovery occurs on the third incoming cell. If a "long cell" occurs (where the number of bytes exceeds the defined cell size and no new SOCR signal received indicating a new cell) the extra bytes are ignored by the UtopiaFIFO . The FIFO receiving the long cell will wait for a new SOCR (and assertion of $\overline{ENR}$ and CLAVR) before continuing data transfer.



3240 drw 19

Figure 16. Out-Band Routing, Building Block Mode (Singlecast)

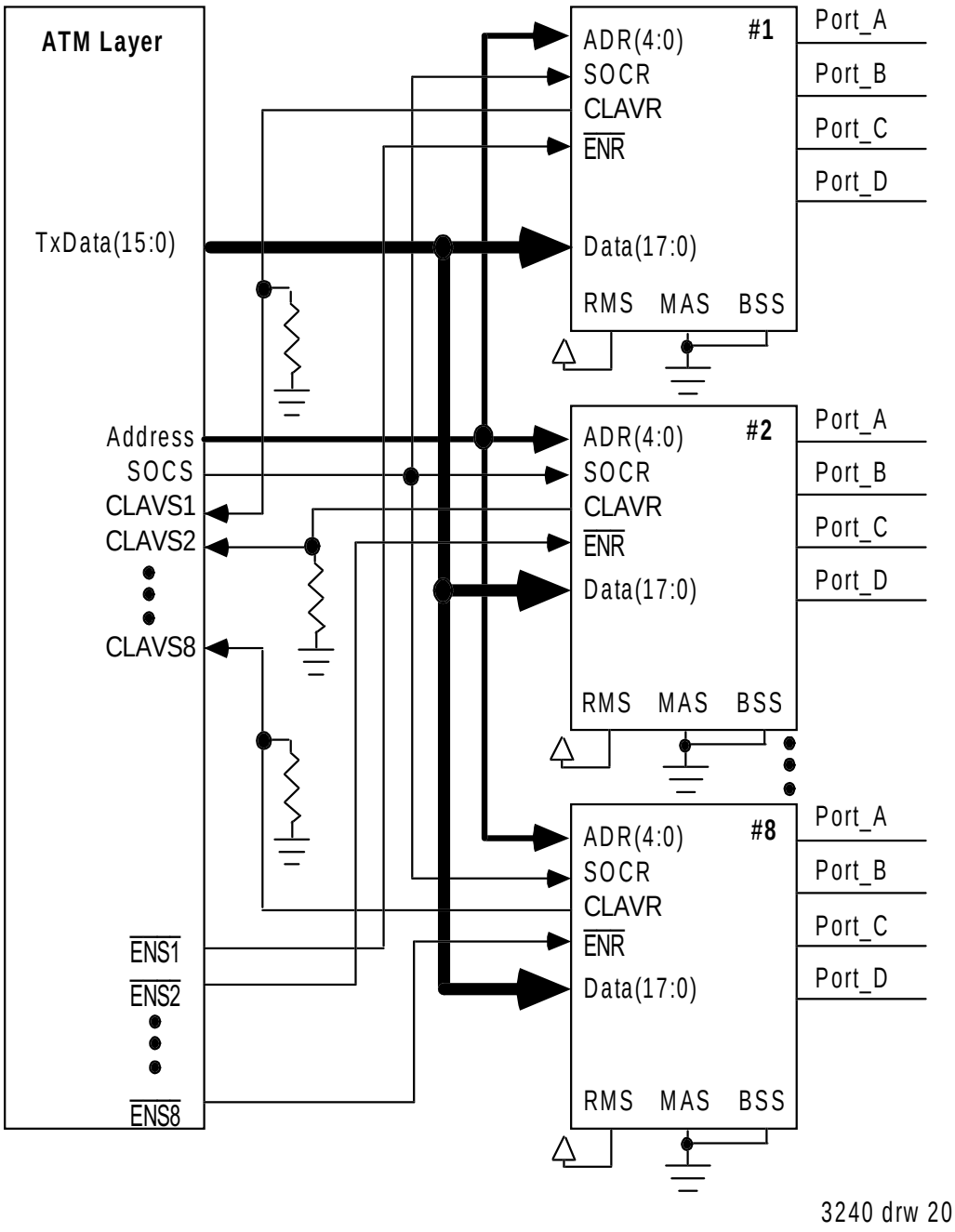


Figure 17. Out-Band Routing, Building Block Mode Multicast

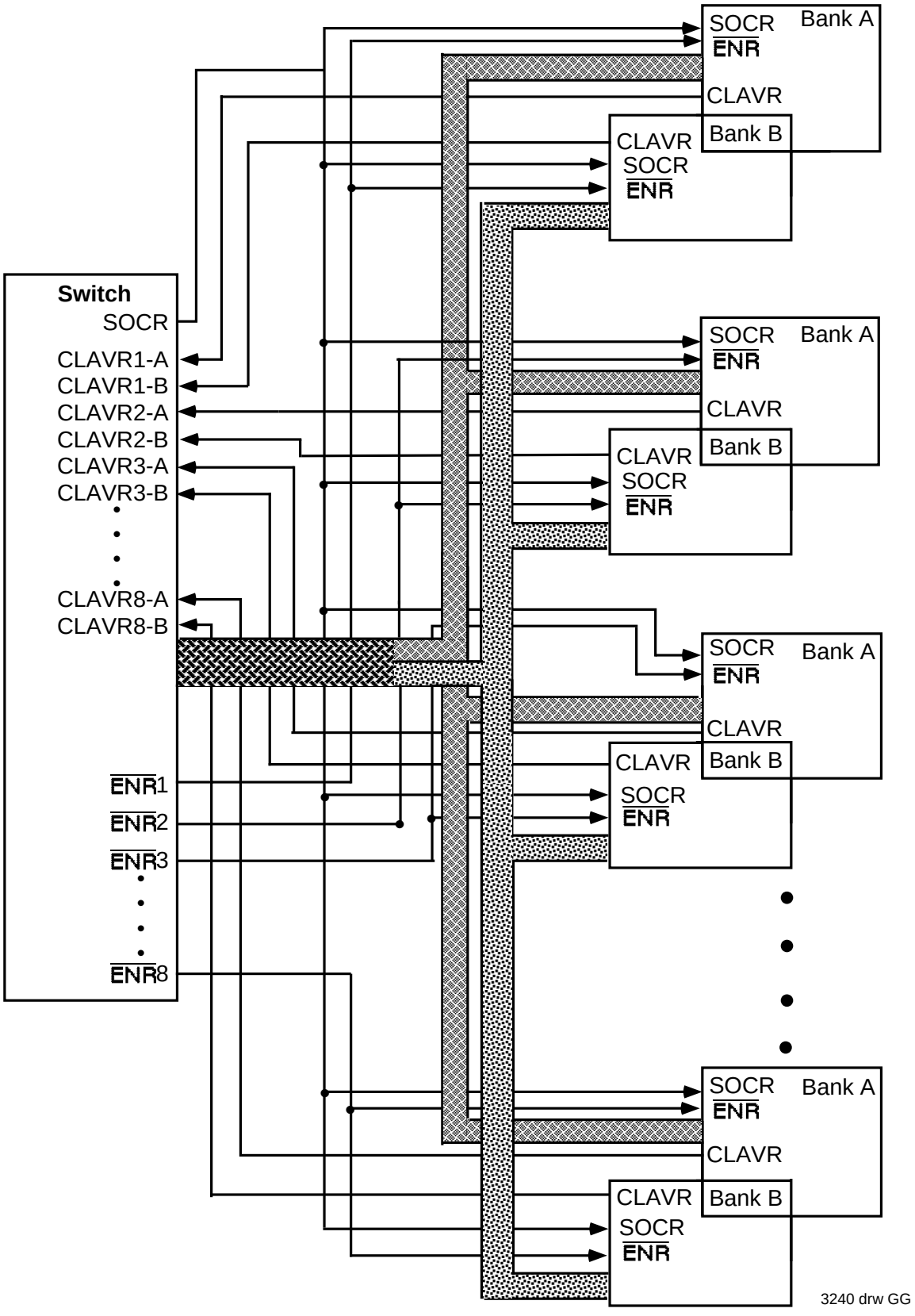


Figure 18. Multicast Mode

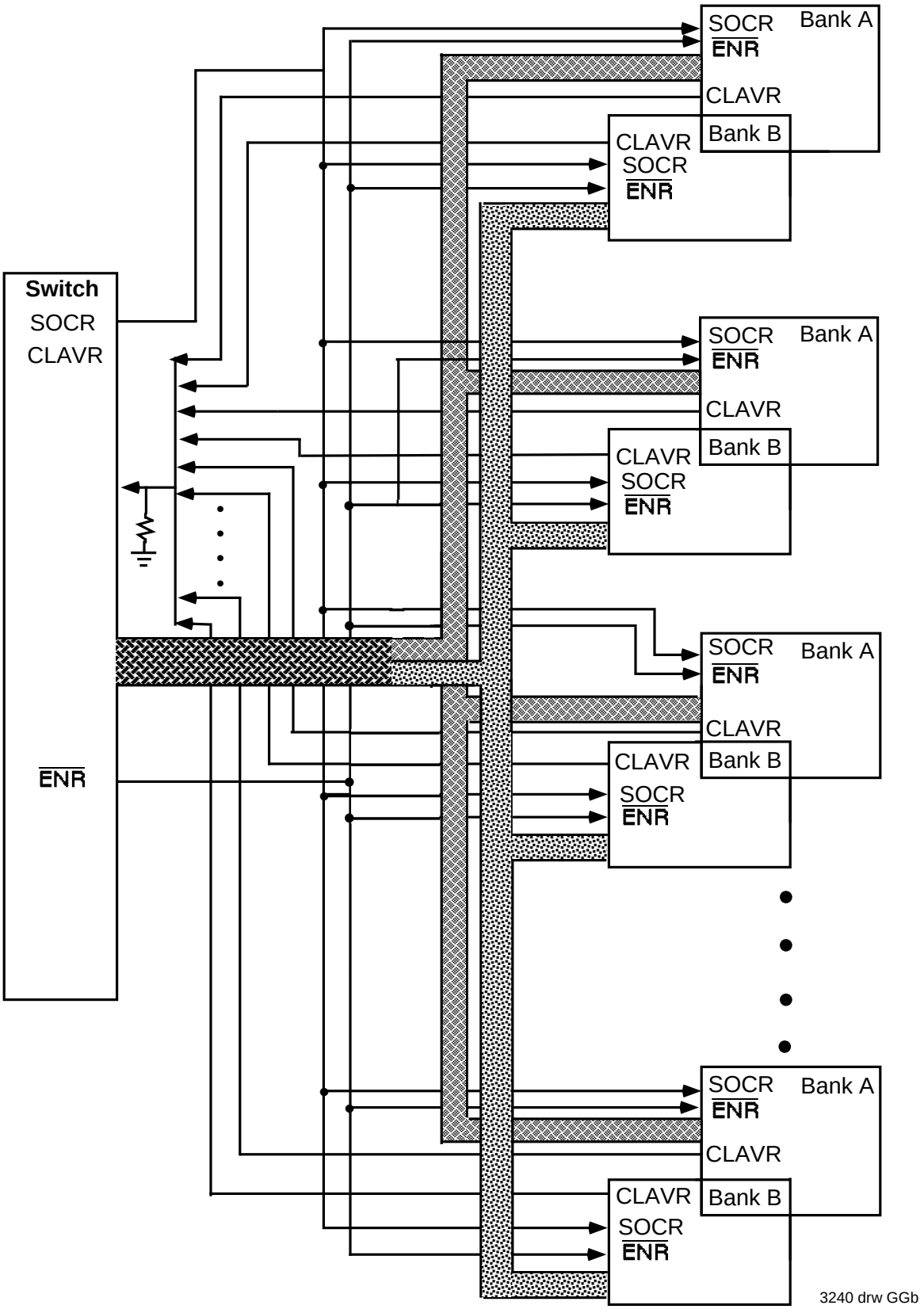


Figure 19. Singlecast Mode

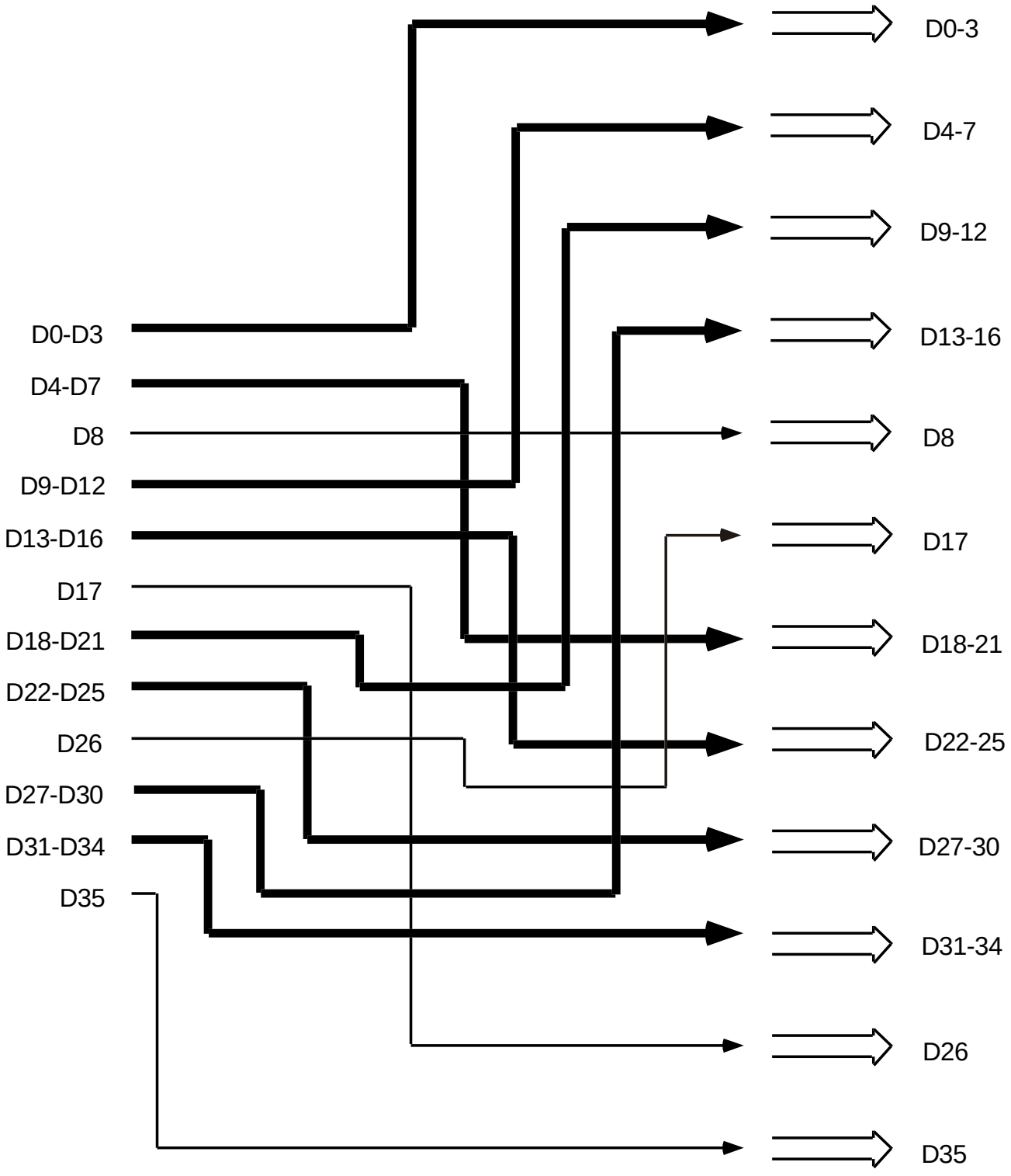


Figure 20. Single Cast Mode

3240 drw 23

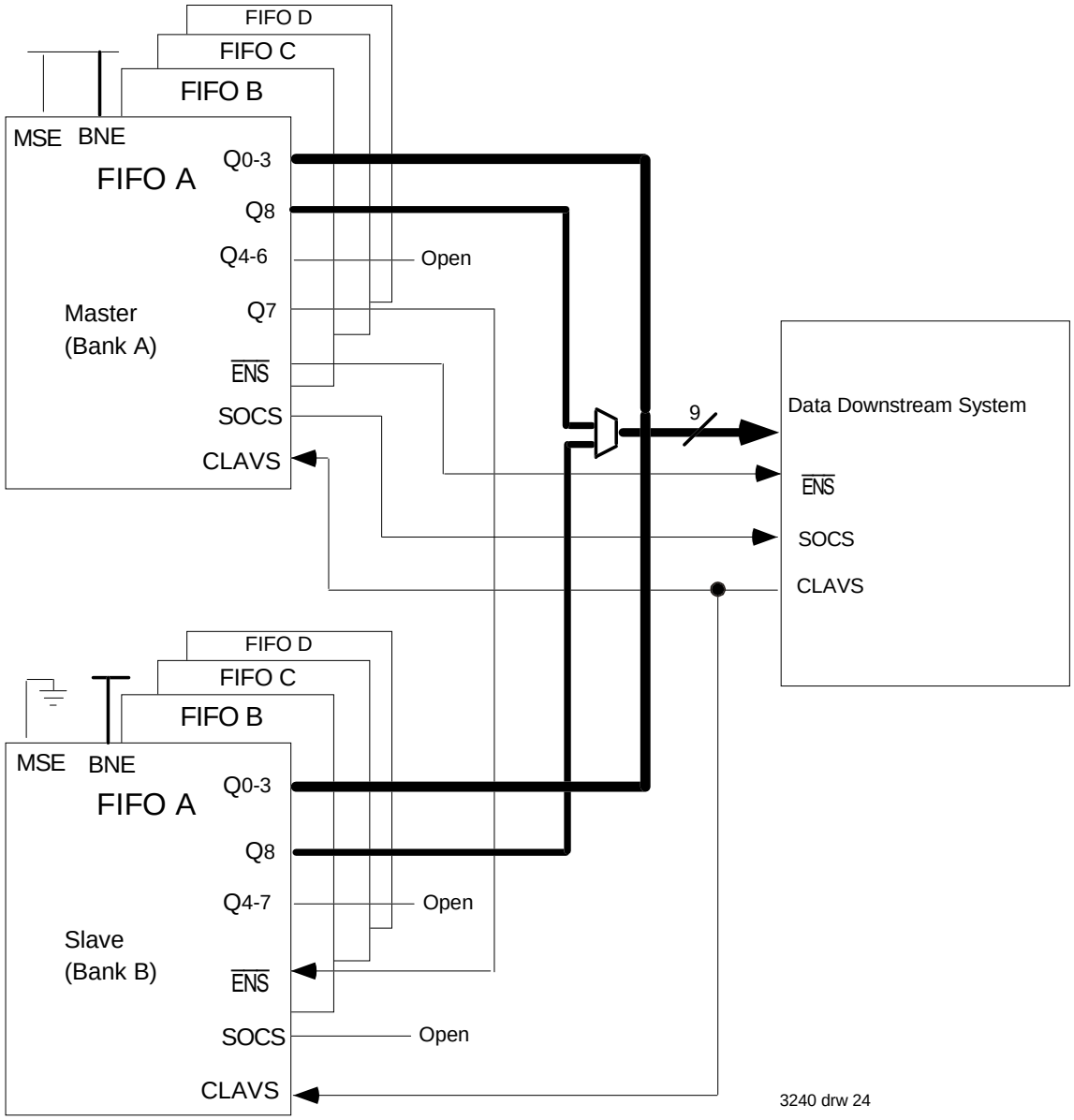
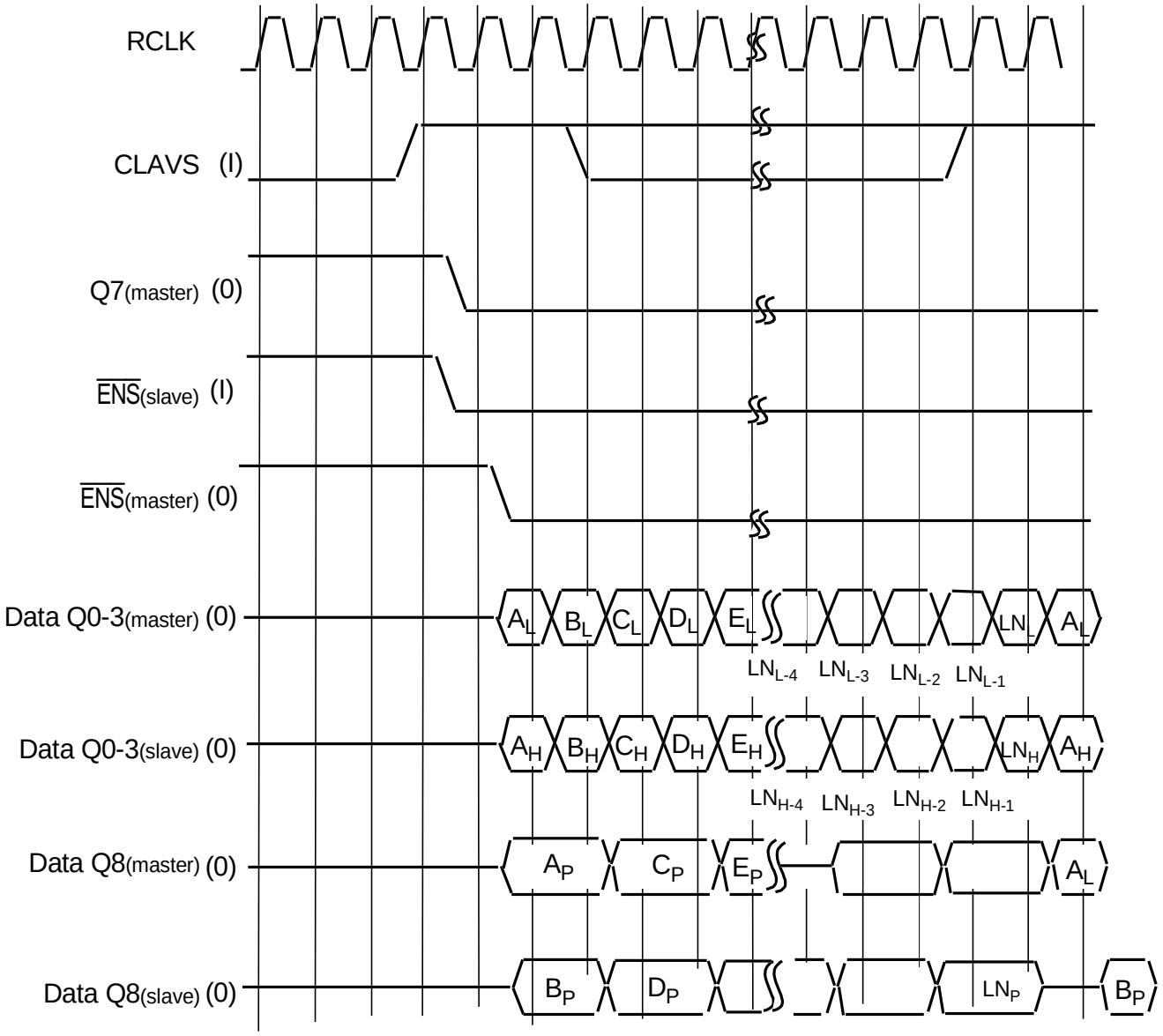


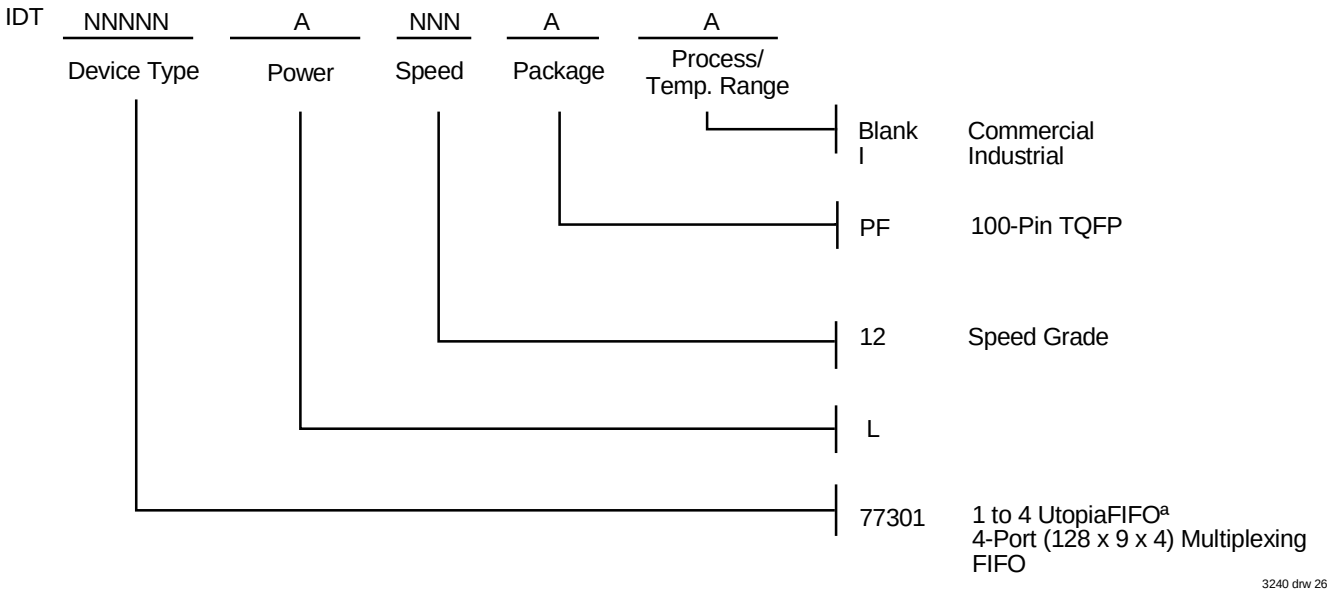
Figure 21. Building Block Implementation with 36-bit Data Bus



3240 drw 25

Figure 22. Building Block Implementation with 36-bit Input Bus Timing

Ordering Information



Datasheet Document History

12/1/95:	Initial Draft
10/31/96:	Added timing diagrams and upgraded to "PRELIMINARY"
11/19/96:	Reworked entire datasheet including text and pin-out.
12/5/96:	Added Sequential Load Diagram for Cell Size and Device ID
6/30/97:	Correct some errors in the first diagram and add the timing specifications.
8/20/97:	Timing specifications added.
1/6/98:	Corrected multiple errors in text, drawings, and timing.
4/15/98:	Corrected in-band and out-band drawings.
2/28/00:	Changed datasheet design format
3/26/01:	Changed Preliminary to Final. In AC Electrical Characteristics Table, changed maximum from 8 to 10 for pins t_{OE} and t_{OH2}.

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