



# STS25NH3LL

## N-CHANNEL 30V - 0.0027Ω - 25A SO-8 STripFET™ III MOSFET FOR DC-DC CONVERSION

PRELIMINARY DATA

TYPE	V <sub>DSS</sub>	R <sub>DS(on)</sub>	I <sub>D</sub>
STS25NH3LL	30 V	< 0.0035Ω	25 A

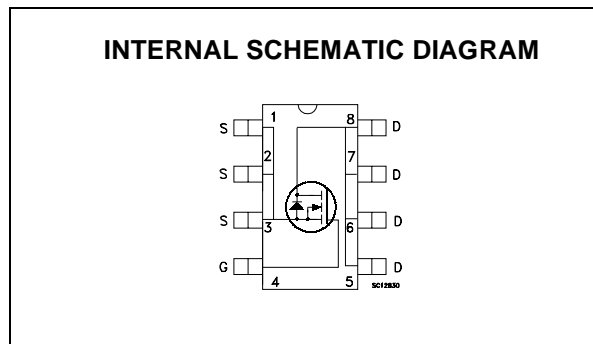
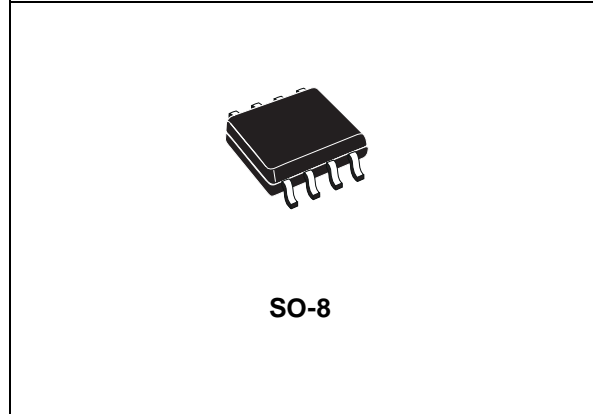
- TYPICAL R<sub>DS(on)</sub> = 0.0027Ω
- OPTIMAL R<sub>DS(ON)</sub> x Q<sub>g</sub> TRADE-OFF @4.5V
- CONDUCTION LOSSES REDUCED
- SWITCHING LOSSES REDUCED
- WORLD INDUSTRY'S LOWEST ON-RESISTANCE

### DESCRIPTION

The **STS25NH3LL** utilizes the latest advanced design rules of ST's proprietary STripFET™ technology. This novel 0.6μ process coupled to unique metallization techniques realizes the most advanced low voltage MOSFET in SO-8 ever produced. It is therefore suitable for the most demanding DC-DC converter applications where high efficiency is to be achieved at high output current.

### APPLICATIONS

- DC-DC CONVERTERS FOR TELECOM AND NOTEBOOK CPU CORE
- SYNCHRONOUS RECTIFIER



### ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V <sub>DS</sub>	Drain-source Voltage (V <sub>GS</sub> = 0)	30	V
V <sub>DGR</sub>	Drain-gate Voltage (R <sub>GS</sub> = 20 kΩ)	30	V
V <sub>GS</sub>	Gate- source Voltage	± 18	V
I <sub>D</sub>	Drain Current (continuous) at T <sub>A</sub> = 25°C Drain Current (continuous) at T <sub>A</sub> = 100°C	25 18	A A
I <sub>DM</sub> (●)	Drain Current (pulsed)	100	A
P <sub>TOT</sub>	Total Dissipation at T <sub>A</sub> = 25°C	3.2	W

(●) Pulse width limited by safe operating area

# STS25NH3LL

## THERMAL DATA

Rthj-amb	(*) Thermal Resistance Junction-ambient Max	47	°C/W
Rthj-lead	Thermal Resistance Junction-leads Max	16	°C/W
T <sub>j</sub>	Max. Operating Junction Temperature	-55 to 175	°C
T <sub>stg</sub>	Storage Temperature		

(\*) When mounted on 1 inch<sup>2</sup> FR4 Board, 2 oz of Cu, t ≤ 10 sec.

## ELECTRICAL CHARACTERISTICS (T<sub>J</sub> = 25 °C UNLESS OTHERWISE SPECIFIED)

OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V <sub>(BR)DSS</sub>	Drain-source Breakdown Voltage	I <sub>D</sub> = 250 μA, V <sub>GS</sub> = 0	30			V
I <sub>DSS</sub>	Zero Gate Voltage Drain Current (V <sub>GS</sub> = 0)	V <sub>DS</sub> = Max Rating V <sub>DS</sub> = Max Rating, T <sub>C</sub> = 125 °C			1 10	μA μA
I <sub>GSS</sub>	Gate-body Leakage Current (V <sub>DS</sub> = 0)	V <sub>GS</sub> = ± 18V			±100	nA

ON (1)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V <sub>GS(th)</sub>	Gate Threshold Voltage	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250μA	1			V
R <sub>DS(on)</sub>	Static Drain-source On Resistance	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 12 A V <sub>GS</sub> = 4.5 V, I <sub>D</sub> = 12 A		0.0027 0.0035	0.0035 0.0050	Ω Ω

DYNAMIC

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
g <sub>fs</sub> (1)	Forward Transconductance	V <sub>DS</sub> = 15V, I <sub>D</sub> = 12 A		30		S
C <sub>iss</sub>	Input Capacitance	V <sub>DS</sub> = 25 V, f = 1 MHz, V <sub>GS</sub> = 0		4450		pF
C <sub>oss</sub>	Output Capacitance			655		pF
C <sub>rss</sub>	Reverse Transfer Capacitance			50		pF

**ELECTRICAL CHARACTERISTICS (CONTINUED)**

**SWITCHING ON**

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on Delay Time	$V_{DD} = 15\text{ V}$ , $I_D = 12.5\text{ A}$ $R_G = 4.7\Omega$ , $V_{GS} = 10\text{ V}$ (see test circuit, Figure 1)		18		ns
$t_r$	Rise Time			50		ns
$Q_g$ $Q_{gs}$ $Q_{gd}$	Total Gate Charge Gate-Source Charge Gate-Drain Charge	$V_{DD} = 15\text{ V}$ , $I_D = 25\text{ A}$ , $V_{GS} = 5\text{ V}$ (see test circuit, Figure 2)		32 12.5 10	43	nC nC nC

**SWITCHING OFF**

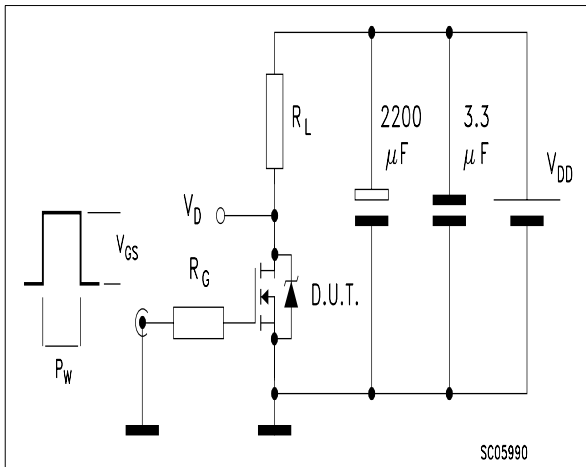
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(off)}$	Turn-off-Delay Time	$V_{DD} = 15\text{ V}$ , $I_D = 12.5\text{ A}$ , $R_G = 4.7\Omega$ , $V_{GS} = 10\text{ V}$ (see test circuit, Figure 1)		75		ns
$t_f$	Fall Time			8		ns

**SOURCE DRAIN DIODE**

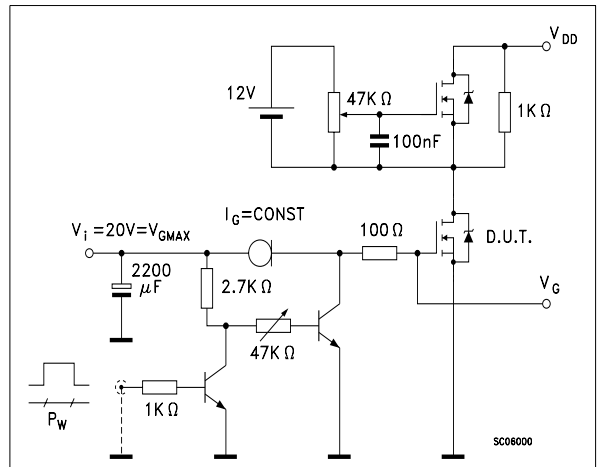
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$I_{SD}$	Source-drain Current				25	A
$I_{SDM(2)}$	Source-drain Current (pulsed)				100	A
$V_{SD(1)}$	Forward On Voltage	$I_{SD} = 25\text{ A}$ , $V_{GS} = 0$			1.2	V
$t_{rr}$ $Q_{rr}$ $I_{RRM}$	Reverse Recovery Time Reverse Recovery Charge Reverse Recovery Current	$I_{SD} = 25\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$ , $V_{DD} = 25\text{ V}$ , $T_j = 150^\circ\text{C}$ (see test circuit, Figure 3)		32 34 2.1		ns nC A

Note: 1. Pulsed: Pulse duration = 300  $\mu\text{s}$ , duty cycle 1.5 %.  
2. Pulse width limited by safe operating area.

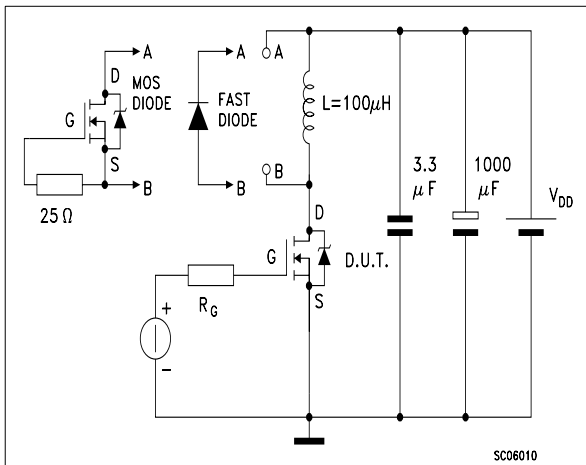
**Fig. 1: Switching Times Test Circuit For Resistive Load**



**Fig. 2: Gate Charge test Circuit**

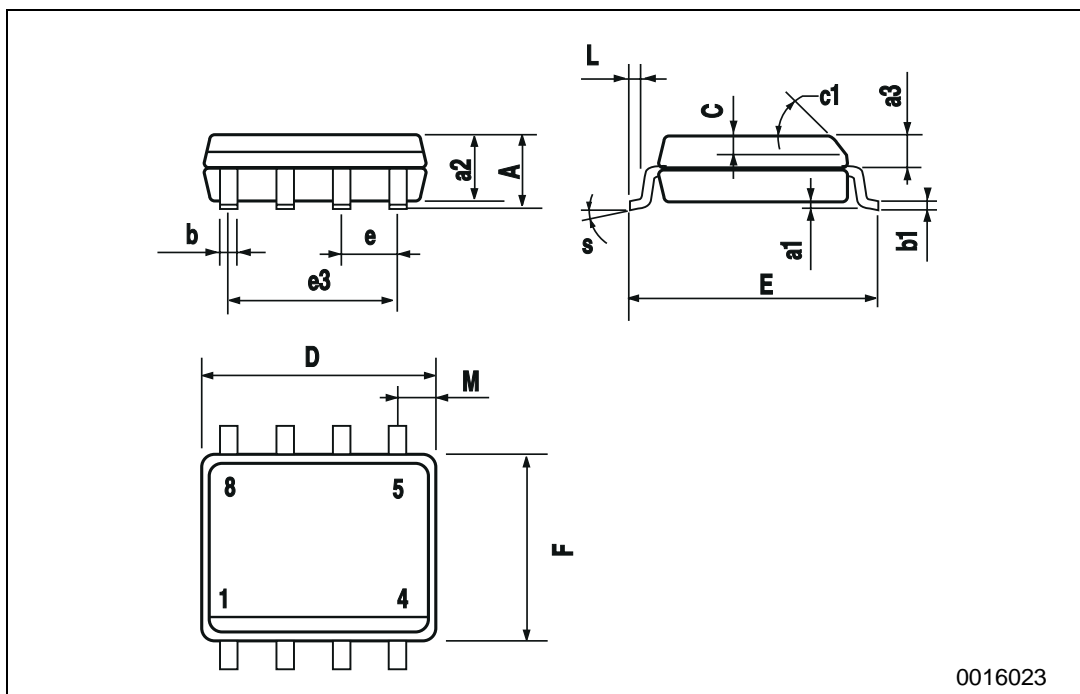


**Fig. 3: Test Circuit For Diode Recovery Behaviour**



**SO-8 MECHANICAL DATA**

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.75			0.068
a1	0.1		0.25	0.003		0.009
a2			1.65			0.064
a3	0.65		0.85	0.025		0.033
b	0.35		0.48	0.013		0.018
b1	0.19		0.25	0.007		0.010
C	0.25		0.5	0.010		0.019
c1	45 (typ.)					
D	4.8		5.0	0.188		0.196
E	5.8		6.2	0.228		0.244
e		1.27			0.050	
e3		3.81			0.150	
F	3.8		4.0	0.14		0.157
L	0.4		1.27	0.015		0.050
M			0.6			0.023
S	8 (max.)					



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