Low Voltage / Low Power CMOS 16-bit Micro-controller

TMP93PS40F
TMP93PS40DF

1. OUTLINE AND DEVICE CHARACTERISTICS

The TMP93PS40 is OTP type MCU which includes 64K byte One-time PROM. Using the adapter-socket (BM11109 or BM11129), you can write and verify the data for the TMP93PS40.

TMP93PS40 has the same pin-assignment with TMP93CM40 / CS40 (Mask ROM type).

Writing the program to Built-in PROM, the TMP93PS40 operates as the same way as the TMP93CS40.

There is a difference in ROM capacity between TMP93PS40 (64K-byte) and the TMP93CM40 (32K-byte). Please pay attention to the difference of memory maps.

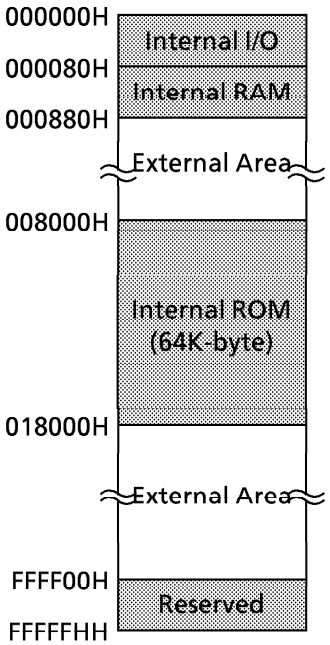
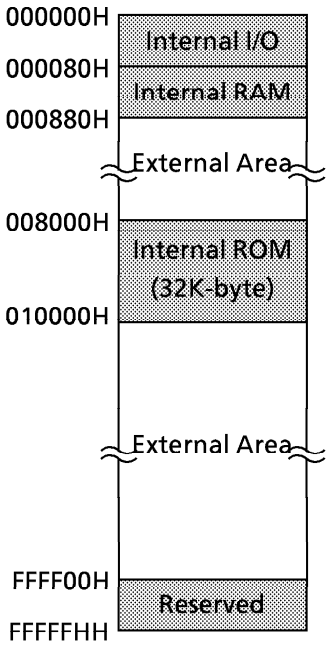


Fig.1.1 Memory map of TMP93CS40 / PS40



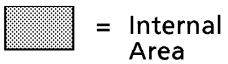


Fig.1.2 Memory map of TMP93CM40

MCU	ROM	RAM	Package	Adapter Socket
TMP93PS40F	OTP 64K byte	2K-byte	QFP100-P-1414-0.50	BM11109
TMP93PS40DF			QFP100-P-1414-0.50C	BM11129

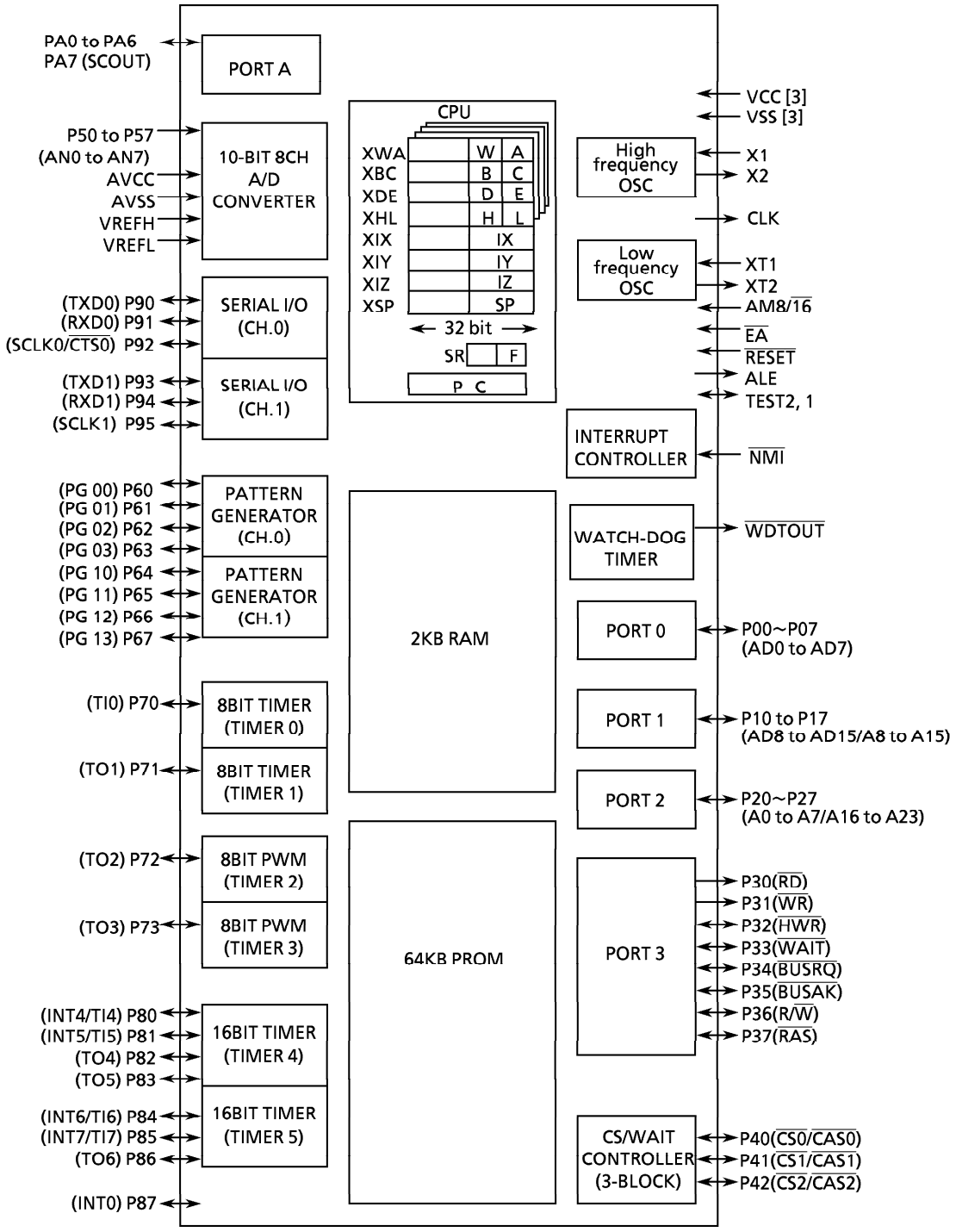


Figure 1.3 TMP93PS40 block diagram

2. PIN ASSIGNMENT AND FUNCTIONS

The assignment of input / output pins for TMP93PS40, their name and outline functions are described below.

2.1 Pin Assignment

Figure 2.1 shows pin assignment of TMP93PS40.

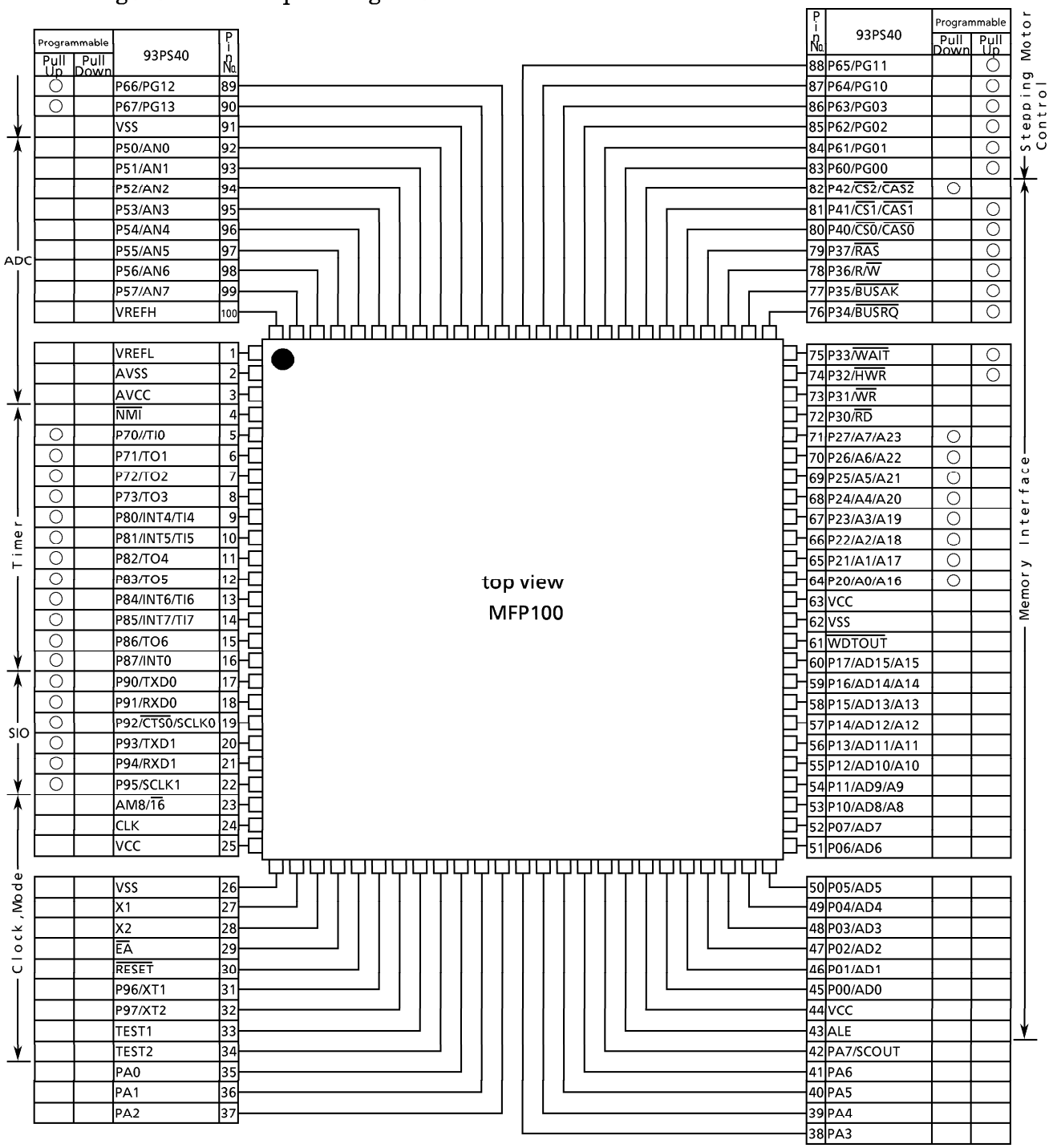


Figure 2.1 Pin Assignment (100-pin MFP)

2.2 Pin Names and Functions

(1) Pin function of TMP93PS40 in MCU mode.

Table 2.2 (1) Name and function MCU mode

Pin name	Number of pins	I/O	Functions
P00 to P07 AD0 to AD7	8	I/O Tri-state	Port 0: I/O port that allows I/O to be selected on a bit basis Address/data (lower): 0 to 7 for address/data bus
P10 to P17 AD8 to AD15 A8 to A15	8	I/O Tri-state Output	Port 1: I/O port that allows I/O to be selected on a bit basis Address data (upper): 8 to 15 for address/data bus Address: 8 to 15 for address bus
P20 to P27 A0 to A7 A16 to A23	8	I/O Output Output	Port 2: I/O port that allows selection of I/O on a bit basis (with pull-down resistor) Address: 0 to 7 for address bus Address: 16 to 23 for address bus
P30 $\overline{RD}$	1	Output Output	Port 30: Output port Read: Strobe signal for reading external memory
P31 $\overline{WR}$	1	Output Output	Port 31: Output port Write: Strobe signal for writing data on pins AD0 to 7
P32 $\overline{HWR}$	1	I/O Output	Port 32: I/O port (with pull-up resistor) High write: Strobe signal for writing data on pins AD8 to 15
P33 $\overline{WAIT}$	1	I/O Input	Port 33: I/O port (with pull-up resistor) Wait: Pin used to request CPU bus wait
P34 $\overline{BUSRQ}$	1	I/O Input	Port34: I/O port (with pull-up resistor) Bus request: Signal used to request high impedance for AD0 to 15, A0 - 23, $\overline{RD}$, $\overline{WR}$,$\overline{HWR}$, R/$\overline{W}$, $\overline{RAS}$, $\overline{CS0}$, $\overline{CS1}$, and $\overline{CS2}$ pins. (For external DMAC)
P35 $\overline{BUSAK}$	1	I/O Output	Port 35: I/O port (with pull-up resistor) Bus acknowledge: Signal indicating that AD0 to 15, A0 to 23, $\overline{RD}$, $\overline{WR}$,$\overline{HWR}$, R/$\overline{W}$, $\overline{RAS}$, $\overline{CS0}$, $\overline{CS1}$, and $\overline{CS2}$ pins are at high impedance after receiving BUSRQ. (For external DMAC)
P36 R/$\overline{W}$	1	I/O Output	Port 36: I/O port (with pull-up resistor) Read/write: 1 represents read or dummy cycle; 0, write cycle.
P37 $\overline{RAS}$	1	I/O Output	Port 37: I/O port (with pull-up resistor) Row address strobe: Outputs RAS strobe for DRAM.
P40 $\overline{CS0}$ $\overline{CAS0}$	1	I/O Output Output	Port 40: I/O port (with pull-up resistor) Chip select 0: Outputs 0 when address is within specified address area. Column address strobe 0: Outputs CAS strobe for DRAM when address is within specified address area.

Note : With the external DMA controller, this device's built-in memory or built-in I/O cannot be accessed using the $\overline{BUSRQ}$ and $\overline{BUSAK}$ pins.

Pin name	Number of pins	I/O	Functions
P41 $\overline{CS1}$ $\overline{CAS1}$	1	I/O Output Output	Port 41: I/O port (with pull-up resistor) Chip select 1: Outputs 0 if address is within specified address area. Column address strobe 1: Outputs $\overline{CAS}$ strobe for DRAM if address is within specified address area.
P42 $\overline{CS2}$ $\overline{CAS2}$	1	I/O Output Output	Port 42: I/O port (with pull-down resistor) Chip select 2: Outputs 0 if address is within specified address area. Column address strobe 2: Outputs $\overline{CAS}$ strobe for DRAM if address is within specified address area.
P50 to P57 AN0 to AN7	8	Input Input	Port 5: Input port Analog input: Input to A/D converter
VREFH	1	Input	Pin for reference voltage input to A/D converter (H)
VREFL	1	Input	Pin for reference voltage input to A/D converter (L)
P60 to P63 PG00 to PG03	4	I/O Output	Ports 60 - 63: I/O ports that allow selection of I/O on a bit basis (with pull-up resistor) Pattern generator ports: 00 - 03
P64 to P67 PG10 to PG13	4	I/O Output	Ports 64 - 67: I/O ports that allow selection of I/O on a bit basis (with pull-up resistor) Pattern generator ports: 10 - 13
P70 TI0	1	I/O Input	Port 70: I/O port (with pull-up resistor) Timer input 0: Timer 0 input
P71 TO1	1	I/O Output	Port 71: I/O port (with pull-up resistor) Timer output 1: Timer 0 or 1 output
P72 TO2	1	I/O Output	Port 72: I/O port (with pull-up resistor) PWM output 2: 8-bit PWM timer 2 output
P73 TO3	1	I/O Output	Port 73: I/O port (with pull-up resistor) PWM output 3: 8-bit PWM timer 3 output
P80 TI4 INT4	1	I/O Input Input	Port 80: I/O port (with pull-up resistor) Timer input 4: Timer 4 count / capture trigger signal input Interrupt request pin 4: Interrupt request pin with programmable rising / falling edge
P81 TI5 INT5	1	I/O Input Input	Port 81: I/O port (with pull-up resistor) Timer input 5: Timer 4 count / capture trigger signal input Interrupt request pin 5: Interrupt request pin with rising edge
P82 TO4	1	I/O Output	Port 82: I/O port (with pull-up resistor) Timer output 4: Timer 4 output pin
P83 TO5	1	I/O Output	Port 83: I/O port (with pull-up resistor) Timer output 5: Timer 4 output pin

Pin name	Number of pins	I/O	Functions
P84 TI6 INT6	1	I/O Input Input	Port 84: I/O port (with pull-up resistor) Timer input 6: Timer 5 count / capture trigger signal input Interrupt request pin 6: Interrupt request pin with programmable rising / falling edge
P85 TI7 INT7	1	I/O Input Input	Port 85: I/O port (with pull-up resistor) Timer input 7: Timer 5 count / capture trigger signal input Interrupt request pin 7: Interrupt request pin with rising edge
P86 TO6	1	I/O Output	Port 86: I/O port (with pull-up resistor) Timer output 6: Timer 5 output pin
P87 INT0	1	I/O Input	Port 87: I/O port (with pull-up resistor) Interrupt request pin 0: Interrupt request pin with programmable level / rising edge
P90 TXD0	1	I/O Output	Port 90: I/O port (with pull-up resistor) Serial send data 0
P91 RXD0	1	I/O Input	Port 91: I/O port (with pull-up resistor) Serial receive data 0
P92 $\overline{CTS0}$ SCLK0	1	I/O Input I/O	Port 92: I/O port (with pull-up resistor) Serial data send enable 0 (Clear to Send) Serial Clock I/O 0
P93 TXD1	1	I/O Output	Port 93: I/O port (with pull-up resistor) Serial send data 1
P94 RXD1	1	I/O Input	Port 94: I/O port (with pull-up resistor) Serial receive data 1
P95 SCLK1	1	I/O I/O	Port 95: I/O port (with pull-up resistor) Serial clock I/O 1
PA0 to PA6	7	I/O	Port A: I/O ports
PA7 SCOUT	1	I/O Output	Port A7: I/O port System Clock Output: Outputs system clock or 1/2 oscillation clock for synchronizing to external circuit.
$\overline{WDTOUT}$	1	Output	Watchdog timer output pin
$\overline{NMI}$	1	Input	Non-maskable interrupt request pin: Interrupt request pin with falling edge. Can also be operated at rising edge by program.
CLK	1	Output	Clock output: Outputs ⌈ System Clock ÷ 2 ⌋ Clock. Pulled-up during reset. can be set to Output Disable for reducing noise.
$\overline{EA}$	1	Input	External access: "1" should be inputted with TMP93PS40.

Pin name	Number of pins	I/O	Functions
AM8 / $\overline{16}$	1	Input	Address Mode: Selects external Data Bus width. (the case of TMP93PS40) "1" should be inputted. The Data Bus Width for external access is set by Chip Select / WAIT Control register, Port 1 Control register.
ALE	1	Output	Address Latch Enable Can be set to Output Disable for reducing noise.
$\overline{\text{RESET}}$	1	Input	Reset: Initializes LSI. (With pull-up resistor)
X1/X2	2	I/O	High Frequency Oscillator connecting pin
XT1 P96	1	Input I/O	Low Frequency Oscillator connecting pin Port 96: I/O port (Open Drain Output)
XT2 P97	1	Output I/O	Low Frequency Oscillator connecting pin Port 97: I/O port (Open Drain Output)
TEST1 / TEST2	2	Output / Input	TEST1 Should be connected with TEST2 pin.
VCC	3		Power supply pin
VSS	3		GND pin (0 V)
AVCC	1		Power supply pin for A/D converter
AVSS	1		GND pin for A/D converter (0 V)

Note : Pull-up / pull-down resistor can be released from the pin by software.

(2) PROM mode

Table 2.2 (2) Name and function of PROM mode

Pin function	Pin number	Input / Output	Function	Pin name (MCU mode)
A7 to A0	8	Input	Memory address of program	P27 to P20
A15 to A8	8	Input		P17 to P10
A16	1	Input		P33
D7 to D0	8	I/O	Memory data of pfogram	P07 to P00
$\overline{CE}$	1	Input	Chip enable	P32
$\overline{OE}$	1	Input	Output control	P30
$\overline{PGM}$	1	Input	Program control	P31
VPP	1	Power supply	12.75 V / 5 V (Power supply of program)	$\overline{EA}$
VCC	4	Power supply	6.25 V / 5 V	VCC, AVCC
VSS	4	Power supply	0 V	VSS, AVSS
Pin function	Pin number	Input / Output	Disposal of pin	
P34	1	Input	Fix to low level (security pin)	
$\overline{RESET}$	1	Input	Fix to low level (PROM mode)	
CLK	1	Input		
ALE	1	Output	Open	
X1	1	Input	Crystal	
X2	1	Output		
P42 to P40 P37 to P35 AM8 / $\overline{16}$	7	Input	Fix to high level	
TEST1 / TEST2	2	Input / Output	short	
P57 to P50 P67 to P60 P73 toP70 P87 to P80 P97 to P90 PA7 to PA0 VREFH VREFL $\overline{NMI}$ $\overline{WDTOUT}$	48	I/O	open	

3. OPERATION

This section describes the functions and basic operational blocks of the TMP93PS40.

The TMP93PS40 has ROM in place of the mask ROM which isa included in the TMP93CS40. The other configuration and functions are the same as the TMP93CS40. Regarding the function of the TMP93PS40, which is not described herein, see the TMP93CS40.

The TMP93PS40 has two operational modes: MCU mode and PROM mode.

3.1 MCU mode

(1) Mode-setting and function

The MCU mode is set by opening the CLK pin (Output status). In the MCU mode, the operation is same as TMP93CS40.

3.2 Memory Map

Figure 3.1 is a memory map of the TMP93PS40.

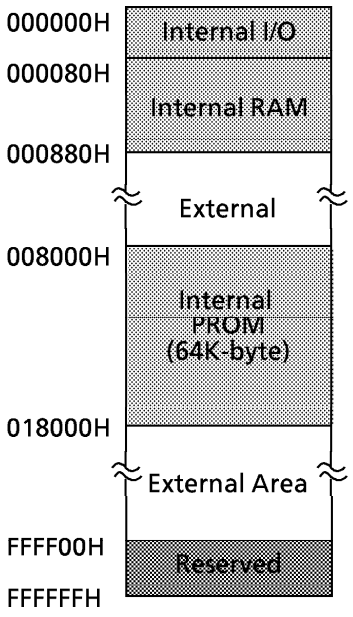


Figure 3.1 (1) Memory map in MCU mode

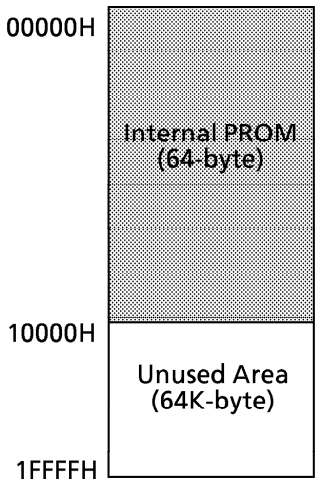


Figure 3.1 (2) Memory map in PROM mode

3.3 PROM Mode

(1) Mode setting and Function

PROM mode is set by setting the $\overline{\text{RESET}}$ and CLK pins to the "L" level. The programming and verification for the internal PROM is achieved by using a general PROM programmer with the adaptor socket.

① OTP adaptor
BM11109 : TMP93PS40F, TMP93PW40F adaptors
BM11129 : TMP93PS40DF, TMP93PW40DF adaptors

② Setting OTP adaptor
Set the switch (SW1) to N side.

③ Setting PROM programmer

i) Set PROM type to TC571000D.
Size : 1 M bit (128K×8 bit)
VPP : 12.75 V
tpw : 100 μs

The electric signature mode (hereinafter referred to as "signature".) is not supported. Therefore if signature is used, the device is damaged because 12.75 V is applied to A9 of address. Do not use signature.

ii) Transferring the data (copy)

In TMP93PS40, PROM is placed on addresses 00000 to 0FFFFH in PROM mode, and addresses 08000H to 17FFFH in MCU mode. Therefore data should be transferred to addresses 00000 to 0FFFFH in PROM mode using the object converter (tuconv) or the block transfer mode (see instruction manual of PROM programmer.) or making the object data.

iii) Setting the programming address

Start address : 00000H
End address : 0FFFFH

Using PROM programmer which can not set the programming address, set FFH at addresses 10000H to 1FFFFH.

④ Programming

Program/verify according to the procedures of PROM programmer.

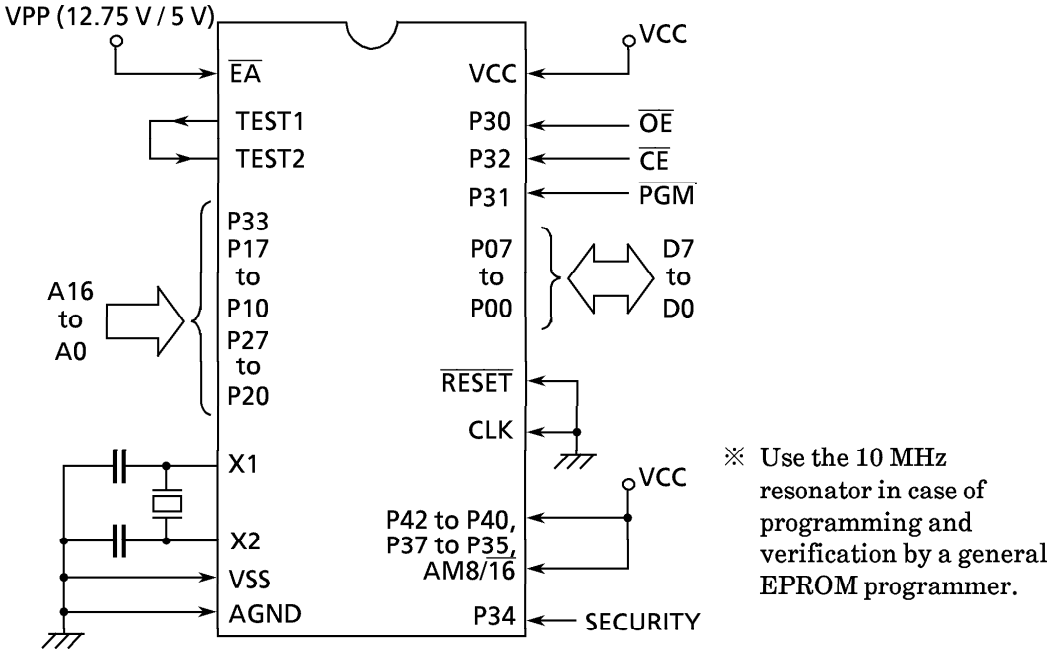


Figure 3.2 PROM Mode Pin Setting

(2) Programming Flow Chart

The programming mode is set by applying 12.75 V (programming voltage) to the VPP pin when the following pins are set as follows,
(VCC : 6.25 V, $\overline{\text{RESET}}$: "L" level, CLK : "L" level).

While address and data are fixed and $\overline{\text{CE}}$ pin is set to "L" level, 0.1 ms of "L" level pulse is applied to $\overline{\text{PGM}}$ pin to program the data.

Then the data in the address is verified.

If the programmed data is incorrect, another 0.1 ms pulse is applied to $\overline{\text{PGM}}$ pin.

This programming procedure is repeated until correct data is read from the address. (25 times maximum)

Subsequently, all data are programmed in all addresses.

The verification for all data is done under the condition of Vpp = Vcc = 5 V after all data were written.

Figure 3.2 (2) shows the programming flow chart.

High Speed Program Writing.

Flow chart

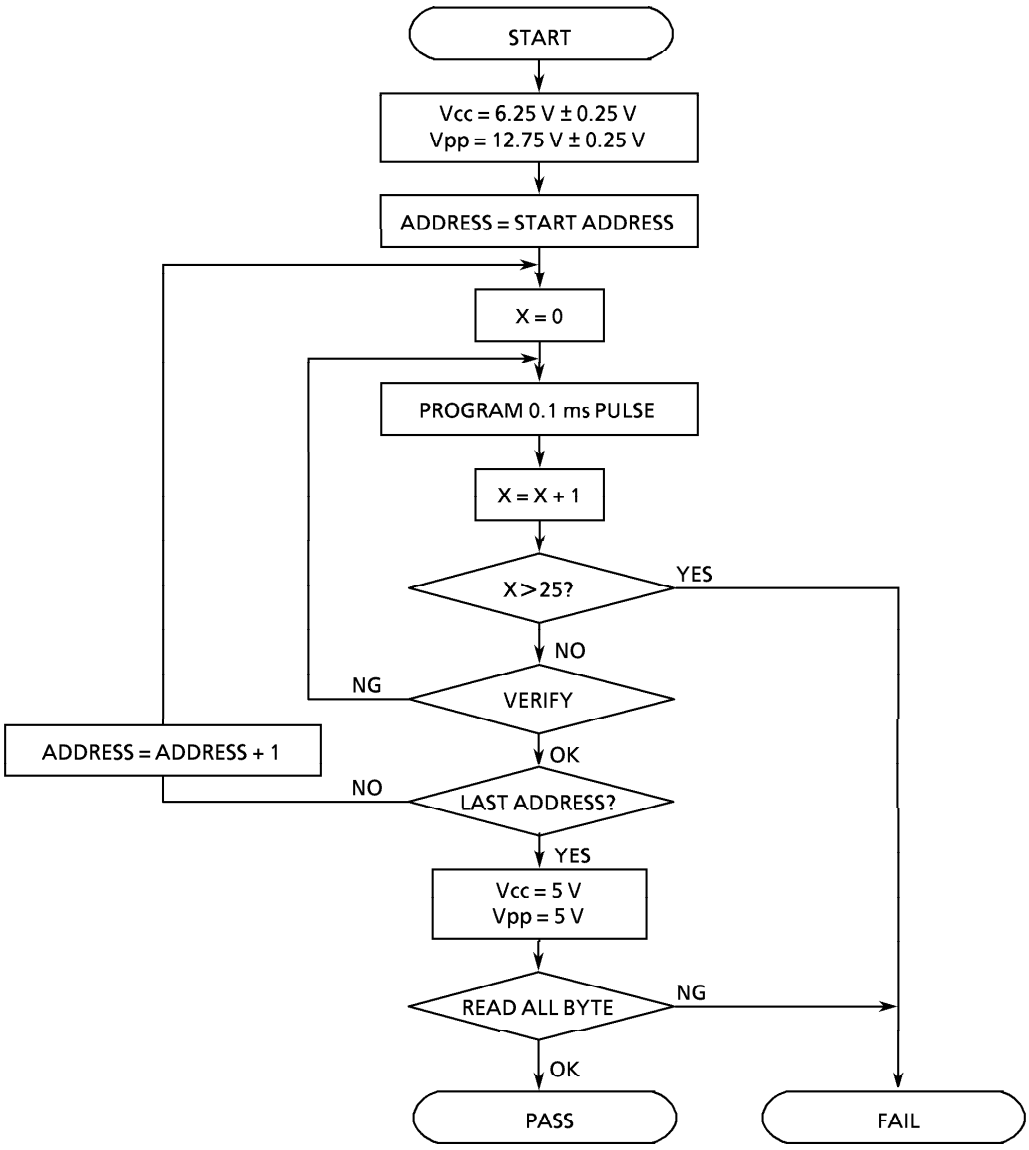


Figure 3.3 Flow chart

(3) Security Bit

The TMP93PS40 has a Security Bit.
If the Security Bit is programmed to "0", the content of the PROM can not be read in PROM mode. (outputs data FFH)

How to program the Security Bit.

The difference from the programming procedures described in section 3.3 (1) are follows.

① Setting OTP adapter
Set the switch (SW1) to S side.

② Setting PROM programmer

ii) Transferring the data

iii) Setting programming address

The security bit is in bit 0 of address 00000H.
Set the start address 00000H and the end address 00000H.
Set the data FEH at the address 00000H.

4. ELECTRICAL CHARACTERISTICS

"X" used in an expression shows a frequency of clock f_{FPH} selected by SYSCR1 < SYSCK >. If a clock gear or a low speed oscillator is selected, a value of "X" is different. The value in an example is calculated at fc, gear = 1/fc (SYSCR1 < SYSCK, GEAR 2 to 0 > = "0000").

4.1 Absolute Maximum Ratings (TMP93PS40F)

Symbol	Parameter	Rating	Unit
V cc	Power Supply Voltage	– 0.5 to 6.5	V
V IN	Input Voltage	– 0.5 to Vcc + 0.5	V
Σ IOL	Output Current (total)	120	mA
Σ IOH	Output Current (total)	– 80	mA
P D	Power Dissipation (Ta = 85 ℃)	600	mW
T SOLDER	Soldering Temperature (10 s)	260	℃
T STG	Storage Temperature	– 65 to 150	℃
T OPR	Operating Temperature	– 40 to 85	℃

4.2 DC Characteristics (1/2)

Ta = – 40 to 85 °C

Symbol	Parameter		Min.	Typ (note 1)	Max.	Unit	Condition
V cc	Power Supply Voltage ($AV_{CC} = V_{CC}$, $AV_{CC} = V_{SS} = 0V$)		4.5		5.5	V	fc = 4 to 20 MHz (fs = 30 to 34 kHz)
			2.7				fc = 4 to 12.5 MHz (fs = 30 to 34 kHz)
V_{IL}	Input Low Voltage	AD0 to 15	– 0.3		0.8	V	$V_{CC} \geqq 4.5$ V
					0.6		$V_{CC} < 4.5$ V
V_{IL1}		Port 2 to A (except P87)			0.3 Vcc		V_{CC} = 2.7 to 5.5 V
V_{IL2}		RESET, NMI, INT0			0.25 Vcc		
V_{IL3}		EA, AM8/16			0.3		
V_{IL4}		X1			0.2 Vcc		
V_{IH}	Input High Voltage	AD0 to 15	2.2		Vcc + 0.3	V	$V_{CC} \geqq 4.5$ V
			2.0				$V_{CC} < 4.5$ V
V_{IH1}		Port 2 to A (except P87)	0.7Vcc				V_{CC} = 2.7 to 5.5 V
V_{IH2}		RESET, NMI, INT0	0.75Vcc				
V_{IH3}		EA, AM8/16	Vcc – 0.3				
V_{IH4}		X1	0.8Vcc				
V_{OL}	Output Low Voltage				0.45	V	I OL = 1.6 mA (V_{CC} = 2.7 to 5.5 V)
V_{OH1}	Output High Voltage		2.4			V	I OH = – 400 μA (V_{CC} = 3 V ± 10 %)
V_{OH2}			4.2				I OH = – 400 μA (V_{CC} = 5 V ± 10 %)

(note1) Typical values are for Ta = 25 °C and V_{CC} = 5 V unless otherwise noted.

4.2 DC Characteristics (2/2)

Symbol	Parameter	Min.	Typ. (Note 1)	Max.	Unit	Condition
I DAR (note 2)	Darlington Drive Current (8 Output Pins Max)	− 1.0		− 3.5	mA	V EXT = 1.5 V R EXT = 1.1 kΩ (when Vcc = 5 V ± 10 %)
I LI	Input Leakage Current		0.02	± 5	μA	0.0 ≦ V_{IN} ≦ V_{CC}
I LO	Output Leakage Current		0.05	± 10		0.2 ≦ V_{IN} ≦ V_{CC} − 0.2
V STOP	Powerdown Voltage (at Stop, RAM Back-up)	2.0		6.0	V	V IL2 = 0.2Vcc, V IH2 = 0.8Vcc
R RST	$\overline{\text{RESET}}$ Pull-up Resistor	50		150	kΩ	Vcc = 5 V ± 10 %
		80		200		Vcc = 3 V ± 10 %
C IO	Pin Capacitance			10	pF	fc = 1 MHz
V TH	Schmitt Width $\overline{\text{RESET}}$, $\overline{\text{NMI}}$, INT0	0.4	1.0		V	
RKL	Programmable Pull-down Resistor	10		80	kΩ	Vcc = 5 V ± 10 %
		30		150		Vcc = 3 V ± 10 %
RKH	Programmable Pull-up Resistor	50		150		Vcc = 5 V ± 10 %
		100		300		Vcc = 3 V ± 10 %
I cc	Normal (note 3)		19	25	mA	Vcc = 5 V ± 10 % fc = 20 MHz
	Normal2 (note 4)		24	30		
	Run		17	25		
	Idle2		10	15		
	Idle1		3.5	5		
	Normal (note 3)		6.5	10	mA	Vcc = 3 V ± 10 % fc = 10 MHz (Typ: Vcc = 3.0 V)
	Normal2 (note 4)		9.5	13		
	Run		5.0	9		
	Idle2		3.0	5		
	Idle1		0.8	1.5		
	Slow (note 3)		20	35	μA	Vcc = 3 V ± 10 % fs = 32.768 kHz (Typ: Vcc = 3.0 V)
	Run		16	30		
	Idle2		10	20		
	Idle1		5	15		
	Stop		0.2	10	μA	Vcc = 2.7 to 5.5 V

(note1) Typical values are for Ta = 25 °C and V_{CC} = 5 V unless otherwise noted.
(note2) I-DAR is guranteed for total of up to 8 ports.
(note3) The condition of measurement of I_{CC} (Normal / Slow).
Only CPU operates. Output ports are open and input ports fixed.
(note4) The condition of measurement of I_{CC} (Normal 2).
CPU and all peripherals operate. Output ports are open and input ports fixed.

4.3 AC Characteristics

(1) Vcc = 5 V ± 10 %

No.	Symbol	Parameter	Variable		16 MHz		20 MHz		Unit
			Min	Max	Min	Max	Min	Max	
1	t_{OSC}	Osc. Period (= x)	50	31250	62.5		50		ns
2	t_{CLK}	CLK Width	2x – 40		85		60		ns
3	t_{AK}	A0 to A23 Valid→ CLK Hold	0.5x – 20		11		5		ns
4	t_{KA}	CLK Valid→ A0 to A23 Hold	1.5x – 70		24		5		ns
5	t_{AL}	A0 to A15 Valid→ ALE Fall	0.5x – 15		16		10		ns
6	t_{LA}	ALE Fall→ A0 to A15 Hold	0.5x – 20		11		5		ns
7	t_{LL}	ALE High Width	x – 40		23		10		ns
8	t_{LC}	ALE Fall→ $\overline{RD}/\overline{WR}$ Fall	0.5x – 25		6		0		ns
9	t_{CL}	$\overline{RD}/\overline{WR}$ Rise→ ALE Rise	0.5x – 20		11		5		ns
10	t_{ACL}	A0 to A15 Valid→ $\overline{RD}/\overline{WR}$ Fall	x – 25		38		25		ns
11	t_{ACH}	A0 to A23 Valid→ $\overline{RD}/\overline{WR}$ Fall	1.5x – 50		44		25		ns
12	t_{CA}	$\overline{RD}/\overline{WR}$ Rise→ A0 to A23 Hold	0.5x – 25		6		0		ns
13	t_{ADL}	A0 to A15 Valid→ D0 to D15 Input		3.0x – 55		133		95	ns
14	t_{ADH}	A0 to A23 Valid→ D0 to D15 Input		3.5x – 65		154		110	ns
15	t_{RD}	$\overline{RD}$Fall →D0 to D15 Input		2.0x – 60		65		40	ns
16	t_{RR}	$\overline{RD}$ Low Pulse Width	2.0x – 40		85		60		ns
17	t_{HR}	$\overline{RD}$Rise→ D0 to D15 Hold	0		0		0		ns
18	t_{RAE}	$\overline{RD}$Rise→ A0 to A15 Output	x – 15		48		35		ns
19	t_{WW}	$\overline{WR}$ Low Pulse Width	2.0x – 40		85		60		ns
20	t_{DW}	D0 to D15 Valid→ $\overline{WR}$ Rise	2.0x – 55		70		45		ns
21	t_{WD}	$\overline{WR}$ Rise →D0 to D15 Hold	0.5x – 15		16		10		ns
22	t_{AWH}	A0 to A23 Valid→ $\overline{WAIT}$ Input (1 WAIT + n mode)		3.5x – 90		129		85	ns
23	t_{AWL}	A0 to A15 Valid→ $\overline{WAIT}$ Input (1 WAIT + n mode)		3.0x – 80		108		70	ns
24	t_{CW}	$\overline{RD}/\overline{WR}$ Fall→$\overline{WAIT}$ Hold (1 WAIT + n mode)	2.0x + 0		125		100		ns
25	t_{APH}	A0 to A23 Valid→ PORT Input		2.5x – 120		36		5	ns
26	t_{APH2}	A0 to A23 Valid→ PORT Hold	2.5x + 50		206		175		ns
27	t_{CP}	$\overline{WR}$ Rise→ PORT Valid		200		200		200	ns
28	t_{ASRH}	A0 to A23 Valid→ $\overline{RAS}$ Fall	1.0x – 40		23		10		ns
29	t_{ASRL}	A0 to A15 Valid→ $\overline{RAS}$ Fall	0.5x – 15		16		10		ns
30	t_{RAC}	$\overline{RAS}$ Fall→ D0 to D15 Input		2.5x – 70		86		55	ns
31	t_{RAH}	$\overline{RAS}$ Fall→ A0 to A15 Hold	0.5x – 15		16		10		ns
32	t_{RAS}	$\overline{RAS}$ Low Pulse Width	2.0x – 40		85		60		ns
33	t_{RP}	$\overline{RAS}$ High Pulse Width	2.0x – 40		85		60		ns
34	t_{RSH}	$\overline{CAS}$ Fall→ $\overline{RAS}$ Rise	1.0x – 40		23		10		ns
35	t_{RSC}	$\overline{RAS}$ Rise→ $\overline{CAS}$ Rise	0.5x – 25		6		0		ns
36	t_{RCD}	$\overline{RAS}$ Fall→ $\overline{CAS}$ Fall	1.0x – 40		23		10		ns
37	t_{CAC}	$\overline{CAS}$ Fall→ D0 to D15 Input		1.5x – 65		29		10	ns
38	t_{CAS}	$\overline{CAS}$ Low Pulse Width	1.5x – 30		64		40		ns

AC Measuring Conditions

- Output Level : High 2.2 V / Low 0.8 V , CL = 50 pF
  (However CL = 100 pF for AD0 to AD15, A0 to A23, ALE, $\overline{RD}$, $\overline{WR}$, $\overline{HWR}$, R/$\overline{W}$, CLK, $\overline{RAS}$, $\overline{CAS0}$ to $\overline{CAS2}$)
- Input Level : High 2.4 V / Low 0.45 V (AD0 to AD15)
  High 0.8 Vcc / Low 0.2 Vcc(Except for AD0 to AD15)

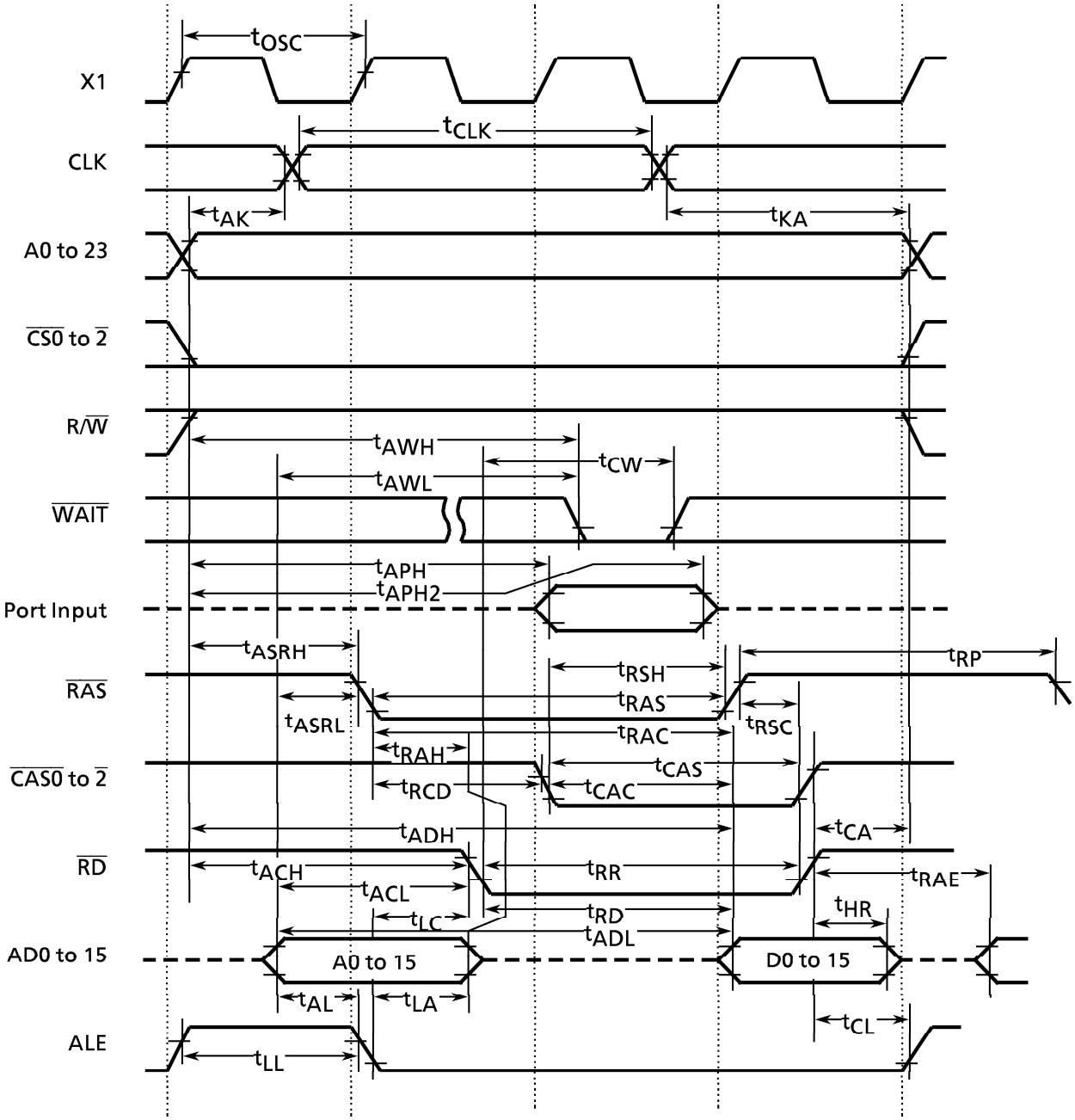
(2) Vcc = 3 V ± 10 %

No.	Symbol	Parameter	Variable		12.5 MHz		Unit
			Min	Max	Min	Max	
1	t_{OSC}	Osc. Period (= x)	80	31250	80		ns
2	t_{CLK}	CLK Width	2x – 40		120		ns
3	t_{AK}	A0 to A23 Valid→ CLK Hold	0.5x – 30		10		ns
4	t_{KA}	CLK Valid→ A0 to A23 Hold	1.5x – 80		40		ns
5	t_{AL}	A0 to A15 Valid→ ALE Fall	0.5x – 35		5		ns
6	t_{LA}	ALE Fall→ A0 to A15 Hold	0.5x – 35		5		ns
7	t_{LL}	ALE High Width	x – 60		20		ns
8	t_{LC}	ALE Fall→ $\overline{RD}/\overline{WR}$ Fall	0.5x – 35		5		ns
9	t_{CL}	$\overline{RD}/\overline{WR}$ Rise→ ALE Rise	0.5x – 40		0		ns
10	t_{ACL}	A0 to A15 Valid→ $\overline{RD}/\overline{WR}$ Fall	x – 50		30		ns
11	t_{ACH}	A0 to A23 Valid→ $\overline{RD}/\overline{WR}$ Fall	1.5x – 50		70		ns
12	t_{CA}	$\overline{RD}/\overline{WR}$ Rise→ A0 to A23 Hold	0.5x – 40		0		ns
13	t_{ADL}	A0 to A15 Valid→ D0 to D15 Input		3.0x – 110		130	ns
14	t_{ADH}	A0 to A23 Valid→ D0 to D15 Input		3.5x – 125		155	ns
15	t_{RD}	$\overline{RD}$Fall →D0 to D15 Input		2.0x – 115		45	ns
16	t_{RR}	$\overline{RD}$ Low Pulse Width	2.0x – 40		120		ns
17	t_{HR}	$\overline{RD}$Rise→ D0 to D15 Hold	0		0		ns
18	t_{RAE}	$\overline{RD}$Rise→ A0 to A15 Output	x – 25		55		ns
19	t_{WW}	$\overline{WR}$ Low Pulse Width	2.0x – 40		120		ns
20	t_{DW}	D0 to D15 Valid→ $\overline{WR}$ Rise	2.0x – 120		40		ns
21	t_{WD}	$\overline{WR}$ Rise →D0 to D15 Hold	0.5x – 40		0		ns
22	t_{AWH}	A0 to A23 Valid→ $\overline{WAIT}$ Input (1 WAIT + n mode)		3.5x – 130		150	ns
23	t_{AWL}	A0 to A15 Valid→ $\overline{WAIT}$ Input (1 WAIT + n mode)		3.0x – 100		140	ns
24	t_{CW}	$\overline{RD}/\overline{WR}$ Fall→ $\overline{WAIT}$ Hold (1 WAIT + n mode)	2.0x + 0		160		ns
25	t_{APH}	A0 to A23 Valid→ PORT Input		2.5x – 120		80	ns
26	t_{APH2}	A0 to A23 Valid→ PORT Hold	2.5x + 50		250		ns
27	t_{CP}	$\overline{WR}$ Rise→ PORT Valid		200		200	ns
28	t_{ASRH}	A0 to A23 Valid→ $\overline{RAS}$ Fall	1.0x – 60		20		ns
29	t_{ASRL}	A0 to A15 Valid→ $\overline{RAS}$ Fall	0.5x – 40		0		ns
30	t_{RAC}	$\overline{RAS}$ Fall→ D0 to D15 Input		2.5x – 90		110	ns
31	t_{RAH}	$\overline{RAS}$ Fall→ A0 to A15 Hold	0.5x – 25		15		ns
32	t_{RAS}	$\overline{RAS}$ Low Pulse Width	2.0x – 40		120		ns
33	t_{RP}	$\overline{RAS}$ High Pulse Width	2.0x – 40		120		ns
34	t_{RSH}	$\overline{CAS}$ Fall→ $\overline{RAS}$ Rise	1.0x – 55		25		ns
35	t_{RSC}	$\overline{RAS}$ Rise→ $\overline{CAS}$ Rise	0.5x – 25		15		ns
36	t_{RCD}	$\overline{RAS}$ Fall→ $\overline{CAS}$ Fall	1.0x – 40		40		ns
37	t_{CAC}	$\overline{CAS}$ Fall→ D0 to D15 Input		1.5x – 120		0	ns
38	t_{CAS}	$\overline{CAS}$ Low Pulse Width	1.5x – 40		80		ns

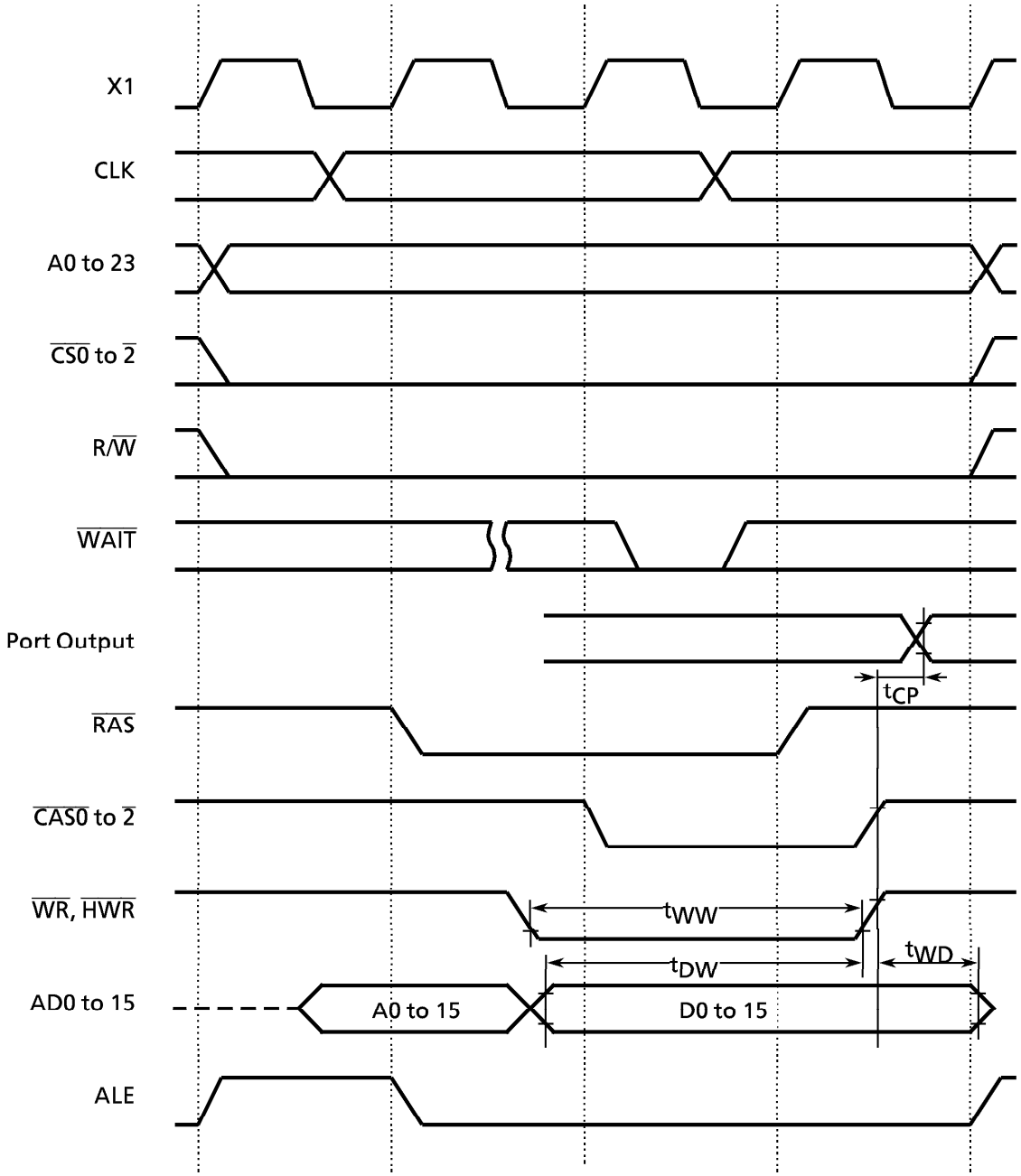
AC Measuring Conditions

- Output Level : High 0.7 × V_{CC} / Low 0.3 × V_{CC} , CL = 50 pF
- Input Level : High 0.9 × V_{CC} / Low 0.1 × V_{CC}

(1) Read Cycle


tOSC
X1
tCLK
CLK
tAK
tKA
A0 to 23
CS0 to 2
R/W
tAWH
tCW
tAWL
WAIT
tAPH
tAPH2
Port Input
tASRH
tRSH
tRP
RAS
tRAS
tASRL
tRSC
tRAC
tRAH
tCAS
CAS0 to 2
tRCD
tCAC
tADH
tCA
RD
tACH
tRR
tRAE
tACL
tRD
tHR
tLC
tADL
AD0 to 15
A0 to 15
D0 to 15
tAL
tLA
tCL
ALE
tLL

(2) Write Cycle



4.4 A/D Conversion Characteristics

AVCC = VCC, AVSS = VSS

Symbol	Parameter	Power Supply	Min	Typ	Max	Unit
V_{REFH}	Analog reference voltage (+)	V_{CC} = 5V ± 10 %	V_{CC} – 1.5V	V_{CC}	V_{CC}	V
		V_{CC} = 3V ± 10 %	V_{CC} – 0.2V	V_{CC}	V_{CC}	
V_{REFL}	Analog reference voltage (–)	V_{CC} = 5V ± 10 %	V_{SS}	V_{SS}	V_{SS} + 0.2V	
		V_{CC} = 3V ± 10 %	V_{SS}	V_{SS}	V_{SS} + 0.2V	
V_{AIN}	Analog input voltage range		VREFL		VREFH	
I_{REF} (V_{REFL} = 0 V)	Analog current for analog reference voltage <VREFON> = 1	V_{CC} = 5V ± 10 %		0.5	1.5	mA
		V_{CC} = 3V ± 10 %		0.3	0.9	
	<VREFON> = 0	V_{CC} = 2.7 to 5.5V		0.02	5.0	μA
–	Error (excluding quantizing error)	V_{CC} = 5V ± 10 %		± 1.0	± 3.0	LSB
		V_{CC} = 3V ± 10 %		± 1.0	± 3.0	

Note 1 : 1LSB = (VREFH – VREFL) / 2^{10} [V]

Note 2 : Minimum operation frequency
The operation of the A/D converter is guaranteed only when fc (high-frequency oscillator) is used. (It is not guaranteed when fs is used.) Additionally, it is guaranteed with $f_{FPH} \geqq 4$ MHz.

Note 3 : The value I_{CC} includes the current which flows through the AV_{CC} pin.

4.5 Serial Channel Timing

(1) I/O Interface Mode

① SCLK Input Mode

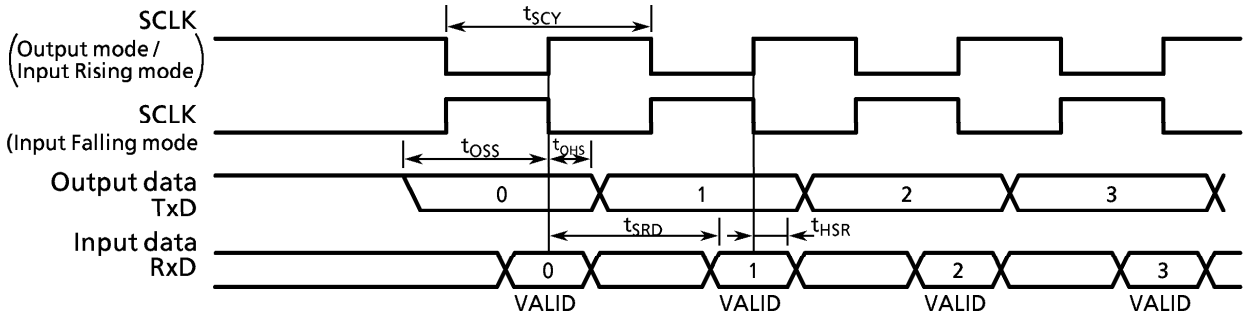
Symbol	Parameter	Variable		32.768 MHz (Note)		12.5 MHz		20 MHz		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{SCY}	SCLK cycle	16X		488 μs		1.28		0.8		μs
t_{OSS}	Output Data → Rising edge or SCLK	t_{SCY}/2 – 5X – 50		91.5 μs		190		100		ns
t_{OHS}	SCLK rising edge → Output Data hold	5X – 100		152 μs		300		150		ns
t_{HSR}	SCLK rising edge → Input Data hold	0		0		0		0		ns
t_{SRD}	SCLK rising edge → effective data input		t_{SCY} – 5X – 100		336 μs		780		450	ns

Note : When fs is used as system clock (f_{SYS}) or fs is used as input clock to prescaler.
*) SCLK rising / falling timing ··· SCLK rising in the rising mode of SCLK, SCLK falling in the falling mode of SCLK.

② SCLK Output Mode

Symbol	Parameter	Variable		32.768 MHz (Note)		12.5 MHz		20 MHz		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{SCY}	SCLK cycle (programmable)	16X	8192X	488 μs	250 ms	1.28	655.36	0.8	409.6	μs
t_{OSS}	Output Data → SCLK rising edge	t_{SCY} – 2X – 150		427 μs		970		550		ns
t_{OHS}	SCLK rising edge→ Output Data hold	2X – 80		60 μs		80		20		ns
t_{HSR}	SCLK rising edge→ Input Data hold	0		0		0		0		ns
t_{SRD}	SCLK rising edge→ effective data input		t_{SCY} – 2X – 150		428 μs		970		550	ns

Note : When fs is used as system clock (f_{SYS}) or fs is used as input clock to prescaler.



4.6 Timer/Counter Input Clock (TI0, TI4, TI5, TI6, TI7)

Symbol	Parameter	Variable		12.5 MHz		20 MHz		Unit
		Min	Max	Min	Max	Min	Max	
t_{VCK}	Clock Cycle	8X + 100		740		500		ns
t_{VCKL}	Low level clock Pulse width	4X + 40		360		240		ns
t_{VCKH}	High level clock Pulse width	4X + 40		360		240		ns

4.7 Interrupt and Capture

(1) $\overline{NMI}$, INT0 interrupts

Symbol	Parameter	Variable		12.5 MHz		20 MHz		Unit
		Min	Max	Min	Max	Min	Max	
t_{INTAL}	$\overline{NMI}$, INT0 Low Level Pulse Width	4X		320		200		ns
t_{INTAH}	$\overline{NMI}$, INT0 High Level Pulse Width	4X		320		200		ns

(2) INT4 to 7 interrupts, capture

Input pulse width of INT4 to 7 depends on the operation clock of CPU and Timer (9 bit prescaler). The following shows the pulse width in each clock.

System clock selected <SYSCK>	Prescaler clock selected <PRCK1 to 0>	t_{INTBL} (INT4 to 7 low level pulse width)		t_{INTBH} (INT4 to 7 high level pulse width)		Unit
		Variable	20 MHz	Variable	20 MHz	
		Min	Min	Min	Min	
0 (fc)	00 (f_{FPH})	8X + 100	500	8X + 100	500	ns
	01 (fs)	8XT + 0.1	244.3	8XT + 0.1	244.3	μs
	10 (fc/16)	128X + 0.1	6.5	128X + 0.1	6.5	
1 (fs) (Note 2)	00 (f_{FPH})	8XT + 0.1	244.3	8XT + 0.1	244.3	
	01 (fs)					

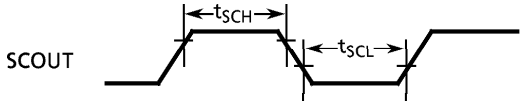
Note 1: XT represents the cycle of the low frequency clock fs. Calculated at fs = 32.768 kHz.
Note 2: When fs is used as the system clock, fc/16 can not be selected for the prescaler clock.

4.8 SCOUT pin AC characteristics

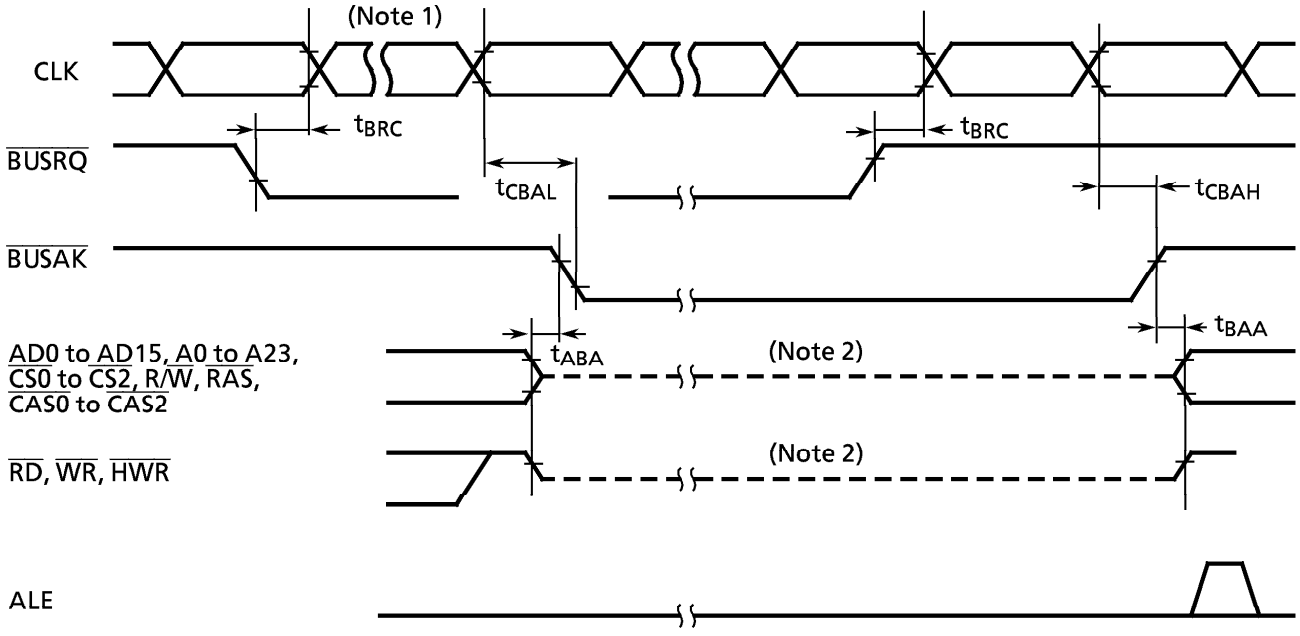
Symbol	Parameter		Variable		10 MHz		20 MHz		Unit
			Min	Max	Min	Max	Min	Max	
t_{SCH}	High-Level Pulse Width	V_{CC} = 5 V ± 10 %	0.5X – 10		40		15		ns
		V_{CC} = 3 V ± 10 %	0.5X – 20		30		–	–	
t_{SCL}	Low-Level Pulse Width	V_{CC} = 5 V ± 10 %	0.5X – 10		40		15		ns
		V_{CC} = 3 V ± 10 %	0.5X – 20		30		–	–	

Measurement condition

- Output level: High 2.2 V / Low 0.8 V, CL = 10 pF



4.9 Timing Chart for Bus Request ($\overline{BUSRQ}$) / Bus Acknowledge ($\overline{BUSAK}$)



Symbol	Parameter	Variable		12.5 MHz		20 MHz		Unit
		Min	Max	Min	Max	Min	Max	
t_{BRC}	$\overline{BUSRQ}$ Set-up Time to CLK	120		120		120		ns
t_{CBAL}	CLK→ $\overline{BUSAK}$ Falling Edge		1.5X + 120		270		195	ns
t_{CBAH}	CLK→ $\overline{BUSAK}$ Rising Edge		0.5X + 40		80		65	ns
t_{ABA}	Output Buffer off to $\overline{BUSAK}$ ↓	0	80	0	80	0	80	ns
t_{BAA}	$\overline{BUSAK}$ ↑ to Output Buffer on	0	80	0	80	0	80	ns

Note 1 : The Bus will be released after the $\overline{WAIT}$ request is inactive, when the $\overline{BUSRQ}$ is set to "0" during "Wait" cycle.

Note 2 : This line only shows the output buffer is off-state.
It doesn't indicate the signal level is fixed.
Just after the bus is released, the signal level which is set before the bus is released is kept dynamically by the external capacitance. Therefore, to fix the signal level by an external resistor during bus releasing, designing is executed carefully because the level-fix will be delayed.
The internal programmable pull-up/pull-down resistor is switched active/non-active by an internal signal.

4.10 Read operation in PROM mode

DC / AC characteristics

Ta = 25 ± 5 °C Vcc = 5 V ± 10 %

Symbol	Parameter	Condition	Min	Max	Unit
V_{PP}	V_{PP} Read Voltage	–	4.5	5.5	V
V_{IH1}	Input High Voltage (A0 to A16, $\overline{CE}$, $\overline{OE}$, $\overline{PGM}$)	–	2.2	V_{CC} + 0.3	V
V_{IL1}	Input Low Voltage (A0 to A16, $\overline{CE}$, $\overline{OE}$, $\overline{PGM}$)	–	– 0.3	0.8	V
t_{ACC}	Address to Output Delay	C_L = 50 pF	–	2.25TCYC + α	ns

TCYC = 400 ns (10 MHz Clock)
α = 200 ns

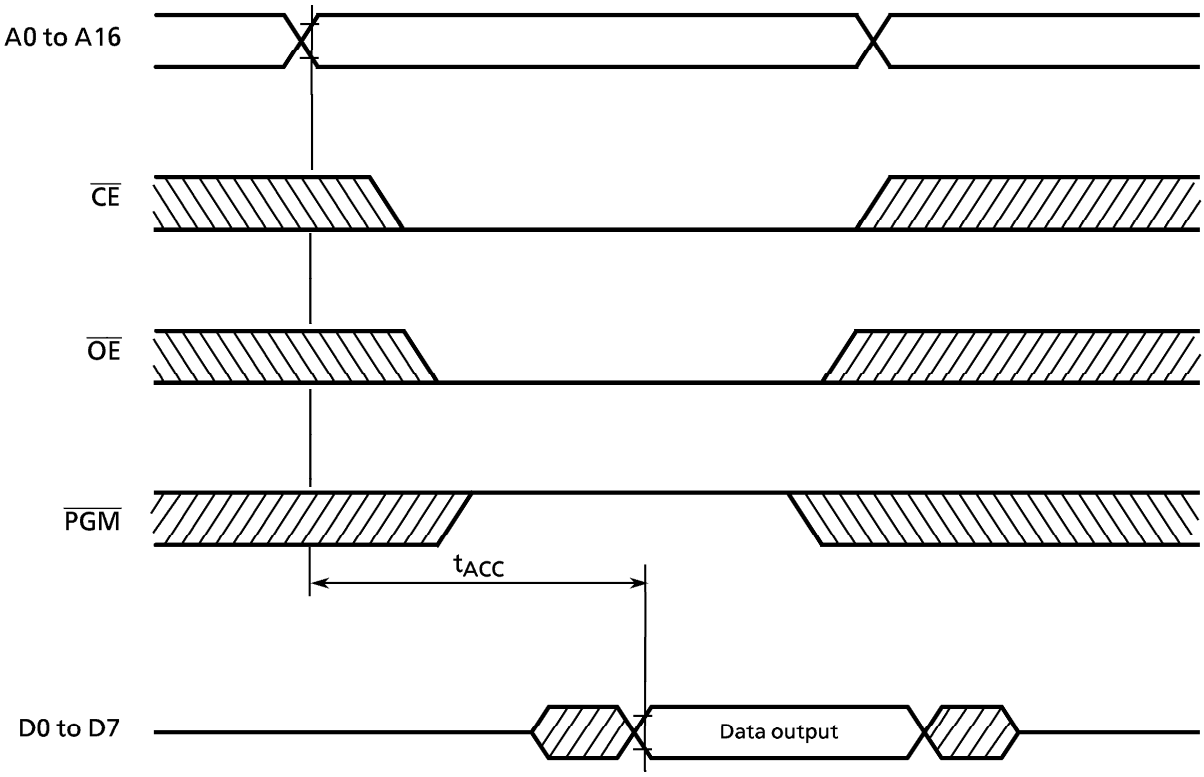
4.11 Program operation in PROM mode

DC / AC characteristics

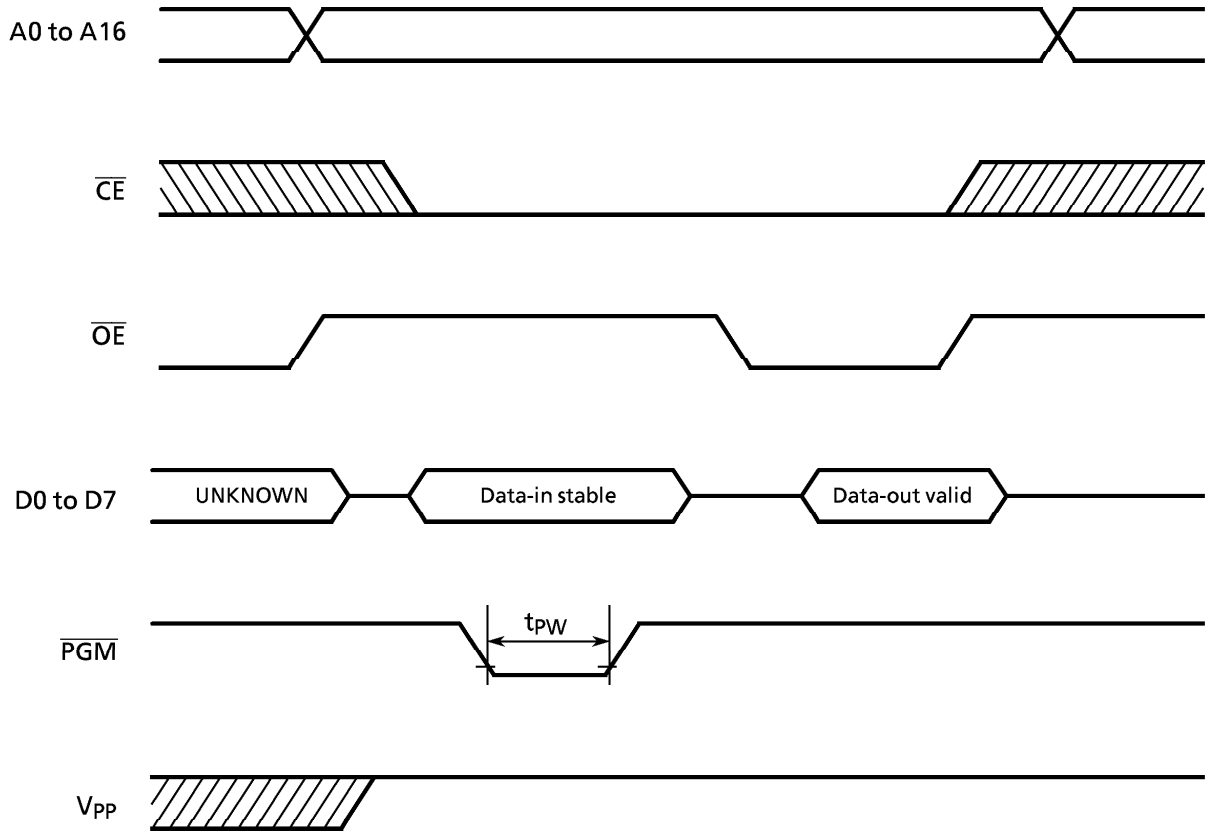
Ta = 25 ± 5 °C Vcc = 6.25 V ± 0.25 V

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{PP}	Programming Supply Voltage	–	12.50	12.75	13.00	V
V_{IH}	Input High Voltage (D0 to D7, A0 to A16, $\overline{CE}$, $\overline{OE}$, $\overline{PGM}$)	–	2.6		V_{CC} + 0.3	V
V_{IL}	Input Low Voltage (D0 to D7, A0 to A16, $\overline{CE}$, $\overline{OE}$, $\overline{PGM}$)	–	– 0.3		0.8	V
I_{CC}	V_{CC} Supply Current	fc = 10 MHz	–		50	mA
I_{PP}	V_{PP} Supply Current	V_{PP} = 13.00 V	–		50	mA
t_{PW}	$\overline{PGM}$ Program Pulse Width	C_L = 50 pF	0.095	0.1	0.105	ms

4.12 Timing chart of read operation in PROM mode



4.13 Timing chart of read operation in PROM mode



NOTE

1. The power supply of V_{PP} (12.75 V) must be turned on at the same time or the later time for a power supply of V_{CC} and must be turned off at the same time or early time for a power supply of V_{CC}.
2. The device suffers a damage taking out and putting in on the condition of $V_{PP} = 12.75$ V.
3. The maximum spec of V_{PP} pin is 14.0 V. Be carefull a overshoot at the programming.

4.14 Recommended Oscillator

The TMP93PS40 is evaluated with the resonators. The evaluation results are referred to your usable application.

Note: The load capacitance of the resonator consists of the load capacitance C1, C2 to be connected and the floating capacitance on the target board.
Even if the specified values of C1 and C2 are used, there is a possibility that the oscillator malfunctions due to different load capacitance of the target boards. Therefore the peripheral patterns of the oscillator should be designed to take the shortest course on the board.
It is recommended that the evaluation of the resonators is executed on the target board.

(1) Recommended oscillator circuit

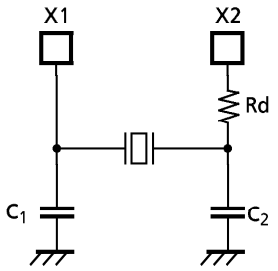


Figure 1 : Example of High Frequency Resonator Connection

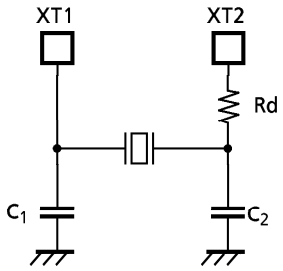


Figure 2 : Example of Low Frequency Resonator Connection

(2) Ceramic resonator: TOYAMA MURATA MFG. CO., LTD

Ta = – 20 to 80 °C

Parameter	Frequency (MHz)	Recommended resonator	Recommended value			Vcc [V]
			C_1 [pF]	C_2 [pF]	Rd [kΩ]	
High frequency oscillation	4.00	CSA4.00MGU	30	30	0	2.7 to 5.5
		CST4.00MGWU	*(30)	*(30)		
	10.00	CSA10.0MTZ093	30	30		
		CST4.00MGWU	*(30)	*(30)		
	12.50	CSA12.5MTZ093	30	30		
		CST12.5MTW093	*(30)	(30)		
	16.00	CSA16.00MXZ040	5	5		4.5 to 5.5
	20.00	CSA20.00MXZ040	3	3		

* : In case of built-in condenser type.
Reference : TOYAMA MURATA MFG. CO., LTD
PRODUCT ENGINEERING SERVICE SECTION
PHONE : 0764-29-1221
FAX : 0764-29-9971