ZILOG

ADVANCE INFORMATION SPECIFICATION

Z86B07

CMOS Z8® 8-BIT MICROCONTROLLER FOR INTELLIGENT BATTERY CHARGING AND MONITORING

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FEATURES

- Low-Cost, 8-Bit CMOS MCU
- 2 Kbytes of ROM, 124 Bytes of RAM
- 18-Pin Package Styles (DIP, SOIC)
- Clock Speeds: 8 and 12 MHz
- 3.0 to 5.5 Volt Operation Range
- Extended Operating Temperature Range: –40°C to +105°C
- Low Power Consumption: 50 mW (typical)
- Low Voltage Protection
- Fast Instruction Pointer: 1 µs at 12 MHz
- Two Standby Modes: STOP and HALT
- 14 Input/Output Lines
- Three Digital Inputs at CMOS Levels
- Eleven Schmitt-Triggered Digital Inputs at CMOS Levels
- Two Programmable 8-Bit Counter/Timers Each with a 6-Bit Programmable Prescaler
- Six Vectored, Priority Interrupts from Six Different Sources
- On-Board Power-On Reset Circuit
- Permanently Enabled Watch-Dog Timer
- Two Enhanced Comparators with Programmable Interrupt Polarity.
- On-Chip Oscillator that Accepts a Crystal, Ceramic Resonator, LC, or External Clock Drive.
- Incorporates patented Black and Decker Intelligent Battery Charging and Logarithmic A/D Functions.

GENERAL DESCRIPTION

The Z86B07 Microcontroller Unit (MCU) is a member of Zilog's Z8® single-chip microcontroller family with 2 Kbytes of ROM and 124 bytes of general-purpose RAM. The device is housed in 18-pin DIP and SOIC style packages and manufactured in CMOS technology.

As a modified version of Zilog's Z86C07, the Z86B07 offers all the outstanding features of the Z8 family architecture, plus hardware/software enhancements for intelligent battery charging and system power control functions. Furthermore, by means of a special licensing agreement, the designer can have the added advantage of patented Black and Decker software code that ensures accurate sensing and control of the charging function to eliminate battery overcharging and reduce charge time to as little as 15 minutes.

For applications demanding powerful I/O capabilities, the Z86B07 features 14 pins dedicated to input and output. These lines are grouped into three ports and are configurable under software control to provide I/O, timing and status signals. There are two basic address spaces available to support this design configuration: Program Memory and 124 bytes of general-purpose registers (Figure 1).

GENERAL DESCRIPTION (Continued)

To unburden the system from coping with real-time tasks, such as counting/timing and I/O data communications, the Z86B07 offers two on-chip counter/timers with a large number of user-selectable modes. In addition, the device features two on-board comparators for processing analog signals with a common reference voltage.

Characterized by a flexible I/O scheme, efficient register and address space structure and a number of ancillary features, the Z86B07 is well-suited for a variety of consumer and industrial applications.

Notes:
All Signals with a preceding front slash, "/", are active Low, e.g.: B/W (WORD is active Low); /B/W (BYTE is active Low, only).

Power connections follow conventional descriptions below:

Connection	Circuit	Device
Power	V_{CC}	V_{DD}
Ground	GND	V_{SS}

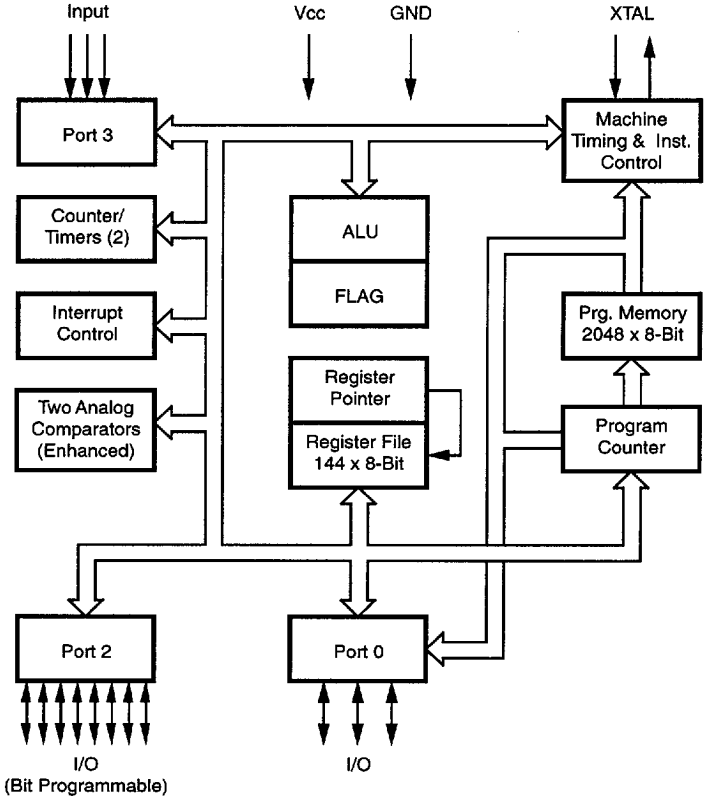


Figure 1. Z86B07 Functional Block Diagram

PIN DESCRIPTION

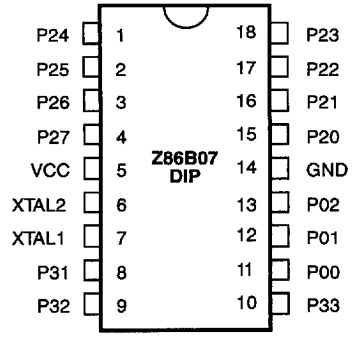


Figure 2. 18-Pin DIP Pin Configuration

Table 1. 18-Pin DIP Pin Identification

Pin #	Symbol	Function	Direction
1-4	P24-P27	Port 2, Pins 4, 5, 6, 7	In/Output
5	V_{cc}	Power Supply	
6	XTAL2	Crystal Oscillator Clock	Input
7	XTAL1	Crystal Oscillator Clock	Output
8	P31	Port 3, Pin 1, AN1	Input
9	P32	Port 3, Pin 2, AN2	Input
10	P33	Port 3, Pin 3, REF	Input
11-13	P00-P02	Port 0, Pins 0, 1, 2	In/Output
14	GND	Ground	
15-18	P20-P23	Port 2, Pins 0, 1 ,2, 3	In/Output

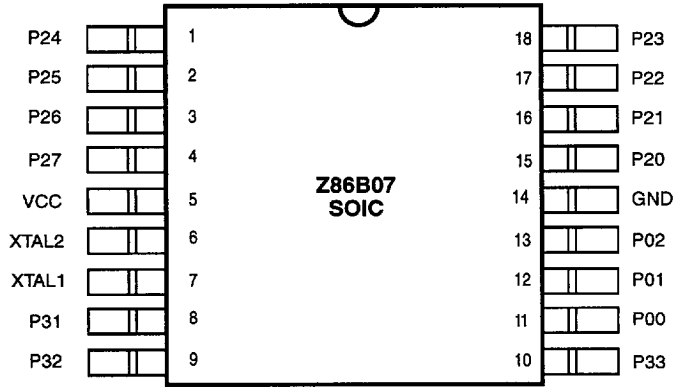


Figure 3. 18-Pin SOIC Pin Configuration

Table 2. 18-Pin SOIC Pin Identification

Pin #	Symbol	Function	Direction
1-4	P24-P27	Port 2, Pins 4, 5, 6, 7	In/Output
5	V_{cc}	Power Supply	
6	XTAL2	Crystal Oscillator Clock	Input
7	XTAL1	Crystal Oscillator Clock	Output
8	P31	Port 3, Pin 1, AN1	Input
9	P32	Port 3, Pin 2, AN2	Input
10	P33	Port 3, Pin 3, REF	Input
11-13	P00-P02	Port 0, Pins 0,1, 2	In/Output
14	GND	Ground	
15-18	P20-P23	Port 2, Pin 0, 1, 2, 3	In/Output

PIN DESCRIPTION (Continued)

XTAL1, XTAL2 *Crystal In, Crystal Out* (time-based input and output, respectively). These pins connect a parallel-resonant crystal, LC, or an external single-phase clock (12 MHz max) to the on-chip clock oscillator and buffer.

Port 0 (P02-P00). Port 0 is a 3-bit I/O, nibble programmable, bidirectional, CMOS compatible I/O port. These three I/O lines can be configured under software control to be input or output (Figure 4). Inputs are Schmitt-triggered.

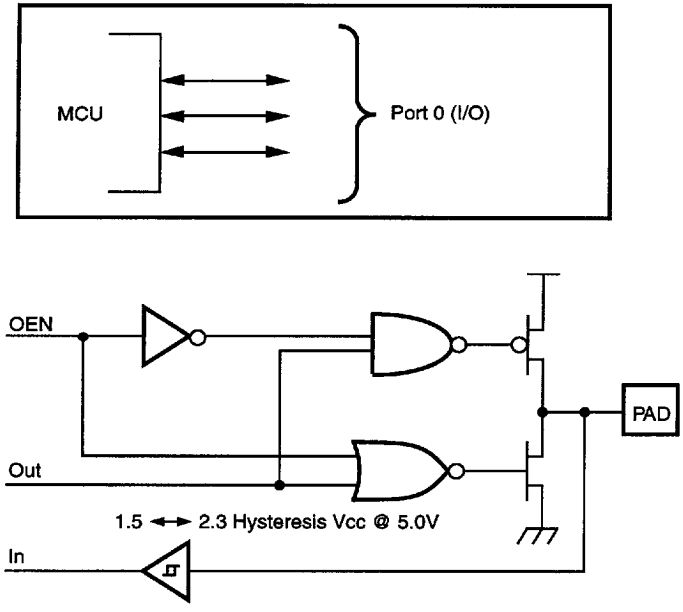


Figure 4. Port 0 Configuration

Port 2 (P27-P20). Port 2 is an 8-bit I/O, bit programmable, bidirectional, CMOS compatible I/O port. These eight I/O lines can be configured under software control to be input or output, independently. Bits programmed as outputs may be globally programmed as either push-pull or open-drain (Figure 5). Inputs are Schmitt-triggered.

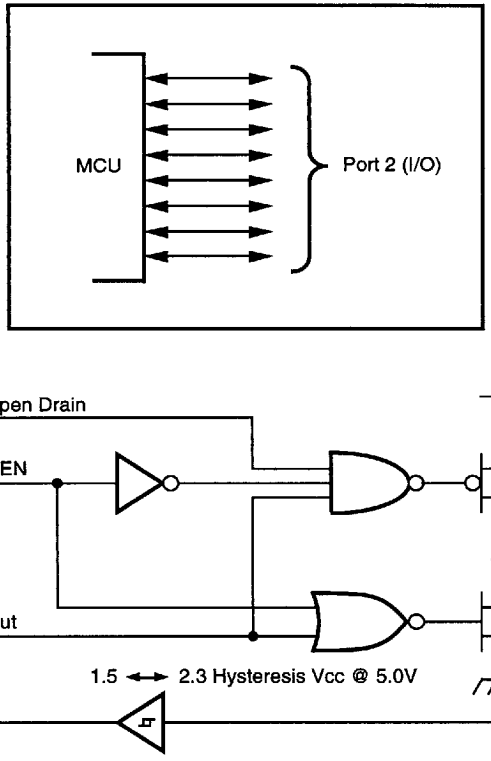


Figure 5. Port 2 Configuration

PIN DESCRIPTION (Continued)

Port 3 (P33-P31). Port 3 is a 3-bit, CMOS compatible port with three fixed input (P33-P31) lines. These three input lines can be configured under software control as digital or analog inputs. These three input lines can also be used as the interrupt sources IRQ0-IRQ3 and as the timer input signal (T_{IN}) (Figure 6).

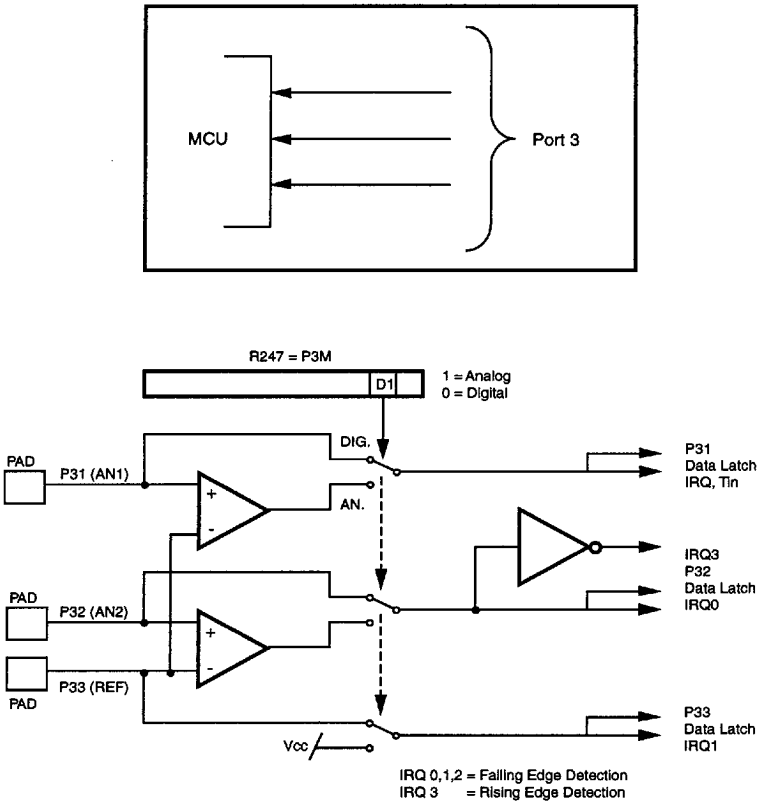


Figure 6. Port 3 Configuration

Comparator Inputs. Two analog comparators are added to Port 3 inputs for interface flexibility.

Typical applications for the on-board comparators are: Zero crossing detection, A/D conversion, voltage scaling, and threshold detection.

The dual comparator (common inverting terminal) features a single power supply which discontinues power in STOP Mode. The common voltage range is 0-4V; the power supply and common mode rejection ratios are 90 dB and 60 dB, respectively.

Interrupts are generated on either edge of Comparator 2's output, or on the falling edge of Comparator 1's output. The comparator output may be used for interrupt generation, Port 3 data inputs, or T_{IN} through P31. Alternatively, the comparators may be disabled, freeing the reference input (P33) for use as IRQ1 and/or P33 input.

FUNCTIONAL DESCRIPTION

The Z86B07 MCU incorporates the following special functions to enhance the standard Z8® architecture to provide the user with increased design flexibility.

Reset. Upon power-up the Power-On Reset circuit waits for T_{POR}, plus 18 crystal clocks, then starts program execution at address %000C (HEX) (Figure 7). The Z86B07 control registers' Reset value is stated in Table 3.

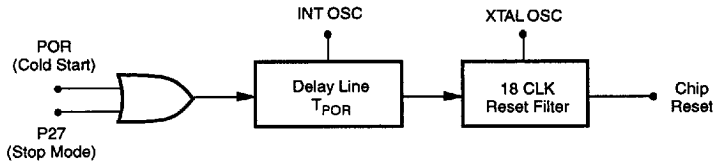


Figure 7. Internal Reset Configuration

Table 3. Z86B07 Control Registers

Addr.	Reg.	Reset Condition D7	D6	D5	D4	D3	D2	D1	D0	Comments
F1	TMR	0	0	0	0	0	0	0	0	
F2	T1	U	U	U	U	U	U	U	U	
F3	PRE1	U	U	U	U	U	U	0	0	
F4	T0	U	U	U	U	U	U	U	U	
F5	PRE0	U	U	U	U	U	U	U	0	
F6*	P2M	1	1	1	1	1	1	1	1	Inputs after reset
F7*	P3M	U	U	U	U	U	U	0	0	
F8*	P01M	U	U	U	0	U	U	0	1	
F9	IPR	U	U	U	U	U	U	U	U	
FA	IRQ	U	U	0	0	0	0	0	0	IRQ3 is used for positive edge detection
PB	IMR	0	U	U	U	U	U	U	U	
PC	FLAGS	U	U	U	U	U	U	U	U	
FD	RP	0	0	0	0	0	0	0	0	
FE	SPH	U	U	U	U	U	U	U	U	Not used, stack always internal
FF	SPL	U	U	U	U	U	U	U	U	

Note:
* Registers are not reset after a Stop-Mode Recovery using P27 pin. A subsequent reset will cause these control registers to be reconfigured as shown in Table 3 and the user must avoid bus contention on the port pins or it may affect device reliability.

Program Memory. The Z86B07 can address up to 2 Kbytes of internal program memory (Figure 8). The first 12 bytes of program memory are reserved for the interrupt vectors. These locations contain six 16-bit vectors that correspond to the six available interrupts. Bytes 0-2048 are on-chip mask-programmed ROM.

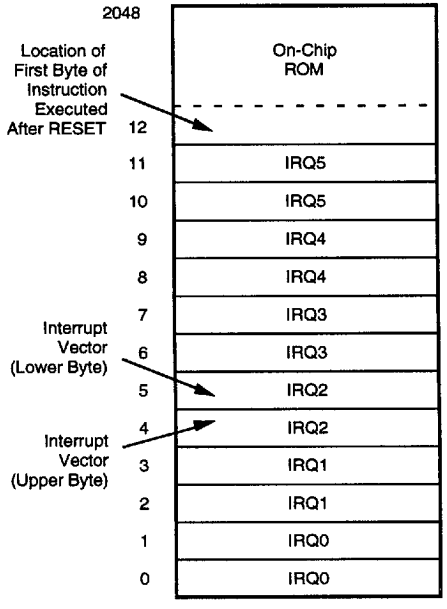


Figure 8. Program Memory Map

FUNCTIONAL DESCRIPTION (Continued)

Register File. The Register File consists of three I/O port registers, 124 general-purpose registers, and 15 control and status registers (R3-R0, R127-R4 and R255-R241, respectively - Figure 9). The Z86B07 instructions can access registers directly or indirectly through an 8-bit address field. This allows short, 4-bit register addressing using the Register Pointer. In the 4-bit mode, the register file is divided into eight working register groups, each occupying 16 continuous locations. The Register Pointer (Figure 10) addresses the starting location of the active working-register group.

General-Purpose Registers (GPR). These registers are undefined after the device is powered up. The registers keep their last value after any reset, as long as the reset occurs in the V_{CC} voltage-specified operating range. **Note:** Register R254 has been designated as a general-purpose register.

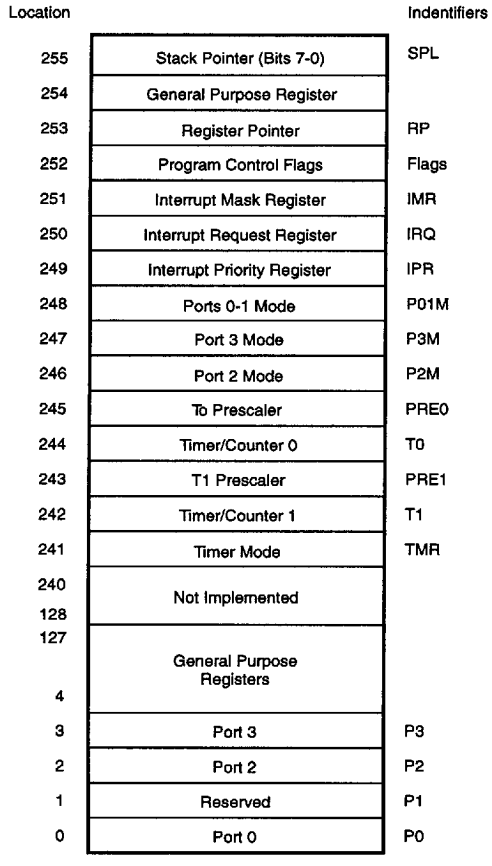


Figure 9. Register File

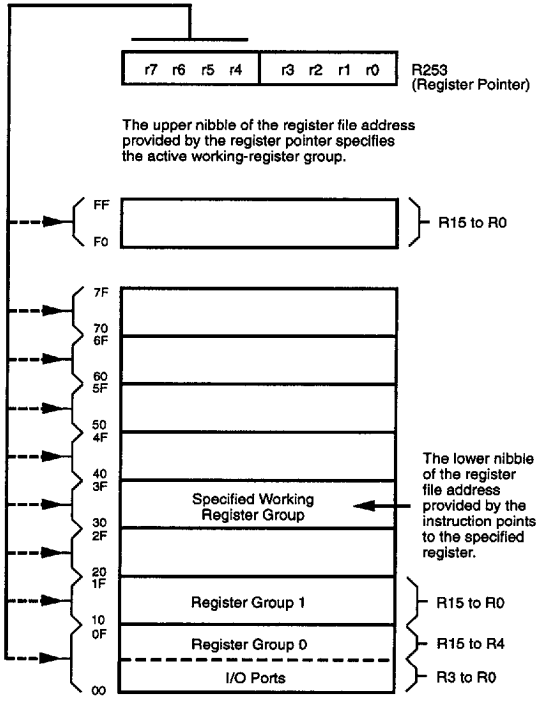


Figure 10. Register Pointer

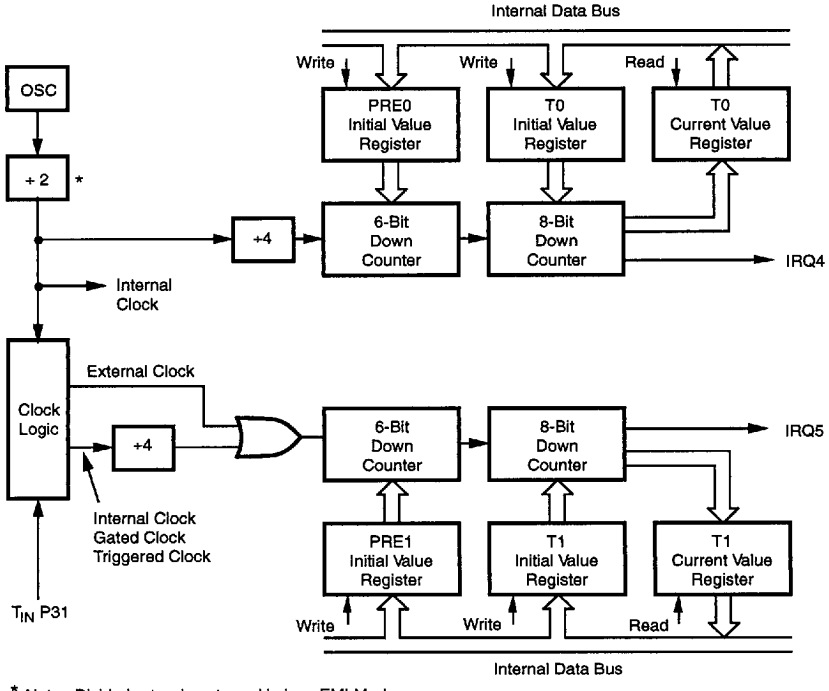
Stack Pointer. The Z86B07 has an 8-bit Stack Pointer (R255) used for the internal stack that resides within the 124 general-purpose registers.

Counter/Timer. There are two 8-bit programmable counter/timers (T0 and T1), each driven by its own 6-bit programmable prescaler. The T1 prescaler can be driven by internal or external clock sources, however the T0 can be driven by the internal clock source only (Figure 11).

The 6-bit prescalers can divide the input frequency of the clock source by any integer number from 1 to 64. Each prescaler drives its counter, which decrements the value (1 to 256) that has been loaded into the counter. When both counter and prescaler reach the end of count, a timer interrupt request IRQ4 (T0) or IRQ5 (T1) is generated.

The counter can be programmed to start, stop, restart to continue, or restart from the initial value. The counters can also be programmed to stop upon reaching zero (single pass mode) or to automatically reload the initial value and continue counting (modulo-n continuous mode).

The counters, but not the prescalers are read at any time without disturbing their value or count mode. The clock source for T1 is user-definable and can be either the internal microprocessor clock divided-by-four, or an external signal input through Port 3. The Timer Mode register configures the external timer input (P30) as an external clock, a trigger input that is retriggerable or not retriggerable, or as a gate input for the internal clock.



* Note: Divide-by-two is not used in Low EMI Mode.

Figure 11. Counter/Timers Block Diagram

FUNCTIONAL DESCRIPTION (Continued)

Interrupts. The Z86B07 has six interrupts from six different sources. These interrupts are maskable and prioritized (Figure 12). The six sources are divided as follows: the falling edge of P31 (AN1), P32 (AN2), P33 (REF), the rising edge of P32 (AN2), and the two counter/timers. The Interrupt Mask Register globally or individually enables or disables the six interrupt requests (Table 4).

When more than one interrupt is pending, priorities are resolved by a programmable priority encoder that is controlled by the Interrupt Priority register. All Z86B07 interrupts are vectored through locations in program memory. When an interrupt machine cycle is activated, an interrupt request is granted. This disables all subsequent interrupts, saves the Program Counter and Status Flags, and then branches to the program memory vector location reserved for that interrupt. This memory location and the next byte contain the 16-bit starting address of the interrupt service routine for that particular interrupt request.

To accommodate polled interrupt systems, interrupt inputs are masked and the interrupt request register is polled to determine which of the interrupt requests needs service.

Note: User must select any Z86C08 mode in Zilog's C12 ICEBOX™ emulator. The rising edge interrupt is not supported on the Z86CCP00ZEM emulator.

Table 4. Interrupt Types, Sources, and Vectors

Source	Name	Vector Location	Comments
AN2(P32)	IRQ0	0,1	External (F)Edge
REF(P33)	IRQ1	2,3	External (F)Edge
AN1(P31)	IRQ2	4,5	External (F)Edge
AN2(P32)	IRQ3	6,7	External (R)Edge
T0	IRQ4	8,9	Internal
T1	IRQ5	10,11	Internal

Notes:
F = Falling edge triggered
R = Rising edge triggered

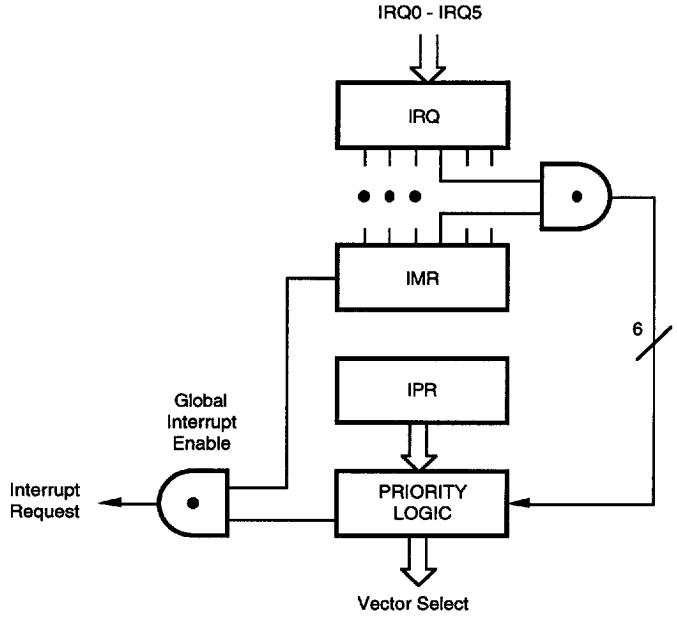


Figure 12. Interrupt Block Diagram

Clock. The Z86B07 on-chip oscillator has a high-gain, parallel-resonant amplifier for connection to a crystal, ceramic resonator, or any suitable external clock source (XTAL1 = Input, XTAL2 = Output). The crystal should be AT cut, 12 MHz max, with a series resistance (RS) less than or equal to 100 Ohms.

The crystal should be connected across XTAL1 and XTAL2 using the vendor's recommended crystal capacitors from each pin directly to device Ground, V_{SS} pin 14, to reduce Ground noise injection.

HALT Mode. Turns off the internal CPU clock but not the crystal oscillation. The counter/timers and external interrupts IRQ0, IRQ1, IRQ2, and IRQ3 remain active. The device can be recovered by interrupts, either externally or internally generated. The program execution begins at location 000C (HEX). An interrupt request must be executed (enabled) to exit HALT mode. After the interrupt service routine, the program continues from the instruction after the HALT.

STOP Mode. This instruction turns off the internal clock and external crystal oscillation and reduces the standby current to less than 10 µA. The STOP Mode can be released by two methods. The first method is a RESET of the device by removing V_{CC}. The second method is to configure P27 as an input line. When the device executes the STOP instruction, a low input level on P27 releases the STOP Mode.

Program execution under both conditions begins at location 000C (HEX). However, when P27 is used to release the STOP Mode, the I/O port mode registers are not reconfigured to their default power-on conditions. This prevents any I/O, configured as output when the STOP instruction was executed, from glitching to an unknown state.

To use the P27 release approach with STOP Mode, use the following instruction:

```
LD      P2M, #1XXXXXXXB
NOP
STOP
X = depends on user's application
```

In order to enter STOP (or HALT) mode, it is necessary to first flush the instruction pipeline to avoid suspending execution in mid-instruction. To do this, the user must execute a NOP (opcode = FFH) immediately before the appropriate SLEEP instruction. i.e.:

```
FF   NOP    ; clear the pipeline
6F   STOP   ; enter STOP mode
            or
FF   NOP    ; clear the pipeline
7F   HALT   ; enter HALT mode
```

Watch-Dog Timer (WDT). The Watch-Dog Timer is permanently enabled and should be refreshed at least every Twdt; otherwise, a Reset will occur.

WDT = 5F (HEX).

Opcode WDT (5FH). Execution of the command clears the WDT counter. This must be done at least every 15 µsec, otherwise, the WDT times out and generates a Reset. The generated Reset is the same as a Power-On Reset of T_{POR} plus 18 XTAL clock cycles. The WDT instruction affects the Flags accordingly: Z = 1, S = 0, V = 0.

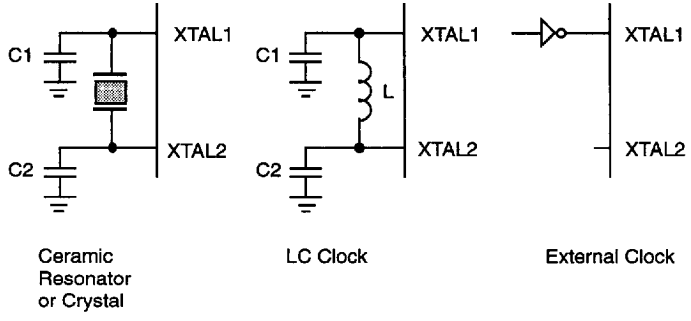


Figure 13. Oscillator Configuration

FUNCTIONAL DESCRIPTION (Continued)

Low Voltage Protection (V_{LV}). The Low Voltage trip voltage (V_{LV}) is less than 3 volts and above 1.4 volts under the following conditions:

Maximum (V_{LV}) Conditions:

Case 1 T_A = –40°C, +105°C, Internal Clock Frequency equal or less than 1 MHz

Case 2 T_A = –40°C, +85°C, Internal Clock Frequency equal or less than 2 MHz

Note: The internal clock frequency is one-half the external clock frequency.

The device will function normally at or above 3.0V under all conditions. Below 3.0V, the device functions normally until the Low Voltage Protection trip point (V_{LV}) is reached. The device is guaranteed to function normally at supply voltages above the low voltage trip point for the temperatures and operating frequencies in Case 1 and Case 2 above. The actual low voltage trip point is a function of temperature and process parameters (Figure 14).

2 MHz (Typical)

Temp	–40°C	0°C	+25°C	+70°C	+105°C
V_{LV}	2.55	2.4	2.1	1.7	1.6

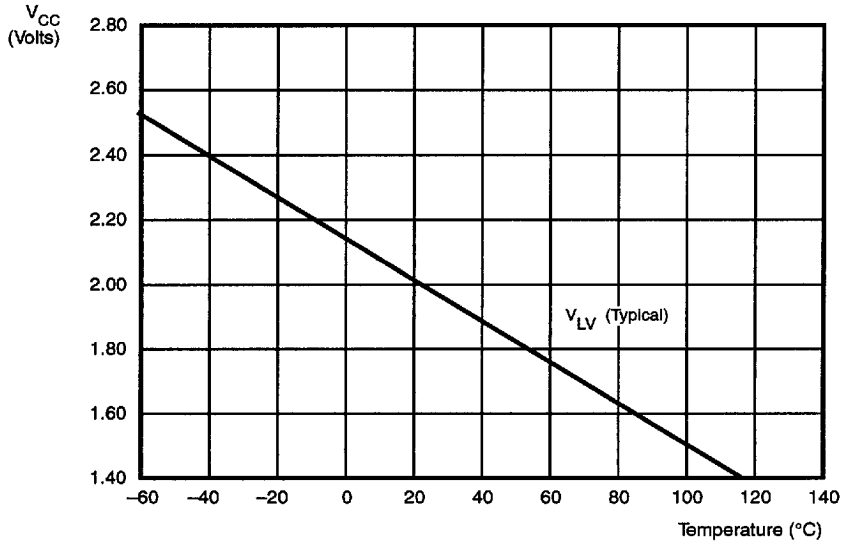


Figure 14. Typical Z86B07 V_{LV} vs Temperature

ABSOLUTE MAXIMUM RATINGS

Parameter	Min	Max	Units
Ambient Temperature under Bias	–40	+105	°C
Storage Temperature	–65	+150	°C
Voltage on any Pin with Respect to V_{SS} (Note 1)	–0.6	+12	V
Voltage on V_{DD} Pin with Respect to V_{SS}	–0.3	+7	V
Voltage on Pin 7 with Respect to V_{SS} (Note 2)	–0.6	V_{DD}+1	V
Total Power Dissipation		462	mW
Maximum Current out of V_{SS}		85	mA
Maximum Current into V_{DD}		85	mA
Maximum Current into an Input Pin (Note 3)		±600	µA
Maximum Current into an Open-Drain Pin (Note 4)		±600	µA
Maximum Output Current Sinked by any I/O Pin		12	mA
Maximum Output Current Sourced by any I/O Pin		12	mA
Total Maximum Output Current Sinked by Port 2		70	mA
Total Maximum Output Current Sourced by Port 2		70	mA

Notice:
Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability. Total power dissipation should not exceed 616 mW for the package. Power dissipation is calculated as follows:

Notes:
[1] This applies to all pins except where noted. Maximum current into pin must be ±600 µA.
[2] There is no input protection diode from pin to V_{DD}.
[3] This excludes Pin 7 and Pin 8.
[4] Device pin is not at an output Low state.

Total Power Dissipation = V_{DD} x [I_{DD} – (sum of I_{OH})] + sum of [(V_{DD}–V_{OH}) x I_{OH}] + sum of (V_{OL} x I_{OL})

STANDARD TEST CONDITIONS

The characteristics listed below apply for standard test conditions as noted. All voltages are referenced to GND. Positive current flows into the referenced pin (Figure 15).

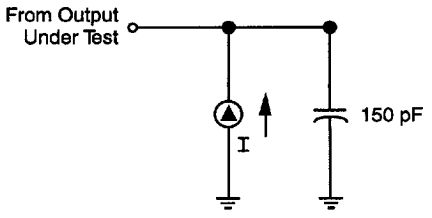


Figure 15. Test Load Diagram

CAPACITANCE

T_A = GND = 0V, f = 1.0 MHz, unmeasured pins returned to GND.

Parameter	Max
Input capacitance	10 pF
Output capacitance	20 pF
I/O capacitance	25 pF

V_{CC} SPECIFICATION

V_{CC} = 3.0V to 5.0V
Typicals are at 3.3V and 5.0V.

DC ELECTRICAL CHARACTERISTICS

Sym	Parameter	V_{CC}[4]	T_A = 0°C to +70°C Min	Max	T_A = −40°C to +105°C Min	Max	Typical @ 25°C	Units	Conditions
	Max Input Voltage	3.0V		12		12		V	I_{IN} < 250 µA [6]
		5.5V		12		12		V	I_{IN} < 250 µA [6]
V_{CH}	Clock Input High Voltage	3.0V	0.8 V_{CC}	V_{CC}+0.3	0.8 V_{CC}	V_{CC}+0.3	1.7	V	Driven by External Clock Generator
		5.5V	0.8 V_{CC}	V_{CC}+0.3	0.8 V_{CC}	V_{CC}+0.3	2.75	V	Driven by External Clock Generator
V_{CL}	Clock Input Low Voltage	3.0V	V_{SS}–0.3	0.2 V_{CC}	V_{SS}–0.3	0.2 V_{CC}	0.8	V	Driven by External Clock Generator
		5.5V	V_{SS}–0.3	0.2 V_{CC}	V_{SS}–0.3	0.2 V_{CC}	1.5	V	Driven by External Clock Generator
V_{IH}	Input High Voltage	3.0V	0.7 V_{CC}	V_{CC}+0.3	0.7 V_{CC}	V_{CC}+0.3	1.8	V	
		5.5V	0.7 V_{CC}	V_{CC}+0.3	0.7 V_{CC}	V_{CC}+0.3	2.8	V	
V_{IL}	Input Low Voltage	3.0V	V_{SS}–0.3	0.2 V_{CC}	V_{SS}–0.3	0.2 V_{CC}	0.8	V	
		5.5V	V_{SS}–0.3	0.2 V_{CC}	V_{SS}–0.3	0.2 V_{CC}	1.5	V	
V_{OH}	Output High Voltage	3.0V	V_{CC}–0.4		V_{CC}–0.4		2.7	V	I_{OH} = −2.0 mA [5]
		5.5V	V_{CC}–0.4		V_{CC}–0.4		5.5	V	I_{OH} = −2.0 mA [5]
		3.0V	V_{CC}–0.4		V_{CC}–0.4			V	Low Noise @ 0.5 mA
		5.5V	V_{CC}–0.4		V_{CC}–0.4			V	Low Noise @ 0.5 mA
V_{OL1}	Output Low Voltage	3.0V		0.8		0.8	0.3	V	I_{OL} = +4.0 mA [5]
		5.5V		0.4		0.4	0.2	V	I_{OL} = +4.0 mA [5]
		3.0V		0.4		0.4		V	Low Noise @ 0.5 mA
		5.5V		0.4		0.4		V	Low Noise @ 0.5 mA
V_{OL2}	Output Low Voltage	3.0V		1.0		1.0	0.8	V	I_{OL} = +12 mA, 3 Pin Max [5]
		5.5V		0.8		0.8	0.3	V	I_{OL} = +12 mA, 3 Pin Max [5]
V_{OFFSET}	Comparator Input Offset Voltage	3.0V		25		25	10	mV	
		5.5V		25		25	10	mV	
V_{LV}	V_{CC} Low Voltage			2.7		2.95	2.1	V	@ 1 MHz Max, Int. CLK Freq
I_{IL}	Input Leakage	3.0V	−1.0	1.0	−1.0	1.0		µA	V_{IN} = 0V, V_{CC}
		5.5V	−1.0	1.0	−1.0	1.0		µA	V_{IN} = 0V, V_{CC}
$_{OL}$	Output Leakage	3.0V	−1.0	1.0	−1.0	1.0		µA	V_{IN} = 0V, V_{CC}
		5.5V	−1.0	1.0	−1.0	1.0		µA	V_{IN} = 0V, V_{CC}
V_{ICMR}	Input Common Mode Range		0	V_{CC} −1.0	0	V_{CC} −1.5		V	

DC ELECTRICAL CHARACTERISTICS (Continued)

Sym	Parameter	V_{CC}[4]	T_A = 0°C to +70°C Min	Max	T_A = −40°C to +105°C Min	Max	Typical @ 25°C	Units	Conditions
I_{CC}	Supply Current	3.0V		3.5		3.5	1.0	mA	All Output and I/O Pins Floating @ 2 MHz
		5.5V		7.0		7.0	3.5	mA	All Output and I/O Pins Floating @ 2 MHz
		3.0V		5.0		8.0	2.5	mA	All Output and I/O Pins Floating @ 8 MHz
		5.5V		11.0		11.0	5.3	mA	All Output and I/O Pins Floating @ 8 MHz
		3.0V		7.5		10	3.0	mA	All Output and I/O Pins Floating @ 12 MHz
		5.5V		15		15	7.5	mA	All Output and I/O Pins Floating @ 12 MHz
I_{CC1}	Standby Current	3.0V		2.5		2.5	0.7	mA	HALT Mode V_{IN} = 0V, V_{CC} @ 2 MHz
		5.5V		4.0		5.0	2.0	mA	HALT Mode V_{IN} = 0V, V_{CC} @ 2 MHz
		3.0V		3.0		4.0	1.0	mA	HALT Mode V_{IN} = 0V, V_{CC} @ 8 MHz
		5.5V		5.0		5.0	2.8	mA	HALT Mode V_{IN} = 0V, V_{CC} @ 8 MHz
		3.0V		4.5		4.5	1.5	mA	HALT Mode V_{IN} = 0V, V_{CC} @ 12 MHz
		5.5V		7.0		7.0	4.0	mA	HALT Mode V_{IN} = 0V, V_{CC} @ 12 MHz
I_{CC}	Supply Current (Low Noise Mode)	3.0V		3.5		3.5	1.0	mA	All Output and I/O Pins Floating @ 1 MHz
		5.5V		7.0		7.0	2.8	mA	All Output and I/O Pins Floating @ 1 MHz
		3.0V		5.8		5.8	1.5	mA	All Output and I/O Pins Floating @ 2 MHz
		5.5V		9.0		9.0	3.5	mA	All Output and I/O Pins Floating @ 2 MHz
		3.0V		8.0		8.0	2.0	mA	All Output and I/O Pins Floating @ 4 MHz
		5.5V		11.0		11.0	5.4	mA	All Output and I/O Pins Floating @ 4 MHz

Sym	Parameter	V_{CC}[4]	T_A = 0°C to +70°C Min	Max	T_A = −40°C to +105°C Min	Max	Typical @ 25°C	Units	Conditions
I_{CC1}	Standby Current (Low Noise Mode)	3.0V		1.2		1.2	0.3	mA	HALT Mode V_{IN} = 0V, V_{CC} @ 1 MHz
		5.5V		1.6		1.6	0.5	mA	HALT Mode V_{IN} = 0V, V_{CC} @ 1 MHz
		3.0V		1.5		1.5	0.5	mA	HALT Mode V_{IN} = 0V, V_{CC} @ 2 MHz
		5.5V		1.9		1.9	1	mA	HALT Mode V_{IN} = 0V, V_{CC} @ 2 MHz
		3.0V		2.0		2.0	0.9	mA	HALT Mode V_{IN} = 0V, V_{CC} @ 4 MHz
		5.5V		2.4		2.4	1.6	mA	HALT Mode V_{IN} = 0V, V_{CC} @ 4 MHz
I_{CC2}	Standby Current	3.0V		10		20	1.2	µA	STOP Mode V_{IN} = 0V, V_{CC} WDT is not Running
		5.5V		10		20	2.0	µA	STOP Mode V_{IN} = 0V, V_{CC} WDT is not Running

Notes:

[1] I_{CC1}

	Typ	Max	Unit	Freq
Clock Driven	0.3	5.0	mA	8 MHz
Crystal/Resonator	3.5	5.0	mA	8 MHz

[2] V_{SS} = 0V = GND

[3] The device is operational until the Low Voltage Protection Trip Point (V_{LV}) is reached. The minimum operational V_{CC} depends on the value of the voltage V_{LV} at the ambient temperature. The V_{LV} increases as the temperature decreases.

[4] The V_{CC} Voltage specification of 3.0V guarantees 3.3V ±0.3V and V_{CC} voltage specification of 5.5V guarantees 5.0V ±0.5V.

[5] Standard Mode (not Low EMI Mode)

[6] Excludes clock pins.

DC ELECTRICAL CHARACTERISTICS

Timing Diagrams

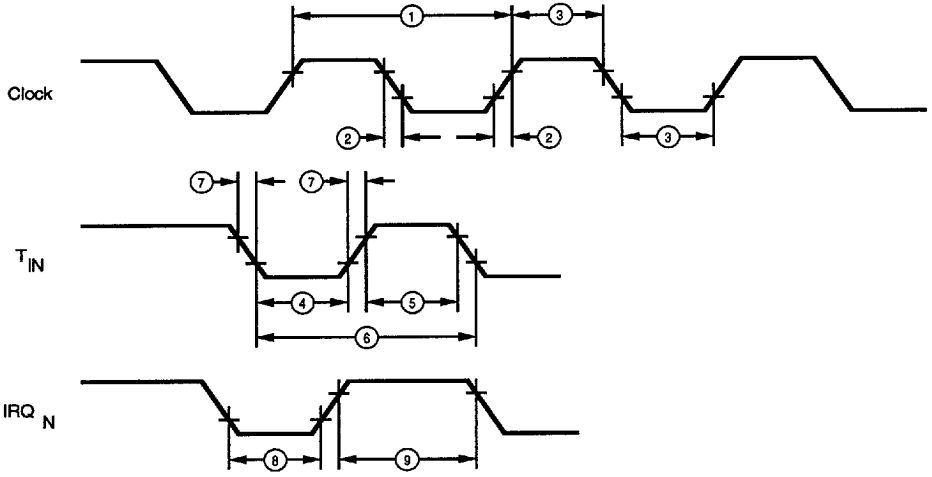


Figure 16. Electrical Timing Diagram

AC ELECTRICAL CHARACTERISTICS

Timing Table (Standard Mode)

				T_A = −40°C to +105°C					
				8 MHz		12 MHz			
No	Symbol	Parameter	V_{cc}[3]	Min	Max	Min	Max	Units	Notes
1	TpC	Input Clock Period	3.0V	125	DC	83	DC	ns	[1]
			5.5V	125	DC	83	DC	ns	[1]
2	TrC,TfC	Clock Input Rise and Fall Times	3.0V		25		15	ns	[1]
			5.5V		25		15	ns	
3	TwC	Input Clock Width	3.0V	62		41			[1]
			5.5V	62		41		ns	[1]
4	TwTinL	Timer Input Low Width	3.0V	100		100		ns	[1]
			5.5V	70		70		ns	[1]
5	TwTinH	Timer Input High Width	3.0V	5TpC		5TpC			[1]
			5.5V	5TpC		5TpC			[1]
6	TpTin	Timer Input Period	3.0V	8TpC		8TpC			[1]
			5.5V	8TpC		8TpC			[1]
7	TrTin, TtTin	Timer Input Rise and Fall Timer	3.0V		100		100	ns	[1]
			5.5V		100		100	ns	[1]
8	TwiL	Int. Request Input Low Time	3.0V	100		100		ns	[1,2]
			5.5V	70		70		ns	[1,2]
9	TwIH	Int. Request Input High Time	3.0V	5TpC		5TpC			[1]
			5.5V	5TpC		5TpC			[1,2]
10	Twdt	Watch-Dog Timer Delay Time	3.0V	25		25		ms	[1,4]
			5.5V	5		5		ms	[1,4]
11	Tpor		3.0V		24		24	ms	[1]
			5.5V		12		12	ms	[1]

Notes:

[1] Timing Reference uses 0.7 V_{cc} for a logic 1 and 0.2 V_{cc} for a logic 0.

[2] Interrupt request through Port 3 (P33-P31).

[3] The V_{cc} Voltage specification of 3.0V guarantees 3.3V ±0.3V and V_{cc} voltage specification of 5.5V guarantees 5.0V ±0.5V.

[4] Length of time before WDT times out.

Low Noise Version

Low EMI Emission

The Z86B07 can be programmed to operate in a Low EMI emission mode by means of a mask ROM bit option. Use of this feature results in:

- Less than 1 mA consumed during HALT mode, –0°C to +70°C.
- All pre-driver slew rates reduced to 10 ns (typical).
- Internal SCLK/TCLK = XTAL operation limited to a maximum of 4 MHz - 250 ns cycle time.
- Output drivers have resistances of 200 ohms (typical).
- Oscillator divide-by-two circuitry eliminated.

The Low EMI mode is mask-programmable to be selected by the customer at the time the ROM code is submitted.

EMI Characteristics

The Z86B07 operating in the Low EMI mode generates EMI as measured in the following chart:

The measurements were made while operating the Z86B07 in three states: (1) Idle condition; (2) static output; (3) switched output.

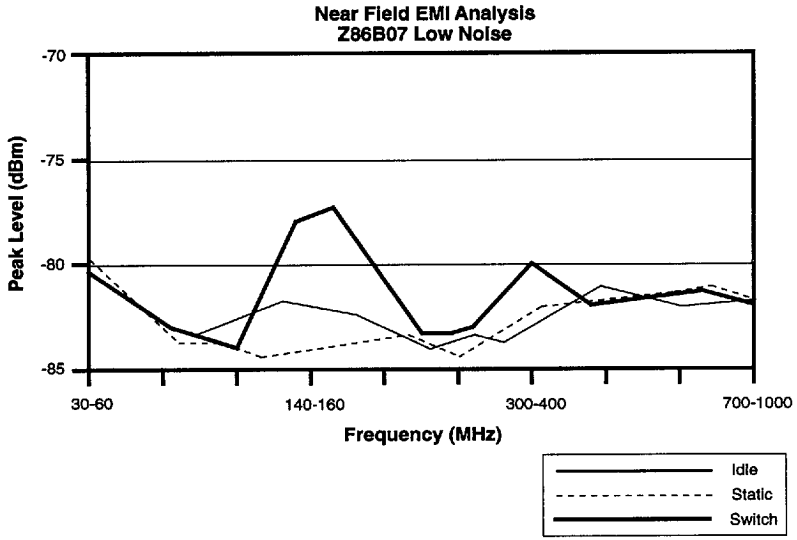


Figure 17. Low Noise Analysis

Z86B07 Comparator Data

Parameter	Symbol	T_A= 0°C to +70°C Min	Max	V_{CC}= 5 V ±10% (Typical)	Notes and Conditions
Input Offset Voltage	V_{OFFSET}		±15 mV	5 mV	Output switch point VO = 1.4 VDC with V_{IN} (V+) over the specified V_{ICR}
Average Temperature Co-efficient of V_{OFFSET}	TCVIO			15 µV/C	
Input Bias Current	I_{IB}		±150 na	2 na	[1]
Input Offset Current	I_{IO}		400 na	2 na	[1]
Input Common Mode Voltage Range	V_{ICR}	0	V_{CC} –1.0V		[5]
Slew Rate	SR	60V		70V	Per 1 µs (output) [6]
Response Time (Low to High)	TPLH		5 µs	1 µs	[2]
Response Time (High to Low)	TPHL		330 ns	110 ns	[2]
Response Time1 (Low to High)	TPLH1		180 ns	60 ns	[3]
Response Time1 (High to Low)	TPHL1		330 ns	110 ns	[3]
Large Signal Response Time2 (Low to High)	TPLH2		180 ns	60 ns	[4]
Large Signal Response Time2 (High to Low)	TPHL2		330 ns	110 ns	[4]
Common mode Rejection Ratio	CMRR	40 dB		44 dB	[7,8] Freq = 4 MHz T_A = 25°C
				54 dB	[7,8] Freq = 0.5 MHz T_A = 25°C

Notes:

[1] Due to the nature of CMOS transistor, input current is a measure of input leakage with voltage applied over the specified input common mode range.

[2] Over the input common mode range (V_{REF} Max of V_{CC} –1.0 VDC)

[3] V_{REF} = 50 MVDC with V+ = 0 V to 150 mV step

[4] V_{REF} = 1.4 VDC with V+ = 0 V to V_{CC} –1.0 V logic swing

[5] The comparator will exhibit proper output state if one of the inputs becomes greater than V_{DD}, the other input must remain within the common mode range. The low input state cannot be less than –0.3 V of V_{SS}.

[6] V+ = 0 V to V_{CC} logic swing with V_{REF} in common mode range.

[7] Both inputs must be in common mode voltage range.

[8] Freq means the internal system clock frequency.

AC ELECTRICAL CHARACTERISTICS

Low Noise Mode

				T_A = 0°C to +70°C				T_A = −40°C to +105°C					
				1 MHz		4 MHz		1 MHz		4 MHz			
No	Symbol	Parameter	V_{CC}[3]	Min	Max	Min	Max	Min	Max	Min	Max	Units	Notes
5	TwTinH	Timer Input High Width	3.0V	2.5TpC		2.5TpC		2.5TpC		2.5TpC			[1]
			5.5V	2.5TpC		2.5TpC		2.5TpC		2.5TpC			[1]
6	TpTin	Timer Input Period	3.0V	4TpC		4TpC		4TpC		4TpC			[1]
			5.5V	4TpC		4TpC		4TpC		4TpC			[1]
7	TrTin,	Timer Input Rise	3.0V		100		100		100		100	ns	[1]
	TtTin	and Fall Timer	5.5V		100		100		100		100	ns	[1]
8	TwIL	Int. Request Input	3.0V	100		100		100		100		ns	[1,2]
		Low Time	5.5V	70		70		70		70		ns	[1,2]
9	TwIH	Int. Request Input	3.0V	2.5TpC		2.5TpC		2.5TpC		2.5TpC			[1]
		High Time	5.5V	2.5TpC		2.5TpC		2.5TpC		2.5TpC			[1,2]
10	Twdt	Watch-Dog Timer	3.0V	25		25		25		25		ms	[1,4]
		Delay Time	5.5V	5		5		5		5		ms	[1,4]

Notes:

[1] Timing Reference uses 0.7 V_{CC} for a logic 1 and 0.2 V_{CC} for a logic 0.

[2] Interrupt request through Port 3 (P33-P31).

[3] The V_{CC} Voltage specification of 3.0V guarantees 3.3V ±0.3V and V_{CC} voltage specification of 5.5V guarantees 5.0V ±0.5V.

[4] Length of time before WDT times out.

Z8 CONTROL REGISTER DIAGRAMS

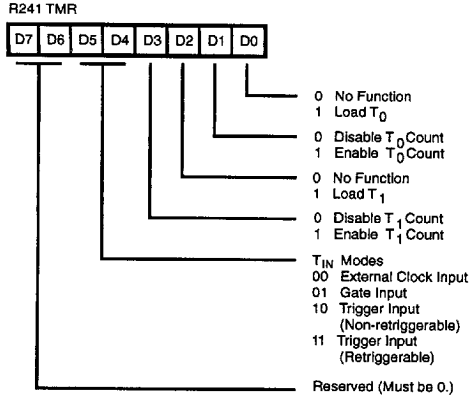


Figure 18. Timer Mode Register ($F1_H$: Read/Write)

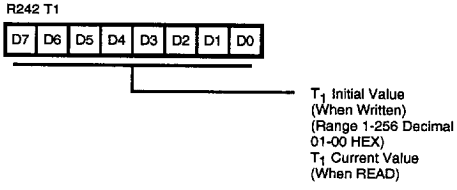


Figure 19. Counter Time 1 Register ($F2_H$: Read/Write)

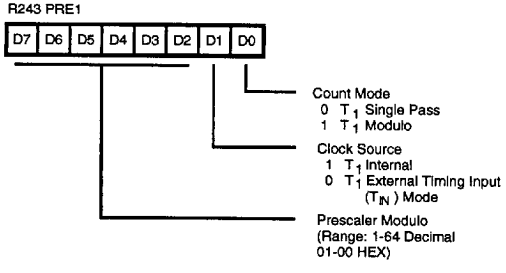


Figure 20. Prescaler 1 Register ($F3_H$: Write Only)

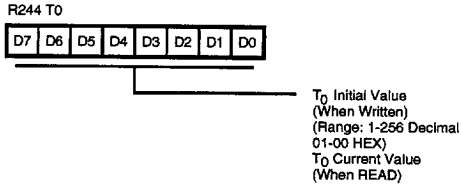


Figure 21. Counter/Timer 0 Register ($F4_H$: Read/Write)

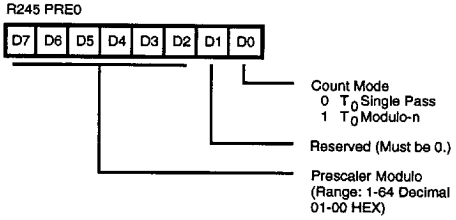


Figure 22. Prescaler 0 Register ($F5_H$: Write Only)

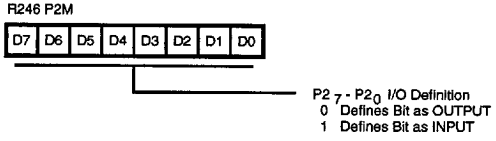


Figure 23. Port 2 Mode Register ($F6_H$: Write Only)

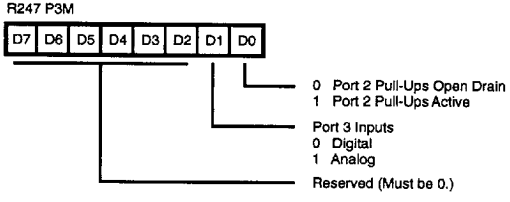


Figure 24. Port 3 Mode Register ($F7_H$: Write Only)

Z8 CONTROL REGISTER DIAGRAMS (Continued)

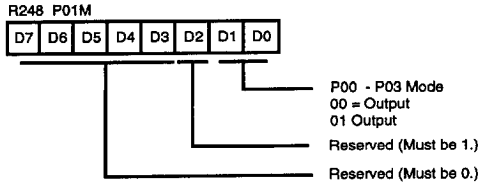


Figure 25. Port 0 and 1 Mode Register ($F8_H$: Write Only)

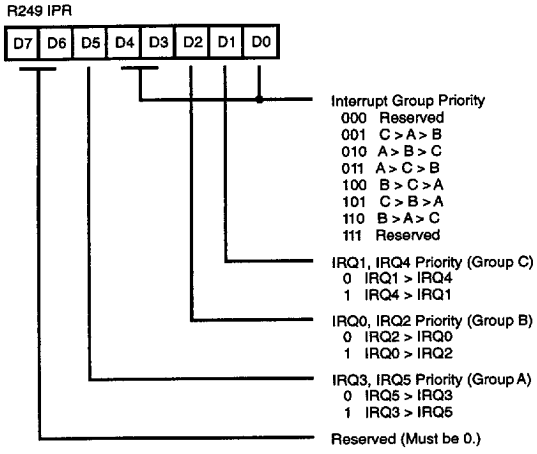


Figure 26. Interrupt Priority Register ($F9_H$: Write Only)

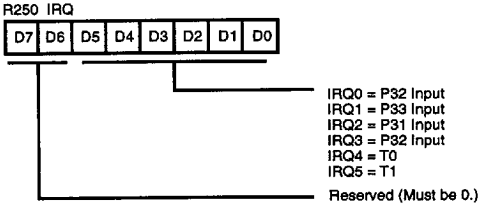


Figure 27. Interrupt Request Register (FA: Read/Write)

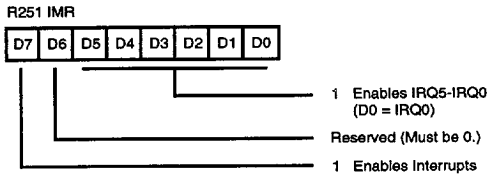


Figure 28. Interrupt Mask Register (FB_H: Read/Write)

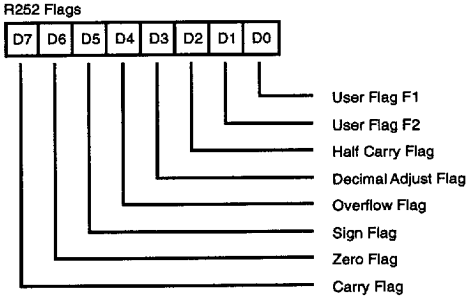


Figure 29. Flag Register (FC_H: Read/Write)

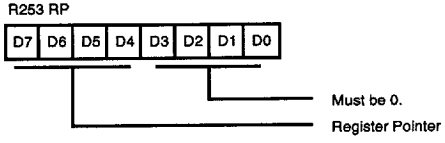


Figure 30. Register Pointer (FD_H: Read/Write)

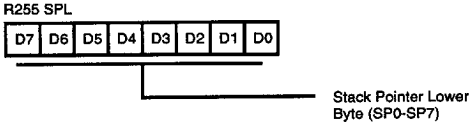


Figure 31. Stack Pointer (FF_H: Read/Write)

DEVICE CHARACTERISTICS

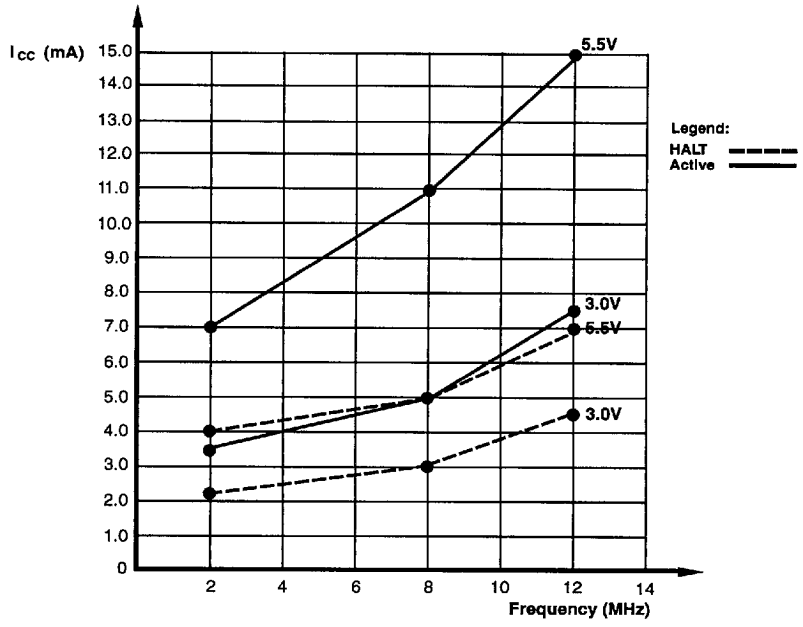


Figure 32. Maximum I_{cc} vs Frequency

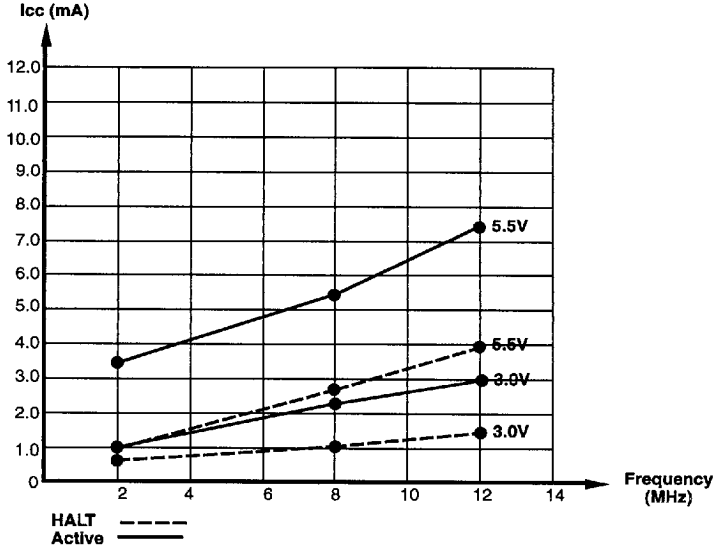


Figure 33. Typical I_{cc} vs Frequency

DEVICE CHARACTERISTICS (Continued)

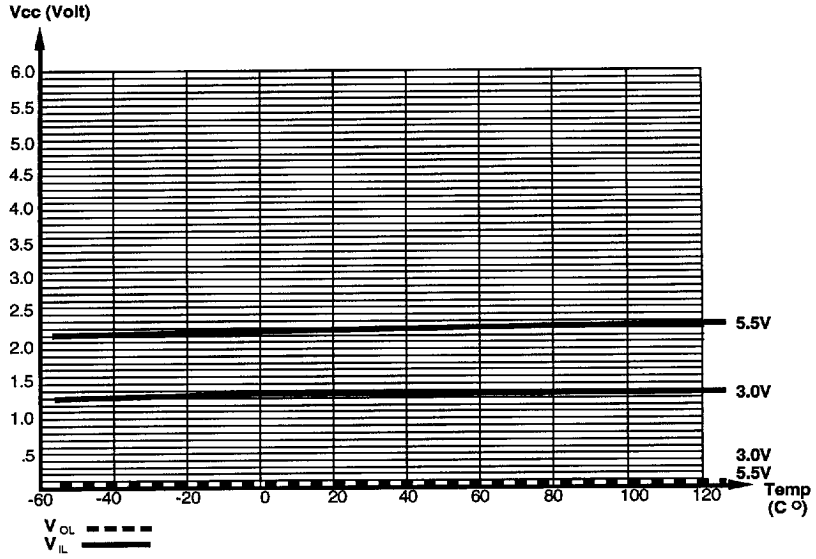


Figure 34. V_{IL}, V_{OL} **vs Temperature**

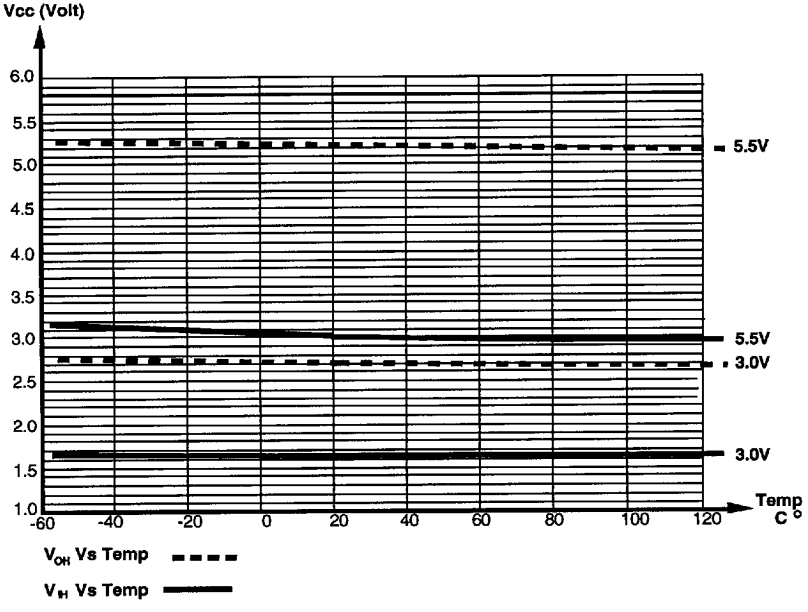


Figure 35. V_{IH}, V_{OH} **vs Temperature**

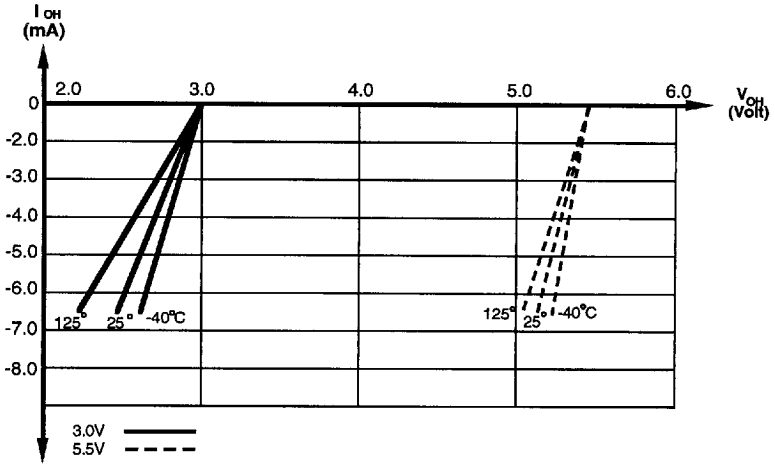


Figure 36. Typical I_{OH} vs V_{OH}

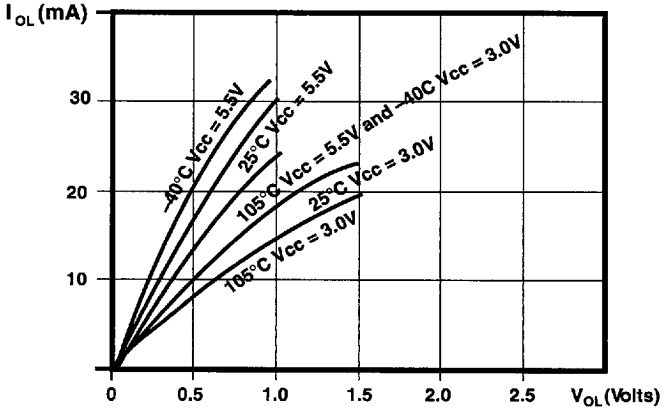


Figure 37. Typical I_{OL} vs V_{OL}

INSTRUCTION SET NOTATION

Addressing Modes. The following notation is used to describe the addressing modes and instruction operations as shown in the instruction summary.

Symbol	Meaning
IRR	Indirect register pair or indirect working-register pair address
Ir	Indirect working-register pair only
X	Indexed address
DA	Direct address
RA	Relative address
IM	Immediate
R	Register or working-register address
r	Working register address only
IR	Indirect-register or indirect working-register address
Ir	Indirect working-register address only
RR	Register pair or working register pair address

Symbols. The following symbols are used in describing the instruction set.

Symbol	Meaning
dst	Destination location or contents
src	Source location or contents
cc	Condition code
@	Indirect address prefix
SP	Stack pointer
PC	Program counter
FLAGS	Flag register (Control Register 252)
RP	Register Pointer (R253)
IMR	Interrupt mask register (R251)

Flags. Control register (R252) contains the following six flags.

Symbol	Meaning
C	Carry flag
Z	Zero flag
S	Sign flag
V	Overflow flag
D	Decimal-adjust flag
H	Half-carry flag

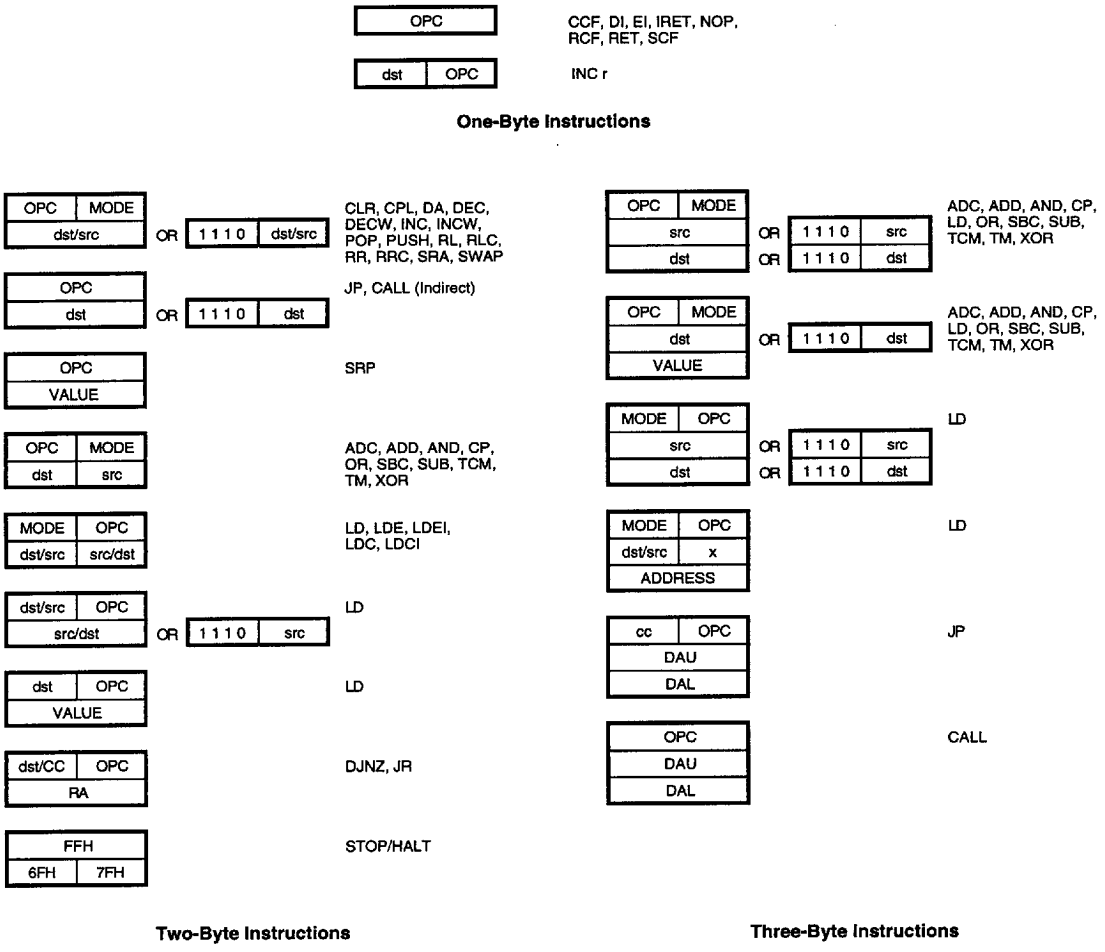
Affected flags are indicated by:

0	Clear to zero
1	Set to one
*	Set to clear according to operation
-	Unaffected
X	Undefined

CONDITION CODES

Value	Mnemonic	Meaning	Flags Set
1000	---	Always true	---
0111	C	Carry	C = 1
1111	NC	No Carry	C = 0
0110	Z	Zero	Z = 1
1110	NZ	Not zero	Z = 0
1101	PL	Plus	S = 0
0101	MI	Minus	S = 1
0100	OV	Overflow	V = 1
1100	NOV	No overflow	V = 0
0110	EQ	Equal	Z = 1
1110	NE	Not equal	Z = 0
1001	GE	Greater than or equal	(S XOR V) = 0
0001	LT	Less than	(S XOR V) = 1
1010	GT	Greater than	[Z OR (S XOR V)] = 0
0010	LE	Less than or equal	[Z OR (S XOR V)] = 1
1111	UGE	Unsigned greater than or equal	C = 0
0111	ULT	Unsigned less than	C = 1
1011	UGT	Unsigned greater than	(C = 0 AND Z = 0) = 1
0011	ULE	Unsigned less than or equal	(C OR Z) = 1
0000	F	Never True (Always False)	---

INSTRUCTION FORMATS



INSTRUCTION SUMMARY

Note: Assignment of a value is indicated by the symbol "←". For example:

dst ← dst + src

indicates that the source data is added to the destination data and the result is stored in the destination location. The notation "addr (n)" is used to refer to bit (n) of a given operand location. For example:

dst(7)

refers to bit 7 of the destination operand.

INSTRUCTION SUMMARY (Continued)

Instruction and Operation	Address Mode dst	Address Mode src	Opcode Byte (Hex)	Flags C	Z	S	V	D	H
ADC dst, src dst←dst + src +C	†		1[ ]	*	*	*	*	0	*
ADD dst, src dst←dst + src	†		0[ ]	*	*	*	*	0	*
AND dst, src dst←dst AND src	†		5[ ]	-	*	*	0	-	-
CALL dst SP←SP – 2 @SP←PC, PC←dst	DA IRR		D6 D4	-	-	-	-	-	-
CCF C←NOT C			EF	*	-	-	-	-	-
CLR dst dst←0	R IR		B0 B1	-	-	-	-	-	-
COM dst dst←NOT dst	R IR		60 61	-	*	*	0	-	-
CP dst, src dst – src	†		A[ ]	*	*	*	*	-	-
DA dst dst←DA dst	R IR		40 41	*	*	*	X	-	-
DEC dst dst←dst – 1	R IR		00 01	-	*	*	*	-	-
DECW dst dst←dst – 1	RR IR		80 81	-	*	*	*	-	-
DI IMR(7)←0			8F	-	-	-	-	-	-
DJNZr, dst r←r – 1 if r ≠ 0 PC←PC + dst Range: +127, –128	RA		rA r = 0 – F	-	-	-	-	-	-
EI IMR(7)←1			9F	-	-	-	-	-	-
HALT			7F	-	-	-	-	-	-

Instruction and Operation	Address Mode dst	Address Mode src	Opcode Byte (Hex)	Flags C	Z	S	V	D	H
INC dst dst←dst + 1	r R IR		rE r = 0 – F 20 21	-	*	*	*	-	-
INCW dst dst←dst + 1	RR IR		A0 A1	-	*	*	*	-	-
IRET FLAGS←@SP; SP←SP + 1 PC←@SP; SP←SP + 2; IMR(7)←1			BF	*	*	*	*	*	*
JP cc, dst if cc is true, PC←dst	DA IRR		cD c = 0 – F 30	-	-	-	-	-	-
JR cc, dst if cc is true, PC←PC + dst Range: +127, –128	RA		cB c = 0 – F	-	-	-	-	-	-
LD dst, src dst←src	r r R r X r Ir R R R IR IR	Im R r X r Ir r R IR IM IM R	rC r8 r9 r = 0 – F C7 D7 E3 F3 E4 E5 E6 E7 F5	-	-	-	-	-	-
LDC dst, src dst←src	r	Irr	C2	-	-	-	-	-	-
LDCI dst, src dst←src r←r + 1;rr←rr + 1	Ir	Irr	C3	-	-	-	-	-	-
NOP			FF	-	-	-	-	-	-

INSTRUCTION SUMMARY (Continued)

Instruction and Operation	Address Mode dst src	Opcode Byte (Hex)	Flags Affected C Z S V D H
OR dst, src dst←dst OR src	†	4[ ]	- * * 0 - -
POP dst dst←@SP; SP←SP + 1	R IR	50 51	- - - - - -
PUSH src SP←SP – 1; @SP←src	R IR	70 71	- - - - - -
RCF C←0		CF	0 - - - - -
RET PC←@SP; SP←SP + 2		AF	- - - - - -
RL dst	R IR	90 91	* * * * - -
RLC dst	R IR	10 11	* * * * - -
RR dst	R IR	E0 E1	* * * * - -
RRC dst	R IR	C0 C1	* * * * - -
SBC dst, src dst←dst–src–C	†	3[ ]	* * * * 1 *
SCF C←1		DF	1 - - - - -
SRA dst	R IR	D0 D1	* * * 0 - -
SRP dst RP←src	Im	31	- - - - - -

Instruction and Operation	Address Mode dst src	Opcode Byte (Hex)	Flags Affected C Z S V D H
STOP		6F	1 - - - - -
SUB dst, src dst←dst–src	†	2[ ]	* * * * 1 *
SWAP dst	R IR	F0 F1	X * * X - -
TCM dst, src (NOT dst) AND src	†	6[ ]	- * * 0 - -
TM dst, src dst AND src	†	7[ ]	- * * 0 - -
WDH		4F	- - - - - -
WDT		5F	- X X X - -
XOR dst, src dst←dst XOR src	†	B[ ]	- * * 0 - -

Notes:

† These instructions have an identical set of addressing modes, which are encoded for brevity. The first opcode nibble is found in the instruction set table above. The second nibble is expressed symbolically by a '[ ]' in this table, and its value is found in the following table to the left of the applicable addressing mode pair.

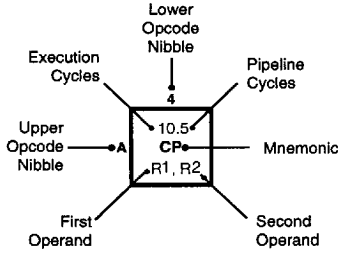
For example, the opcode of an ADC instruction using the addressing modes r (destination) and Ir (source) is 13.

Address Mode dst	Address Mode src	Lower Opcode Nibble
r	r	[2]
r	Ir	[3]
R	R	[4]
R	IR	[5]
R	IM	[6]
IR	IM	[7]

OPCODE MAP

Lower Nibble (Hex)

Upper Nibble (Hex)	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	6.5 **DEC** R1	6.5 **DEC** IR1	6.5 **ADD** r1, r2	6.5 **ADD** r1, Ir2	10.5 **ADD** R2, R1	10.5 **ADD** IR2, R1	10.5 **ADD** R1, IM	10.5 **ADD** IR1, IM	6.5 **LD** r1, R2	6.5 **LD** r2, R1	12/10.5 **DJNZ** r1, RA	12/10.0 **JR** cc, RA	6.5 **LD** r1, IM	12.10.0 **JP** cc, DA	6.5 **INC** r1	
1	6.5 **RLC** R1	6.5 **RLC** IR1	6.5 **ADC** r1, r2	6.5 **ADC** r1, Ir2	10.5 **ADC** R2, R1	10.5 **ADC** IR2, R1	10.5 **ADC** R1, IM	10.5 **ADC** IR1, IM								
2	6.5 **INC** R1	6.5 **INC** IR1	6.5 **SUB** r1, r2	6.5 **SUB** r1, Ir2	10.5 **SUB** R2, R1	10.5 **SUB** IR2, R1	10.5 **SUB** R1, IM	10.5 **SUB** IR1, IM								
3	8.0 **JP** IRR1	6.1 **SRP** IM	6.5 **SBC** r1, r2	6.5 **SBC** r1, Ir2	10.5 **SBC** R2, R1	10.5 **SBC** IR2, R1	10.5 **SBC** R1, IM	10.5 **SBC** IR1, IM								
4	8.5 **DA** R1	8.5 **DA** IR1	6.5 **OR** r1, r2	6.5 **OR** r1, Ir2	10.5 **OR** R2, R1	10.5 **OR** IR2, R1	10.5 **OR** R1, IM	10.5 **OR** IR1, IM								6.0 **WDH**
5	10.5 **POP** R1	10.5 **POP** IR1	6.5 **AND** r1, r2	6.5 **AND** r1, Ir2	10.5 **AND** R2, R1	10.5 **AND** IR2, R1	10.5 **AND** R1, IM	10.5 **AND** IR1, IM								6.0 **WDT**
6	6.5 **COM** R1	6.5 **COM** IR1	6.5 **TCM** r1, r2	6.5 **TCM** r1, Ir2	10.5 **TCM** R2, R1	10.5 **TCM** IR2, R1	10.5 **TCM** R1, IM	10.5 **TCM** IR1, IM								6.0 **STOP**
7	10/12.1 **PUSH** R2	12/14.1 **PUSH** IR2	6.5 **TM** r1, r2	6.5 **TM** r1, Ir2	10.5 **TM** R2, R1	10.5 **TM** IR2, R1	10.5 **TM** R1, IM	10.5 **TM** IR1, IM								7.0 **HALT**
8	10.5 **DECW** RR1	10.5 **DECW** IR1														6.1 **DI**
9	6.5 **RL** R1	6.5 **RL** IR1														6.1 **EI**
A	10.5 **INCW** RR1	10.5 **INCW** IR1	6.5 **CP** r1, r2	6.5 **CP** r1, Ir2	10.5 **CP** R2, R1	10.5 **CP** IR2, R1	10.5 **CP** R1, IM	10.5 **CP** IR1, IM								14.0 **RET**
B	6.5 **CLR** R1	6.5 **CLR** IR1	6.5 **XOR** r1, r2	6.5 **XOR** r1, Ir2	10.5 **XOR** R2, R1	10.5 **XOR** IR2, R1	10.5 **XOR** R1, IM	10.5 **XOR** IR1, IM								16.0 **IRET**
C	6.5 **RRC** R1	6.5 **RRC** IR1	12.0 **LDC** r1, Irr2	18.0 **LDCI** Ir1, Irr2				10.5 **LD** r1,x,R2								6.5 **RCF**
D	6.5 **SRA** R1	6.5 **SRA** IR1	12.0 **LDC** r1, Irr2	18.0 **LDCI** Ir1, Irr2	20.0 **CALL*** IRR1		20.0 **CALL** DA	10.5 **LD** r2,x,R1								6.5 **SCF**
E	6.5 **RR** R1	6.5 **RR** IR1		6.5 **LD** r1, IR2	10.5 **LD** R2, R1	10.5 **LD** IR2, R1	10.5 **LD** R1, IM	10.5 **LD** IR1, IM								6.5 **CCF**
F	8.5 **SWAP** R1	8.5 **SWAP** IR1		6.5 **LD** Ir1, r2		10.5 **LD** R2, IR1										6.0 **NOP**
Bytes per Instruction	2			3					2					3	1	



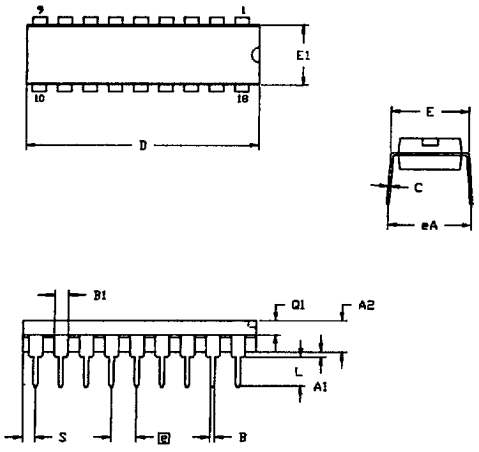
Legend:
R = 8-bit Address
r = 4-bit Address
R1 or r1 = Dst Address
R2 or r2 = Src Address

Sequence:
Opcode, First Operand, Second Operand

Note: Blank areas reserved.

*2-byte instruction appears as a 3-byte instruction

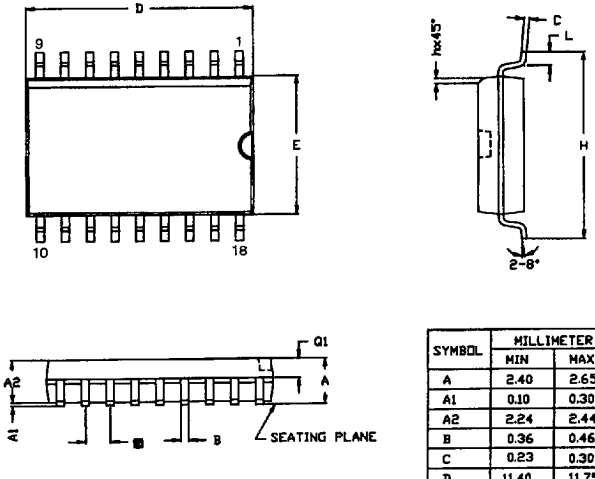
PACKAGE INFORMATION



SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A1	0.51	0.81	.020	.032
A2	3.25	3.43	.128	.135
B	0.38	0.53	.015	.021
B1	1.14	1.65	.045	.065
C	0.23	0.38	.009	.015
D	22.35	23.37	.880	.920
E	7.62	8.13	.300	.320
E1	6.22	6.48	.245	.255
e	2.54 TYP		.100 TYP	
eA	7.87	8.89	.310	.350
L	3.18	3.81	.125	.150
Q1	1.52	1.65	.060	.065
S	0.89	1.65	.035	.065

CONTROLLING DIMENSIONS : INCH

18-Pin DIP Package Diagram



CONTROLLING DIMENSIONS : MM
LEADS ARE COPLANAR WITHIN .004 INCH.

SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A	2.40	2.65	.094	.104
A1	0.10	0.30	.004	.012
A2	2.24	2.44	.088	.096
B	0.36	0.46	.014	.018
C	0.23	0.30	.009	.012
D	11.40	11.75	.449	.463
E	7.40	7.60	.291	.299
e	1.27 TYP		.050 TYP	
H	10.00	10.65	.394	.419
h	0.30	0.40	.012	.016
L	0.60	1.00	.024	.039
Q1	0.97	1.07	.038	.042

18-Pin SOIC Package Diagram

ORDERING INFORMATION

Z86B07 (8 MHz)

Standard Temperature		Extended Temperature	
18-Pin DIP	**18-Pin SOIC**	**18-Pin DIP**	**18-Pin SOIC**
Z86B0708PSC	Z86B0708SSC	Z86B0708PEC	Z86B0708SEC

Z86B07 (12 MHz)

Standard Temperature		Extended Temperature	
18-Pin DIP	**18-Pin SOIC**	**18-Pin DIP**	**18-Pin SOIC**
Z86B0712PSC	Z86B0712SSC	Z86B0712PEC	Z86B0712SEC

For fast results, contact your local Zilog sale offices for assistance in ordering the part desired.

CODES

Preferred Package
P = Plastic DIP

Longer Lead Time
S = SOIC

Preferred Temperature
S = 0°C to 70°C

Longer Lead Time
E = –40°C to +105°C

Speeds
08 = 8 MHz
12 = 12 MHz

Environmental
C = Plastic Standard

Example:

Z 86B07 08 P S C is a Z86B07, 8 MHz, DIP, 0°C to +70°C, Plastic Standard Flow