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54AC/74AC1010 • 54ACT/74ACT1010

T-45-07

16 x 16 Parallel Multiplier/Accumulator

Description

The 'AC/'ACT1010 is a high-speed, low-power 16 x 16 bit parallel multiplier with a 35-bit accumulator that is ideally suited for real-time digital signal processing applications. Fabricated using 1.3-micron FACT technology, the 'AC/'ACT1010 offers a very low power alternative (10% of the power of bipolar and NMOS counterparts) and exceptional speed (55 ns maximum multiply accumulate) performance.

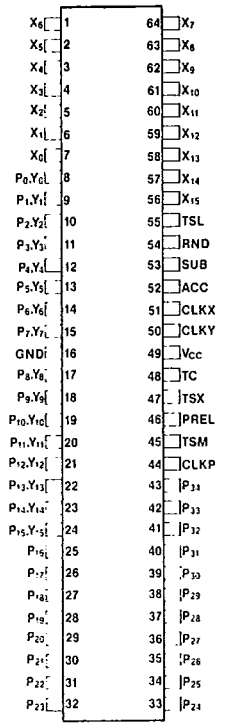
The 'AC/'ACT1010 is a pin and functional replacement for TRW's TDC1010; the 'ACT1010 operates from a single Vcc supply and is compatible with standard TTL logic levels.

The architecture of the 'AC/'ACT1010 features one 16-bit input port dedicated to the X input registers (controlled by CLKX), one 16-bit I/O port used for loading the Y input registers (controlled by CLKY) and for preloading and displaying the LSP of the P output registers (controlled by CLKP), one 16-bit I/O port for preloading and displaying the MSP of the P output registers (controlled by CLKP), and one 3-bit I/O port for loading and displaying the contents of the XTP (most significant bits) of the P output registers (also controlled by CLKP).

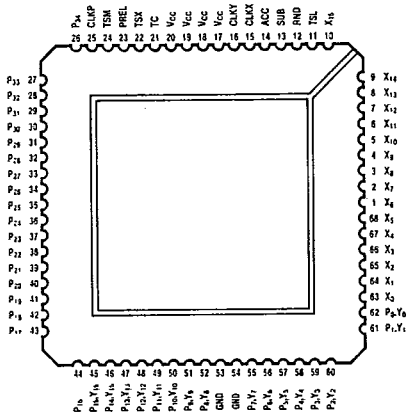
When the unregistered preload input (PREL) is active, all the output buffers are forced into a high impedance state. By using the 3-state controls (TSX, TSM and TSL) as register enables, external data is loaded on the rising edge of each CLKP pulse.

Both twos complement and unsigned magnitude arithmetic are supported through the registered TC line. The accumulator functions are enabled through the registered ACC line. When the registered SUB signal is active/inactive, the accumulator data is subtracted from/added to the multiplier product. The result is loaded into the accumulator registers for use in subsequent operations. The multiplier product is automatically sign extended for twos complement arithmetic with the accumulator. The registered RND signal controls rounding of the arithmetic result if active,

Connection Diagrams



Pin Assignment for DIP



Pin Assignment for PCC

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a '1' is added to the MSB of the LSP of multiplication result and then fed into the accumulator circuitry.

The function of the data busses, X, Y and P and the effect of the format pins, TC, RND, ACC, and SUB can be described mathematically by:

$$P[nT] = \sum_{i=0}^{15}\{X_i \cdot 2^i\} \cdot \sum_{i=0}^{15}\{Y_i \cdot 2^i\} + (-1)^{SUB} \cdot ACC \cdot \sum_{i=0}^{34}\{Pi[(n-1)T] \cdot 2^i\} + RND \cdot 2^{15}$$

where T is the clock period of CLKP, n represents the number of the clock cycle, X, Y, RND, ACC and SUB values are the values found in the registers t_{MA} ns before clock period n.

- **16 x 16 Parallel Multiplier/Accumulator**
- **High Speed—55 ns Multiply/Accumulate Time**
- **Selectable Accumulation, Subtraction, Rounding and Preloading with a 35-Bit Result**
- **Pin and Functionally Compatible with the TRW TDC1010J**
- **High Drive (8 mA) Output Capability**
- **Low Power Consumption (less than 250 mW typical)—Less Than 7% of the Power of Compatible Bipolar and 14% of the Power of NMOS Designs**
- **Inputs and Outputs Directly TTL-Compatible**
- **Single Vcc Supply**
- **± 2000 V ESD Protection**

Ordering Code: See Section 6

Pin Names

X_0 - X_{15}	Multiplicand Data Inputs
Y_0 - Y_{15}	Multiplier Data Inputs
CLKX, CLKY	Input Clocks
ACC	Accumulate Input
SUB	Subtract Input
RND	Round Input
PREL	Preload Input
TC	Twos Complement Control Input
TSM, TSX, TSL	3-State Output Controls
CLKP	Output Clock
P_{15} - P_0	Least Significant Product (LSP)
P_{31} - P_{16}	Most Significant Product (MSP)
P_{34} - P_{32}	Extended Product Output (XTP)

Block Diagram

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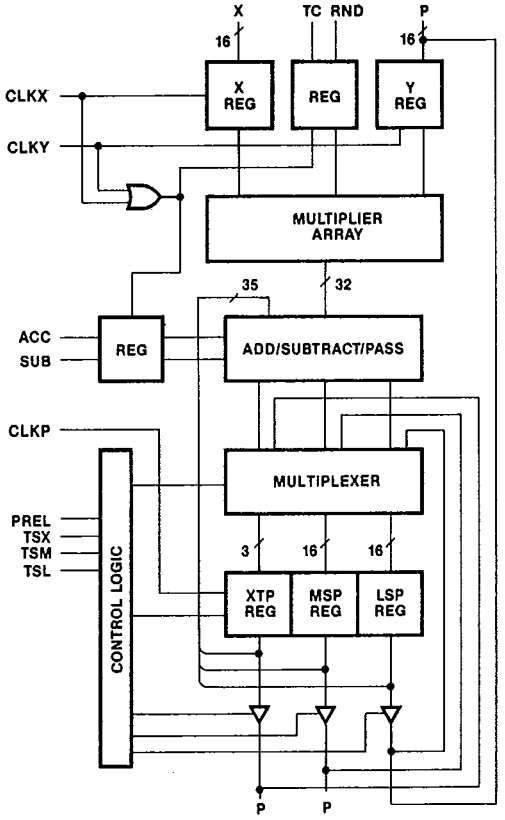

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Functional Description

Signal Descriptions

Inputs:	
XIN (X_{15} - X_0)	Multiplicand Data Inputs
YIN (Y_{15} - Y_0)	Multiplier Data Inputs
Input Clocks:	
CLKX, CLKY	Input data is loaded on the rising edge of these clocks.
Outputs:	
XTP (P_{34} - P_{32})	Extended Product Output (3-bits)
MSP (P_{31} - P_{16})	Most Significant Product
LSP (P_{15} - P_0)	Least Significant Product
Output Clock:	
CLKP	Output data is loaded into the output register on the rising edge of this clock.

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Controls

ACC (Accumulate)
When ACC is HIGH, the contents of the output registers (XTP, MSP and LSP) are added to or subtracted from the multiplier output. When ACC is LOW, the device acts as a simple multiplier with no accumulation being performed and the next product generated will be stored directly into the output registers. The ACC signal is loaded on the rising edge of the CLKX or CLKY and must be valid for the duration of the data input.

SUB (Subtract)
When the ACC and SUB signals are both HIGH, the contents of the output registers are subtracted from the next product generated and the difference is stored back into the output registers at the rising edge of the next CLKP. When ACC is HIGH and SUB is LOW, an addition instead of a subtraction is performed. Like the ACC signal, the SUB signal is loaded into the SUB register at the rising edge of either CLKX or CLKY and must be valid over the same period as the input data is valid. When the ACC is LOW, SUB acts as a "don't care" input.

RND (Round)
A HIGH level at this input adds a '1' to the most significant bit of the LSP to round up the XTP and MSP data. RND, like ACC and SUB, is loaded on the rising edge of either CLKX or CLKY and must be valid for the duration of the input data.

PREL (Preload)
When the PREL input is HIGH, the output is driven to a HIGH impedance state. When the TSX, TSL and TSM inputs are also high, the contents of the output register can be preset to the preload data applied to the output pins at the rising of CLKP. The PREL, TSM, TSL and TSX inputs must all be valid over the same period that the preload input is valid.

YIN/LSP Output
Shares functions between 16-bit data input (YIN) and the least significant product output (LSP).

TSX, TSL, TSM (3-State Output Controls)
The XTP, MSP and LSP registers are controlled by direct non-registered control signals. These output drivers are at high impedance (disabled) when control signals TSX, TSM and TSL are HIGH and are enabled when TSX, TSM and TSL are LOW.

Notes on Twos Complement Formats

1. In twos complement notation, the location of the binary point that signifies the separation of the fractional and integer fields is just after the sign, between the sign bit (-2^0) and the next significant bit for the multiplier inputs. This same format is carried over to the output format, except that the extended significance of the integer field is provided to extend the utility of the accumulator. In the case of the output notation, the output binary point is located between the -2^0 and 2^{-1} bit positions. The location of the binary point is arbitrary, as long as there is consistency with both the input and output formats. The number field can be considered entirely integer with the binary point just to the right of the least significant bit for the input, product and the accumulated sum.

2. When in the non-accumulating mode, the first four bits (P_{34} to P_{31}) will all indicate the sign of the product. Additionally, the P_{30} term will also indicate the sign except for one exceptional case when multiplying $(-1) \times (-1)$. With the additional bits that are available in this multiplier, the $(-1) \times (-1)$ is a valid operation that yields a $(+1)$ product.

3. In operations that require the accumulation of single products or sum of products, there is no change in format. To allow for a valid summation beyond the available for a single multiplication product, three additional significant bits (guard bits) are provided. This is the same as if the product was accumulated off-chip in a separate 35-bit wide adder. Taking the sign at the most significant bit position will guarantee that the largest number field will be used. When the accumulated sum only occupies the right hand portion of the accumulator, the sign will be extended into the lesser significant bit positions.

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Preload Truth Table

PREL	TSX	TSM	TSL	XTP	MSP	LSP
0	0	0	0	Q	Q	Q
0	0	0	1	Q	Q	High Z
0	0	1	0	Q	High Z	Q
0	0	1	1	Q	High Z	High Z
0	1	0	0	High Z	Q	Q
0	1	0	1	High Z	Q	High Z
0	1	1	0	High Z	High Z	Q
0	1	1	1	High Z	High Z	High Z
1	0	0	0	High Z	High Z	High Z
1	0	0	1	High Z	High Z	PL
1	0	1	0	High Z	PL	High Z
1	0	1	1	High Z	PL	PL
1	1	0	0	PL	High Z	High Z
1	1	0	1	PL	High Z	PL
1	1	1	0	PL	PL	High Z
1	1	1	1	PL	PL	PL

Notes:

High Z = Output buffers at high impedance (output disabled).

Q = Output buffers at low impedance. Contents of output register will be transferred to output pins.

PL = Output buffers at high impedance, or output disabled. Preload data supplied externally at output pins will be loaded into the output register at the rising edge of CLKP.

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Figure 1: Fractional Twos Complement Notation

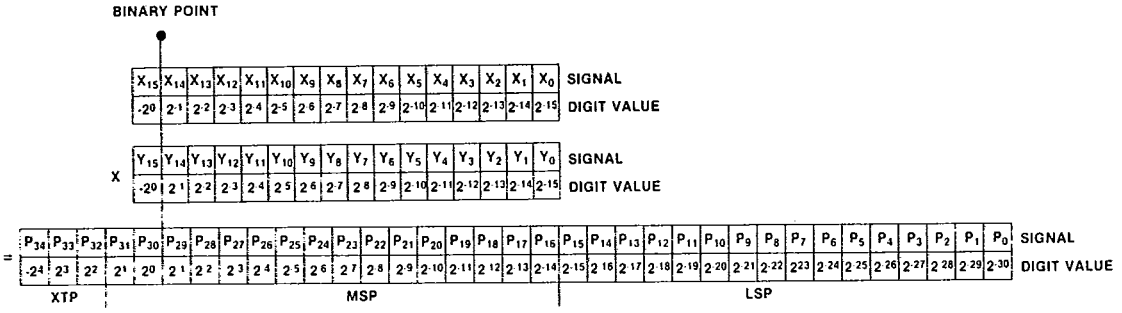


Figure 2: Fractional Unsigned Magnitude Notation

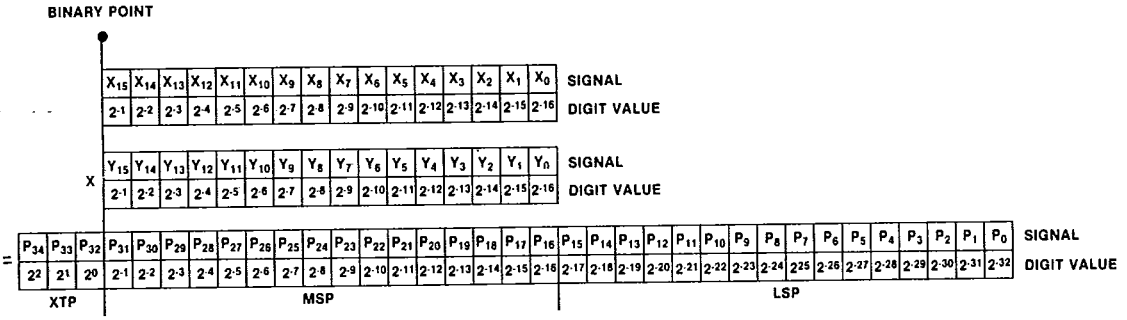


Figure 3: Integer Twos Complement Notation

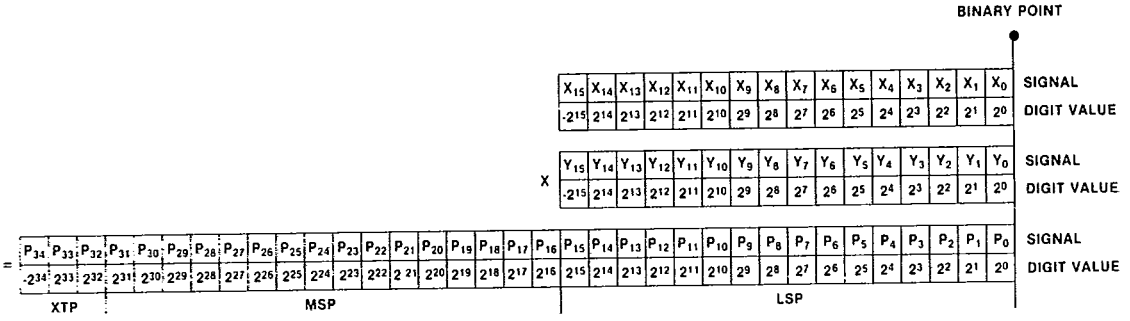
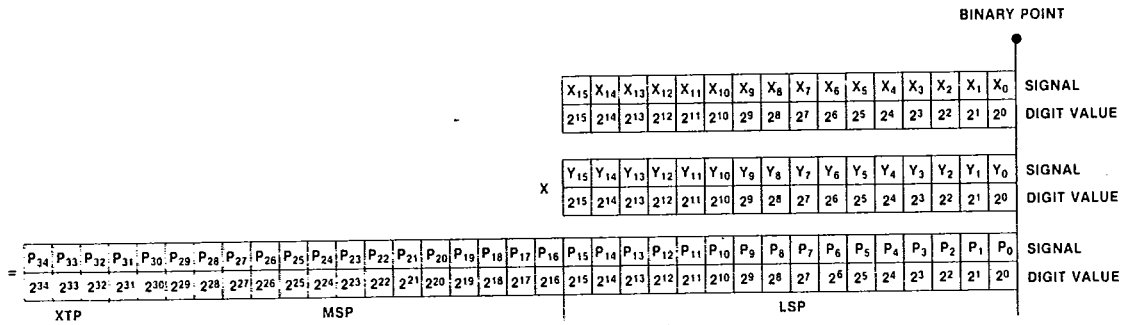


Figure 4: Integer Unsigned Magnitude Notation



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Recommended Operating Conditions

Symbol	Parameter		Conditions	Limits	Units
V_{CC}	Supply Voltage (unless otherwise specified)			2.0 to 6.0	V
V_I	Input Voltage			0 to V_{CC}	V
V_O	Output Voltage			0 to V_{CC}	V
T_A	Operating Temperature	74AC/ACT 54AC/ACT		−40 to +85 −55 to +125	°C °C
Sr	Maximum Slew Rate (except for Schmitt inputs)		V_{IN} V_{meas} V_{CC}@4.5V V_{CC}@5.5V	0.8 to 2.0 0.8 to 2.0 10.0 8.0	V V ns ns

Absolute Maximum Ratings*

Symbol	Parameter	Conditions	Limits	Units
V_{CC}	Supply Voltage		−0.5 to 7.0	V
I_{IK} or V_I	DC Input Diode Current or DC Input Voltage	$V_I = -0.5$ $V_I = V_{CC} + 0.5$	−20 20 −0.5 to V_{CC} + 0.5	mA mA V
I_{OK} or V_O	DC Output Diode Current or DC Output Voltage	$V_O = -0.5$ $V_O = V_{CC} + 0.5$	−20 20 −0.5 to V_{CC} + 0.5	mA mA V
I_O	DC Output Source or Sink Current, Per Output Pin		±15	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current		±20	mA
T_{STG}	Storage Temperature		−65 to 150	°C

*Absolute maximum ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied.

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AC Test Conditions

Input Pulse Levels	GND to 3.0 V
Input Rise and Fall Times	3 ns
Input Timing Reference Levels	1.5 V
Output Reference Levels	1.5 V
Output Load	See Figures 5 and 6

Capacitance (T_A = +25°C, f = 1.0 MHz)

Symbol		Max	Unit	Conditions
C_{IN}	Input Capacitance	7.0	pF	V_{IN} = 0V
C_{OUT}	Output Capacitance	5.0	pF	V_{OUT} = 0V

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DC Characteristics over Operating Temperature Range (unless otherwise specified)

Symbol	Parameter	74AC/ACT 25°C	54AC/ACT	74AC/ACT	Units	Conditions
		Typ	Guaranteed Limit			
I_{IN}	Maximum Input Current		0.1	10.0	1.0	μA	V_{CC} = Max V_{IN} = V_{CC}
I_{OZ}	Maximum 3-State Current		0.5	10.0	5.0	μA	High Z, V_{CC} = Max V_{OUT} = 0 to V_{CC}
I_{CCQ}	Supply Current, Quiescent	1.0	2.0	10.0	10.0	mA	V_{CC} = Max, V_{IN} = 0 V TSL, TSM, TSX = 5.0 V
I_{CCD}	Supply Current, 12.4 MHz Loaded	300		325	325	mA	V_{CC} = Max, f = 12.4 MHz TSL, TSM, TSX = 5.0 V Test Load: See Note 1
I_{CCD}	Supply Current, 20 MHz Loaded	325		350	350	mA	V_{CC} = Max, f = 20 MHz TSL, TSM, TSX = 5.0 V Test Load: See Note 1
V_{OH}	Minimum High Level Output	4.49	4.4	4.4	4.4	V	V_{IN} = V_{IL} or V_{IH} I_{OUT} = 20 μA, V_{CC} = 4.5 V
		5.49	5.4	5.4	5.4	V	V_{IN} = V_{IL} or V_{IH} I_{OUT} = 20 μA, V_{CC} = 5.5 V
			3.86	3.70	3.76	V	I_{OH} = −8 mA, V_{CC} = 4.5 V
			4.86	4.70	4.76	V	I_{OH} = −8 mA, V_{CC} = 5.5 V
V_{OL}	Maximum High Level Output	0.001	0.1	0.1	0.1	V	V_{IN} = V_{IL} or V_{IH}, I_{OUT} = 20 μA, V_{CC} = 4.5 V
		0.001	0.1	0.1	0.1	V	V_{IN} = V_{IL} or V_{IH}, I_{OUT} = 20 μA, V_{CC} = 5.5 V
			0.32	0.4	0.37	V	I_{OL} = 8 mA, V_{CC} = 4.5 V
			0.32	0.4	0.37	V	I_{OL} = 8 mA, V_{CC} = 5.5 V
I_{OLD}	Minimum Dynamic Output Current			32	32	mA	V_{CC} = 5.5 V V_{OLD} = 2.2 V
I_{OHD}	Minimum Dynamic Output Current			−32	−32	mA	V_{CC} = 5.5 V V_{OHD} = 3.3 V

Note 1: Test Load 50 pf, 500 ohm to Ground

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AC Characteristics

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Symbol	Parameter	Vcc* (V)	54AC TA = −55°C to +125°C				74AC TA = −40°C to +85°C				Units	Fig. No.
			1010-60		1010-70		1010-55		1010-65			
			Min	Max	Min	Max	Min	Max	Min	Max		
t_{MA}	Multiply-Accumulate Time	3.3 5.0									ns	5
t_D	Output Delay	3.3 5.0									ns	5
t_{ENA}	3-State Output[1] Enable Delay	3.3 5.0									ns	6
t_{DIS}	3-Stage Output[1] Disable Delay	3.3 5.0									ns	6
t_s	Input Register Setup Time	3.0 5.0									ns	7, 9
t_h	Input Register Hold Time	3.3 5.0									ns	7, 9
t_w	Clock Pulse Width	3.3 5.0									ns	9

PRELIMINARY

Note 1: Transition is measured to ±500 mV from steady state voltage with loading specified in Figure 6.

*Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

Military parameters given herein are for general references only. For current military specifications and subgroup testing information please request Fairchild's Table I data sheet from your Fairchild sales engineer or account representative.

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AC Characteristics

Symbol	Parameter	Vcc* (V)	54ACT TA = −55°C to +125°C				74ACT TA = −40°C to +85°C				Units	Fig. No.
			1010-60		1010-70		1010-55		1010-65			
			Min	Max	Min	Max	Min	Max	Min	Max		
t_{MA}	Multiply-Accumulate Time	5.0						55.0		65.0	ns	5
t_D	Output Delay	5.0						19.5		19.5	ns	5
t_{ENA}	3-State Output[1] Enable Delay	5.0						14.0		14.0	ns	6
t_{DIS}	3-Stage Output[1] Disable Delay	5.0						14.0		14.0	ns	6
t_s	Input Register Setup Time	5.0					5.0		5.0		ns	7, 9
t_h	Input Register Hold Time	5.0					1.0		1.0		ns	7, 9
t_w	Clock Pulse Width	5.0					3.5		3.5		ns	9

Note 1: Transition is measured to ±500 mV from steady state voltage with loading specified in Figure 6.

*Voltage Range 5.0 is 5.0 V ± 0.5 V

Military parameters given herein are for general references only. For current military specifications and subgroup testing information please request Fairchild's Table I data sheet from your Fairchild sales engineer or account representative.

Figure 5: AC Output Test Load

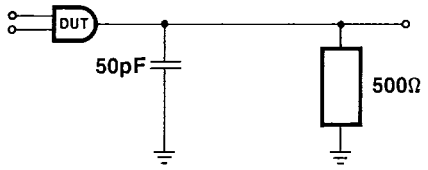

Figure 6: Output 3-State Delay Load

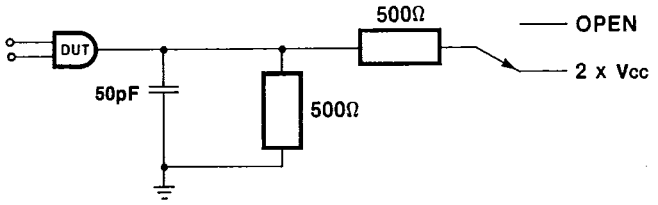

Figure 7: Setup and Hold Time

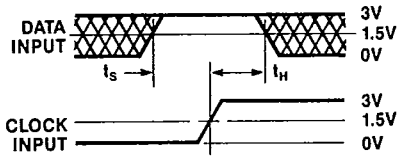

Figure 8: State Control Timing

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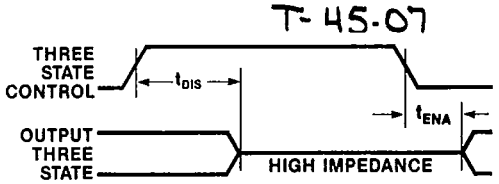
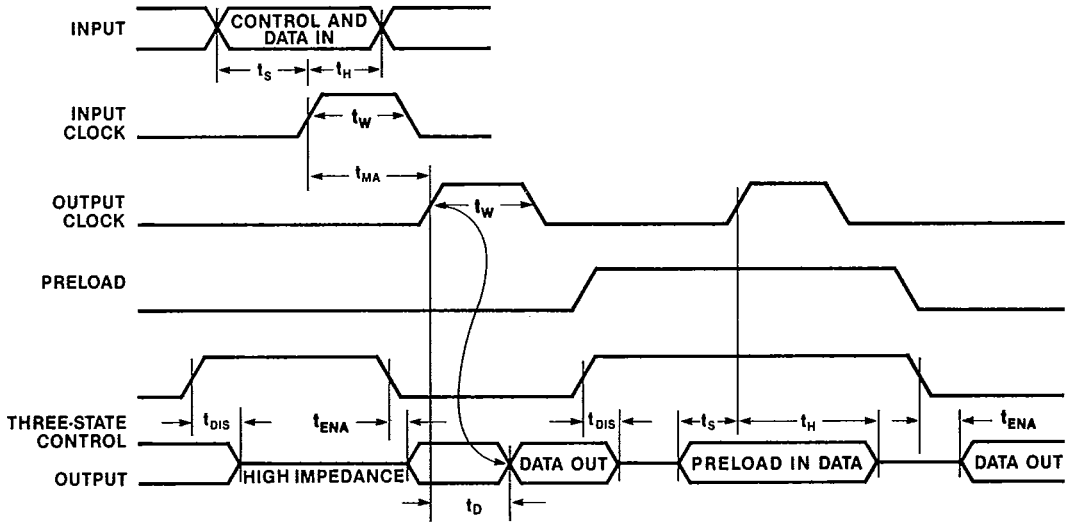


Figure 9: Timing Diagram



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