Ordering number : ENN*7773

CMOS IC

LC8774C8B/B2B/96B/80B

8 Bit Single Chip Microcontroller Incorporating 128K/112K/96K/80K Byte ROM and 4096 Byte RAM on Chip

Preliminary

Overview

The LC8774C8B, LC8774B2B, LC877496B and LC877480B are 8 bit single chip microcontrollers with the following on-chip functional blocks:

- CPU: operable at a minimum bus cycle time of 100ns
- On-chip ROM Maximum Capacity:

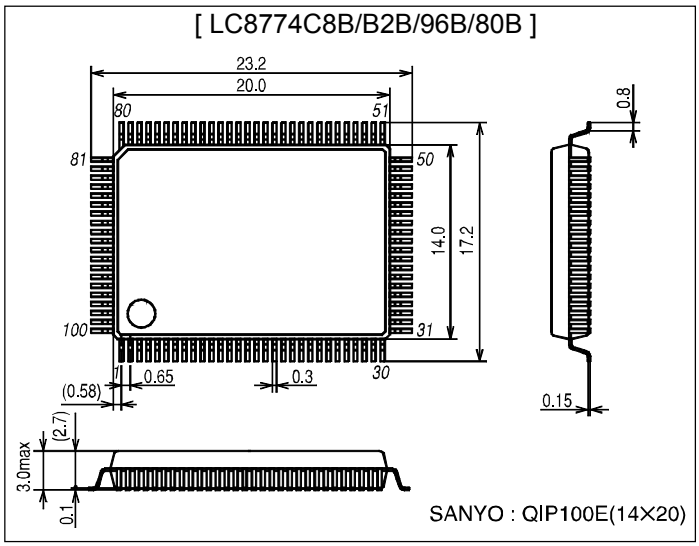
LC8774C8B	128K bytes
LC8774B2B	112K bytes
LC877496B	96K bytes
LC877480B	80K bytes

- On-chip RAM capacity: 4096 bytes
- LCD controller / driver
- 16 bit timer / counter (can be divided into 8 bit timer)
- 16 bit timer (can be divided into 8 bit timer, 8 bit timer can be PWM)
- Four 8 bit timer with prescalers
- Timer for use as date / time clock
- Synchronous serial I/O port (with automatic block transmit / receive function)
- Asynchronous / synchronous serial I/O port
- 15 channel × 8 bit AD converter
- Small signal detector
- High-speed clock counter
- System clock divider
- 20 source 10 vectored interrupt system

Package Dimensions

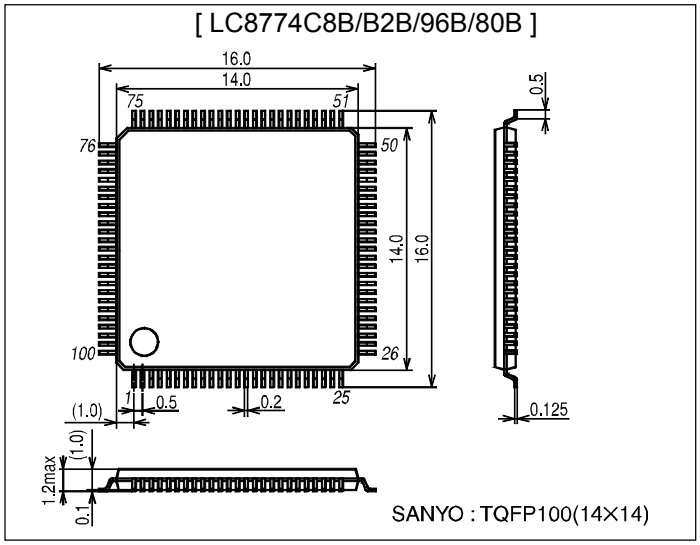
unit: mm

3151A



unit: mm

3274



SANYO Electric Co.,Ltd. Semiconductor Company

TOKYO OFFICE Tokyo Bldg., 1-10, 1 Chome, Ueno, Taito-ku, TOKYO, 110-8534 JAPAN

Features

(1) Read-Only Memory (ROM)
- 49152 × 8 bits (LC877148A)
- 40960 × 8 bits (LC877140A)
- 32768 × 8 bits (LC877132A)
- 24576 × 8 bits (LC877124A)

(2) Random Access Memory (RAM): 4096 × 9 bits (LC8774C8B, LC8774B2B, LC877496B, LC877480B)

(3) Minimum Bus Cycle Time: 100 ns (10MHz)
Note: The bus cycle time indicates ROM read time.

(4) Minimum Instruction Cycle Time: 300 ns (10MHz)

(5) Ports
- Input / output ports
  - Data direction programmable for each bit individually: 26 (P1n, P30 to P35, P70 to P73, P8n)
  - Data direction programmable in nibble units: 8 (P0n)
  - (When N-channel open drain output is selected, data can be input in bit units.)
- Input ports: 2 (XT1, XT2)
- LCD ports
  - Segment output: 48 (S00 to S47)
  - Common output: 4 (COM0 to COM3)
  - Bias terminals for LCD driver: 3 (V1 to V3)

Other functions
- Input / output ports: 48 (PAn, PBn, PCn, PDn, PEn, PFn)
- Input ports: 7 (PLn)
- Oscillator pins: 2 (CF1, CF2)
- Reset pin: 1 ($\overline{\text{RES}}$)
- Power supply: 6 (V_{SS}1 to 3, V_{DD}1 to 3)

(6) LCD controller
- Seven display modes are available (static, 1/2, 1/3, 1/4 duty × 1/2, 1/3 bias)
- Segment output and common output can be switched to general purpose input / output ports.

(7) Small signal detection (MIC signals etc)
- Counts pulses with the level which is greater than a preset value
- 2 bit counter

(8) Timers
- Timer 0: 16 bit timer / counter with capture register
  - Mode 0: 2 channel 8 bit timer with programmable 8 bit prescaler and 8 bit capture register
  - Mode 1: 8 bit timer with 8 bit programmable prescaler and 8 bit capture register + 8 bit counter with 8 bit capture register
  - Mode 2: 16 bit timer with 8 bit programmable prescaler and 16 bit capture register
  - Mode 3: 16 bit counter with 16 bit capture register
- Timer 1: PWM / 16 bit timer / counter with toggle output function
  - Mode 0: 8 bit timer (with toggle output) + 8 bit timer / counter (with toggle output)
  - Mode 1: 2 channel 8 bit PWM
  - Mode 2: 16 bit timer / counter (with toggle output) Toggle output from lower 8 bits is also possible.
  - Mode 3: 16 bit timer (with toggle output) Lower order 8 bits can be used as PWM.
- Timer 4: 8 bit timer with 6 bit prescaler
- Timer 5: 8 bit timer with 6 bit prescaler
- Timer 6: 8 bit timer with 6 bit prescaler
- Timer 7: 8 bit timer with 6 bit prescaler

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- Base Timer
  1) The clock signal can be selected from any of the following:
     Sub-clock (32.768kHz crystal oscillator), system clock, and prescaler output from timer 0
  2) Interrupts of five different time intervals are possible.

(9) High-speed clock counter
- Countable up to 20MHz clock (when using 10MHz main clock)
- Real time output

(10) Serial-interface
- SIO 0: 8 bit synchronous serial interface
  1) LSB first / MSB first is selectable
  2) Internal 8 bit baud-rate generator (fastest clock period 4 / 3 tCYC)
  3) Consecutive automatic data communication (1 to 256 bits)
- SIO 1: 8 bit asynchronous / synchronous serial interface
  Mode 0: Synchronous 8 bit serial I_O (2-wire or 3-wire, transmit clock 2 to 512 tCYC)
  Mode 1: Asynchronous serial I_O (half duplex, 8 data bits, 1 stop bit, baud rate 8 to 2048 tCYC)
  Mode 2: Bus mode 1 (start bit, 8 data bits, transmit clock 2 to 512 tCYC)
  Mode 3: Bus mode 2 (start detection, 8 data bits, stop detection)

(11) AD converter
- 8 bits × 15 channels

(12) Remote control receiver circuit (connected to P73 / INT3 / T0IN terminal)
- Noise rejection function (noise rejection filter's time constant can be selected from 1 / 32 / 128 tCYC)

(13) Watchdog timer
- The watching time period is determined by an external RC.
- Watchdog timer can produce interrupt or system reset

(14) Interrupts: 20 sources, 10 vectors
1) Three priority (low, high and highest) multiple interrupts are supported.
   During interrupt handling, an equal or lower priority interrupt request is postponed.
2) If interrupt requests to two or more vector addresses occur at once, the higher priority interrupt takes precedence.
   In the case of equal priority levels, the vector with the lowest address takes precedence.

No.	Vector	Selectable level	Interrupt signal
1	00003H	X or L	INT0
2	0000BH	X or L	INT1
3	00013H	H or L	INT2 / T0L / INT4
4	0001BH	H or L	INT3 / Base timer / INT5
5	00023H	H or L	T0H
6	0002BH	H or L	T1L / T1H
7	00033H	H or L	SIO0
8	0003BH	H or L	SIO1
9	00043H	H or L	ADC / MIC / T6 / T7
10	0004BH	H or L	Port 0 / T4 / T5

- Priority Level: X > H > L
- For equal priority levels, vector with lowest address takes precedence.

(15) Subroutine stack levels: 2048 levels max. Stack is located in RAM.

(16) Multiplication and division
- 16 bit × 8 bit (executed in 5 cycles)
- 24 bit × 16 bit (12 cycles)
- 16 bit ÷ 8 bit (8 cycles)
- 24 bit ÷ 16 bit (12 cycles)

(17) Oscillation circuits
- On-chip RC oscillation for system clock use.
- CF oscillation for system clock use. (Rf built in, Rd external)
- Crystal oscillation low speed system clock use. (Rf built in, Rd external)
- On-chip frequency variable RC oscillation circuit for system clock use.

(18) System clock divider
- Low power consumption operation is available
- Minimum instruction cycle time (300ns, 600ns, 1.2µs, 2.4µs, 4.8µs, 9.6µs, 19.2µs, 38.4µs, 76.8µs can be switched by program (when using 10MHz main clock)

(19) Standby function
- HALT mode

  HALT mode is used to reduce power consumption. During the HALT mode, program execution is stopped but peripheral circuits keep operating (some parts of serial transfer operation stop.)
  1) Oscillation circuits are not stopped automatically.
  2) Released by the system reset or interrupts.
- HOLD mode

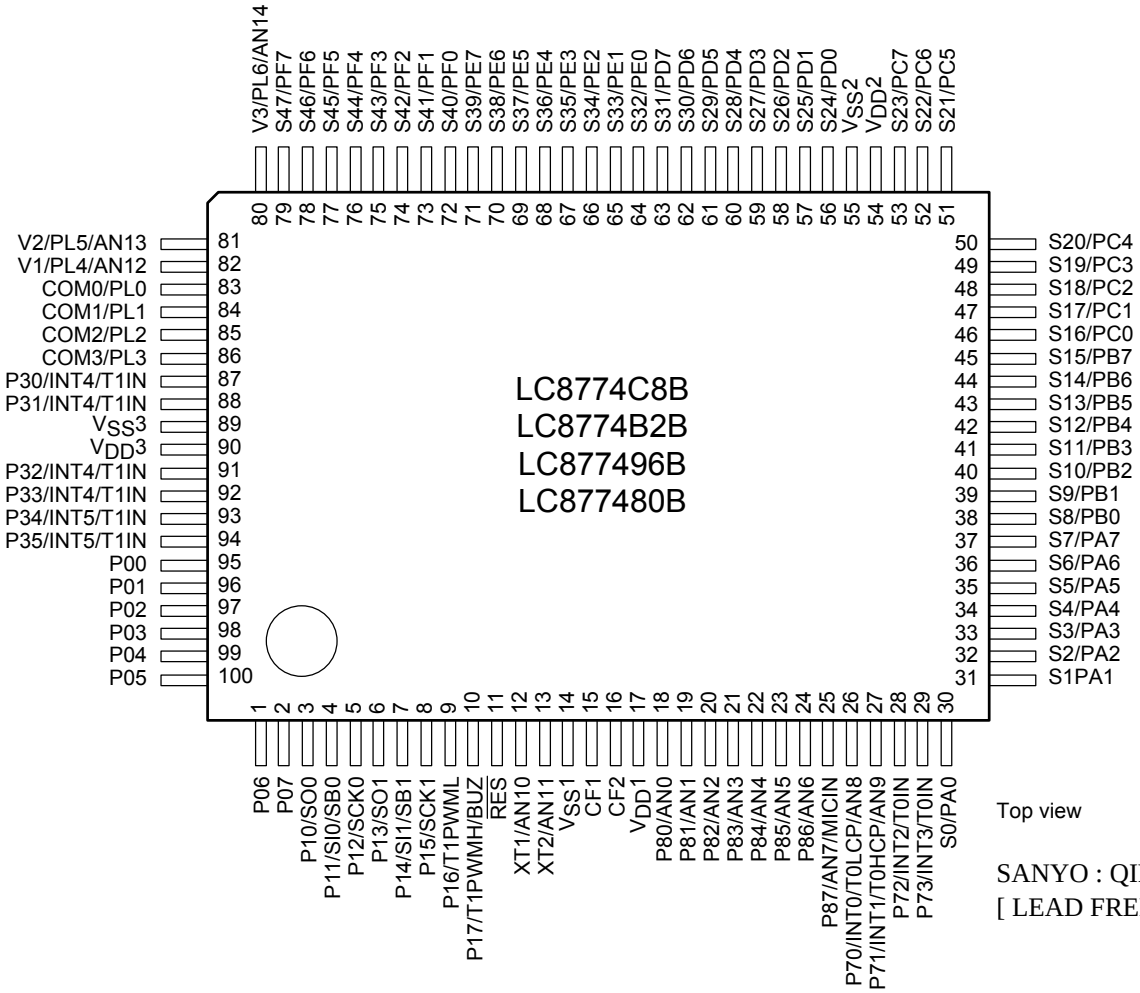
  HOLD mode is used to reduce power consumption. Program execution and peripheral circuits are stopped.
  1) CF, RC and crystal oscillation circuits stop automatically.
  2) Released by any of the following conditions.
     (1) Low level input to the reset pin
     (2) Specified level input to one of INT0, INT1, INT2, INT4, INT5
     (3) Port 0 interrupt
- X'tal HOLD mode

  X'tal HOLD mode is used to reduce power consumption. Program execution is stopped.
  All peripheral circuits except the base timer are stopped.
  1) CF and RC oscillation circuits stop automatically.
  2) Crystal oscillator operation is kept in its state at HOLD mode inception.
  3) Released by any of the following conditions.
     (1) Low level input to the reset pin
     (2) Specified level input to one of INT0, INT1, INT2, INT4, INT5
     (3) Port 0 interrupt
     (4) Base-timer interrupt

(20) Package
- QIP100E [LEAD FREE PRODUCT]
- TQFP100 [LEAD FREE PRODUCT]

(21) Development tools
- Evaluation chip: LC876093
- Emulator: EVA62S + ECB876600 (Evaluation chip board) + SUB877400 + POD100QFP or POD100SQFP (Type B)
  : ICE-B877300 + SUB877400 + POD100QFP or POD100SQFP (Type B)
- Flash ROM version: LC87F74C8A

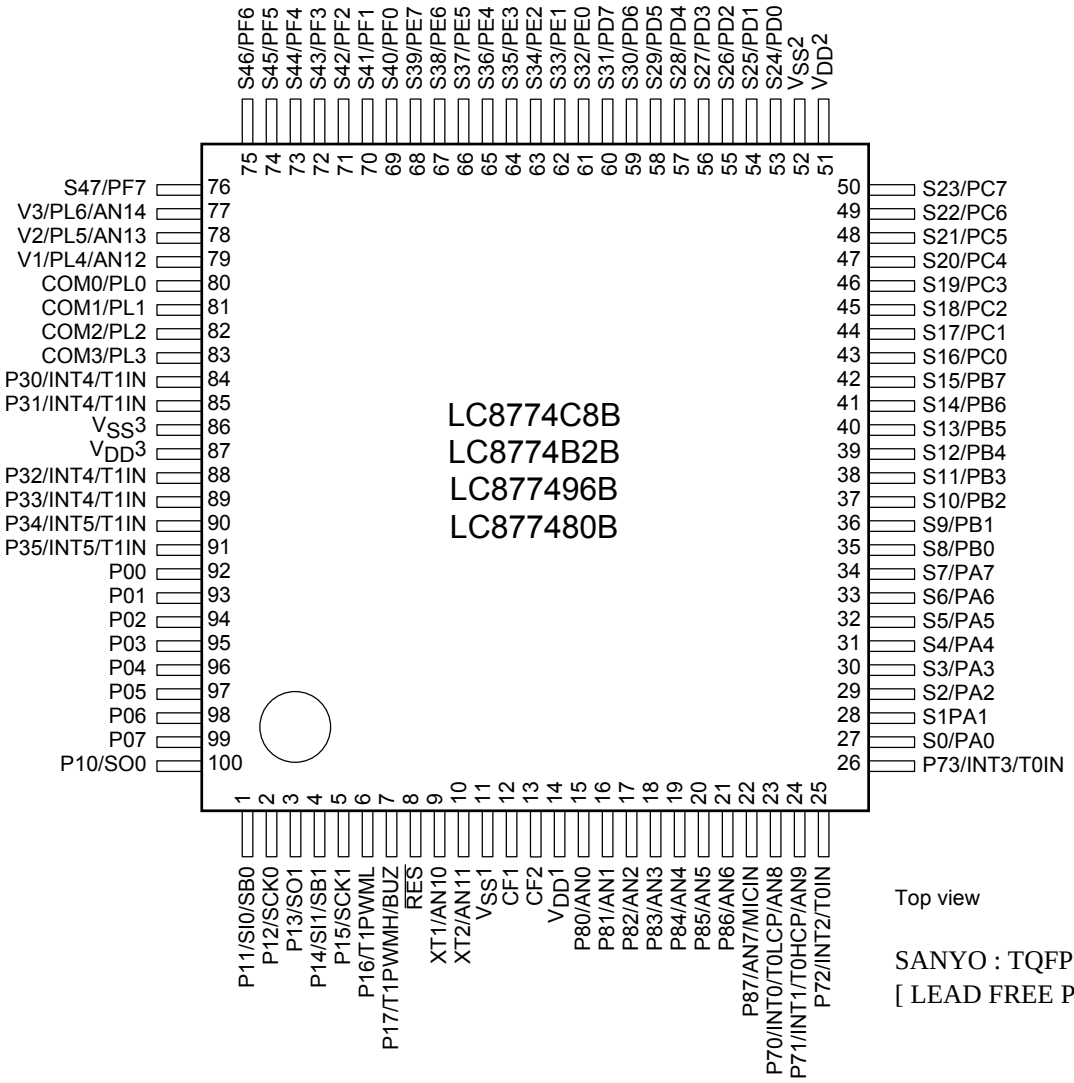
Pin Assignment



Top view

SANYO : QIP100E
[LEAD FREE PRODUCT]

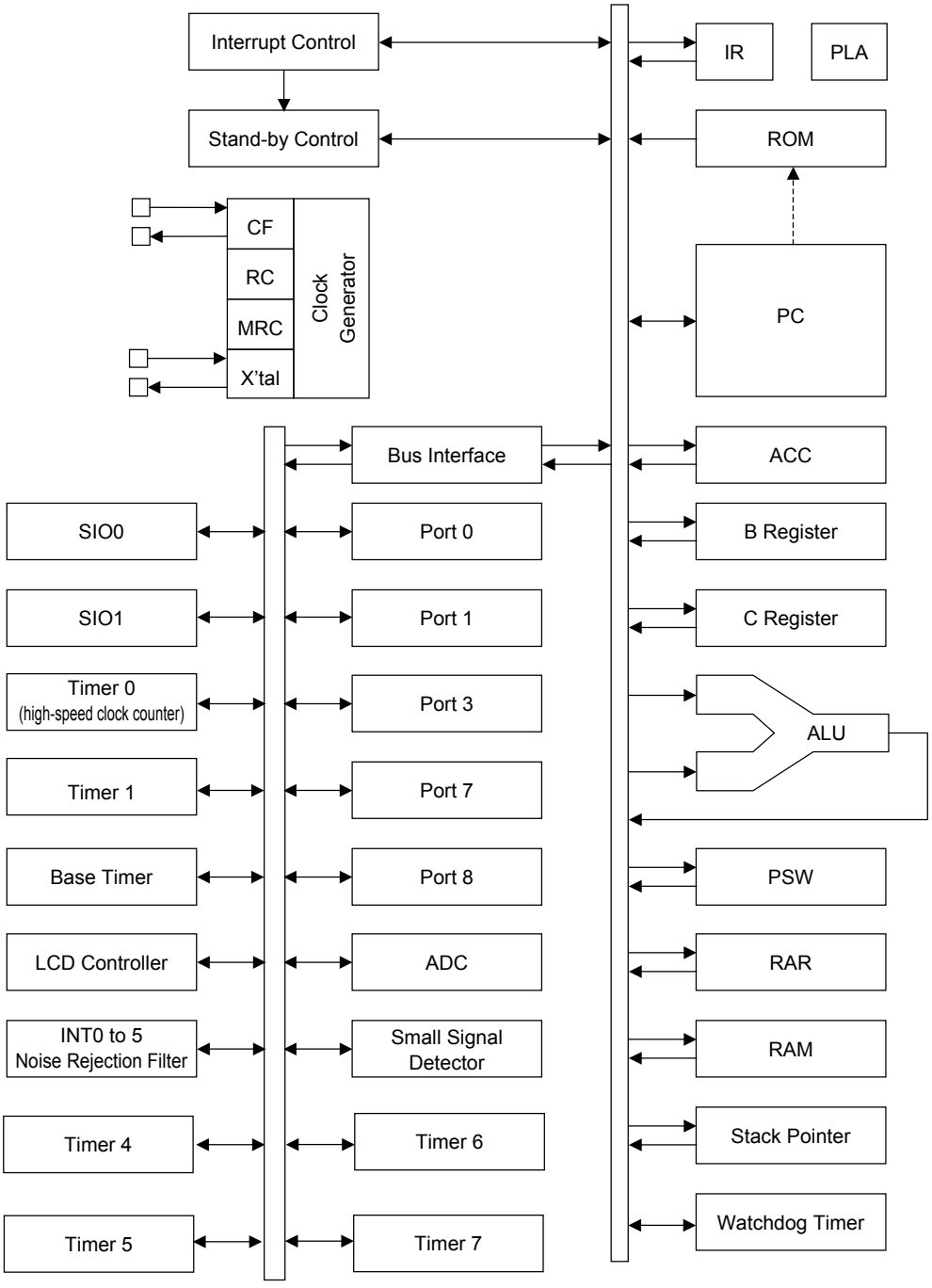
Pin Assignment



Top view

SANYO : TQFP100
[LEAD FREE PRODUCT]

System Block Diagram



Pin Description

<table>
<tr><th>Pin name</th><th>I/O</th><th>Function</th><th>Option</th></tr>
<tr><td>$V_{SS}1$,
$V_{SS}2$,
$V_{SS}3$</td><td>-</td><td>• Power supply (-)</td><td>No</td></tr>
<tr><td>$V_{DD}1$,
$V_{DD}2$,
$V_{DD}3$</td><td>-</td><td>• Power supply (+)</td><td>No</td></tr>
<tr><td>PORT 0
P00 to P07</td><td>I/O</td><td>• 8 bit input / output port
• Data direction programmable in nibble units
• Use of pull-up resistor can be specified in nibble units
• Input for HOLD release
• Input for port 0 interrupt</td><td>Yes</td></tr>
<tr><td>PORT 1
P10 to P17</td><td>I/O</td><td>• 8 bit input / output port
• Data direction programmable for each bit
• Use of pull-up resistor can be specified for each bit individually
• Other pin functions
P10: SIO0 data output
P11: SIO0 data input or bus input / output
P12: SIO0 clock input / output
P13: SIO1 data output
P14: SIO1 data input or bus input / output
P15: SIO1 clock input / output
P16: Timer 1 PWML output
P17: Timer 1 PWMH output / Buzzer output</td><td>Yes</td></tr>
<tr><td>PORT 3
P30 to P35</td><td>I/O</td><td>• 6 bit input / output port
• Data direction can be specified for each bit
• Use of pull-up resistor can be specified for each bit individually
• Other functions
P30 to P33: INT4 input / HOLD release input / Timer 1 event input /
Timer 0L capture input / Timer 0H capture input
P34 to P35: INT5 input / HOLD release input / Timer 1 event input /
Timer 0L capture input / Timer 0H capture input
• Interrupt detection selection
<table>
<tr><th></th><th>Rising</th><th>Falling</th><th>Rising and falling</th><th>H level</th><th>L level</th></tr>
<tr><td>INT4</td><td>Yes</td><td>Yes</td><td>Yes</td><td>No</td><td>No</td></tr>
<tr><td>INT5</td><td>Yes</td><td>Yes</td><td>Yes</td><td>No</td><td>No</td></tr>
</table></td><td>Yes</td></tr>
<tr><td>PORT 7
P70 to P73</td><td>I/O</td><td>• 4 bit input / output port
• Data direction can be specified for each bit
• Use of pull-up resistor can be specified for each bit individually
• Other functions
P70: INT0 input / HOLD release input / Timer 0L capture input / output for watchdog timer
P71: INT1 input / HOLD release input / Timer 0H capture input
P72: INT2 input / HOLD release input / Timer 0 event input / Timer 0L capture input
P73: INT3 input (noise rejection filter attached) / Timer 0 event input / Timer 0H capture input
AD input port: AN8 (P70), AN9 (P71)
• Interrupt detection selection
<table>
<tr><th></th><th>Rising</th><th>Falling</th><th>Rising and falling</th><th>H level</th><th>L level</th></tr>
<tr><td>INT0</td><td>Yes</td><td>Yes</td><td>No</td><td>Yes</td><td>Yes</td></tr>
<tr><td>INT1</td><td>Yes</td><td>Yes</td><td>No</td><td>Yes</td><td>Yes</td></tr>
<tr><td>INT2</td><td>Yes</td><td>Yes</td><td>Yes</td><td>No</td><td>No</td></tr>
<tr><td>INT3</td><td>Yes</td><td>Yes</td><td>Yes</td><td>No</td><td>No</td></tr>
</table></td><td>No</td></tr>
<tr><td>PORT 8
P80 to P87</td><td>I/O</td><td>• 8 bit input / output port
• Input / output can be specified for each bit individually
• Other functions:
AD input ports: AN0 to AN7
Small signal detector input port: MICIN (P87)</td><td>No</td></tr>
</table>

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Pin name	I/O	Function	Option
S0 / PA0 to S7 / PA7	I/O	• Segment output for LCD • Can be used as general purpose input / output port (PA)	No
S8 / PB0 to S15 / PB7	I/O	• Segment output for LCD • Can be used as general purpose input / output port (PB)	No
S16 / PC0 to S23 / PC7	I/O	• Segment output for LCD • Can be used as general purpose input / output port (PC)	No
S24 / PD0 to S31 / PD7	I/O	• Segment output for LCD • Can be used as general purpose input / output port (PD)	No
S32 / PE0 to S39 / PE7	I/O	• Segment output for LCD • Can be used as general purpose input / output port (PE)	No
S40 / PF0 to S47 / PF7	I/O	• Segment output for LCD • Can be used as general purpose input / output port (PF)	No
COM0 / PL0 to COM3 / PL3	I/O	• Common output for LCD • Can be used as general purpose input port (PL)	No
V1 / PL4 to V3 / PL6	I/O	• LCD output bias power supply • Can be used as general purpose input port (PL) • Other functions: AD input ports: AN12 to AN14	No
$\overline{RES}$	I	Reset terminal	No
XT1	I	• Input for 32.768kHz crystal oscillation • Other functions: General purpose input port AD input port: AN10 • When not in use, connect to $V_{DD}1$	No
XT2	I/O	• Output for 32.768kHz crystal oscillation • Other functions: General purpose input port AD input port: AN11 • When not in use, set to oscillation mode and leave open	No
CF1	I	Input terminal for ceramic oscillator	No
CF2	O	Output terminal for ceramic oscillator	No

Port Configuration

Port form and pull-up resistor options are shown in the following table.

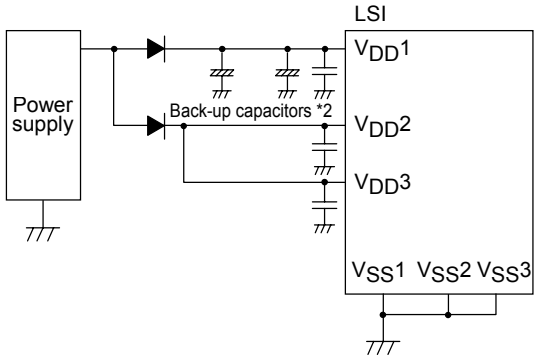
Port status can be read even when port is set to output mode.

Terminal	Option applies to:	Options	Output form	Pull-up resistor
P00 to P07	each bit	1	CMOS	Programmable (Note 1)
		2	Nch-open drain	None
P10 to P17	each bit	1	CMOS	Programmable
		2	Nch-open drain	Programmable
P30 to P35	each bit	1	CMOS	Programmable
		2	Nch-open drain	None
P70	-	None	Nch-open drain	Programmable
P71 to P73	-	None	CMOS	Programmable
P80 to P87	-	None	Nch-open drain	None
S0 / PA0 to S47 / PF7	-	None	CMOS	Programmable
COM0 / PL0 to COM3 / PL3	-	None	Input only	None
V1 / PL4 to V3 / PL6	-	None	Input only	None
XT1	-	None	Input only	None
XT2	-	None	Output for 32.768kHz crystal oscillation	None

Note 1 Attachment of Port 0 programmable pull-up resistors is controllable in nibble units (P00 to 03, P04 to 07).

*Note 1: Connect as follows to reduce noise on V_{DD}.
$V_{SS}1$, $V_{SS}2$ and $V_{SS}3$ must be connected together and grounded.

*Note 2: The power supply for the internal memory is $V_{DD}1$ but it uses the $V_{DD}3$ as the power supply for ports.
When the $V_{DD}3$ is not backed up, the port level does not become "H" even if the port latch is in the "H" level. Therefore, when the $V_{DD}3$ is not backed up and the port latch is "H" level, the port level is unstable in the HOLD mode, and the back up time becomes shorter because the through current runs from V_{DD} to GND in the input buffer.
If $V_{DD}3$ is not backed up, output "L" by the program or pull the port to "L" by the external circuit in the HOLD mode so that the port level becomes "L" level and unnecessary current consumption is prevented.



Absolute Maximum Ratings / Ta=25°C, $V_{SS}1=V_{SS}2=V_{SS}3=0V$

Parameter	Symbol	Pins	Conditions	V_{DD} [V]	min	typ	max	unit
Supply voltage	V_{DD} max	$V_{DD}1$, $V_{DD}2$, $V_{DD}3$	$V_{DD}1=V_{DD}2=V_{DD}3$		-0.3		+7.0	V
Supply voltage for LCD	VLCD	V1 / PL4, V2 / PL5, V3 / PL6	$V_{DD}1=V_{DD}2=V_{DD}3$		-0.3		V_{DD}	
Input voltage	V_I	Port L XT1, XT2, CF1, $\overline{RES}$			-0.3		V_{DD} +0.3	
Input / Output voltage	$V_{IO}1$	•Port 0, 1, 3, 7, 8 •Port A, B, C, D, E, F			-0.3		V_{DD} +0.3	
[High level output current]								
Peak output current	IOPH1	Port 0, 1, 3	•CMOS output selected •Current at each pin		-10			mA
	IOPH2	Port 71, 72, 73	Current at each pin		-3			
	IOPH3	Port A, B, C, D, E, F	Current at each pin		-5			
Total output current	∑IOAH1	Port 0, 1, 32, 33, 34, 35	Total of all pins		-40			
	∑IOAH2	Port 30, 31	Total of all pins		-10			
	∑IOAH3	Port 7	Total of all pins		-5			
	∑IOAH4	Port A, B, C	Total of all pins		-25			
	∑IOAH5	Port D, E, F	Total of all pins		-25			
[Low level output current]								
Peak output current	IOPL1	Port 0, 1, 32 to 35	Current at each pin				20	mA
	IOPL2	Port 30, 31	Current at each pin				30	
	IOPL3	Port 7, 8	Current at each pin				5	
	IOPL4	Port A, B, C, D, E, F	Current at each pin				15	
Total output current	∑IOAL1	Port 0, 1, 32, 33, 34, 35	Total of all pins				60	
	∑IOAL2	Port 30, 31	Total of all pins				60	
	∑IOAL3	Port 7, 8	Total of all pins				20	
	∑IOAL4	Port A, B, C	Total of all pins				40	
	∑IOAL5	Port D, E, F	Total of all pins				40	
Maximum power consumption	Pd max	QIP100E	Ta = -30 to +70°C				517	mW
		TQFP100					388	
Operating temperature range	Topr				-30		+70	°C
Storage temperature range	Tstg				-55		+125	

Recommended Operating Range / Ta=-30°C to +70°C, $V_{SS}1=V_{SS}2=V_{SS}3=0V$

Parameter	Symbol	Pins	Conditions	V_{DD} [V]	min	typ	max	unit
Operating supply voltage range	$V_{DD}1$	$V_{DD}1=V_{DD}2=V_{DD}3$	0.294µs ≤ tCYC ≤ 200µs		4.5		6.0	V
	$V_{DD}2$		0.735µs ≤ tCYC ≤ 200µs		2.5		6.0	
Supply voltage range in Hold mode	VHD	$V_{DD}1$	Keep RAM and register data in HOLD mode		2.0		6.0	
Input high voltage	$V_{IH}1$	•Port 0, 3, 8 •Port A, B, C, D, E, F, L	Output disable	2.5 to 6.0	$0.3V_{DD}+0.7$		V_{DD}	
	$V_{IH}2$	•Port 1 •Port 71, 72, 73 •P70 port input / interrupt	Output disable	2.5 to 6.0	$0.3V_{DD}+0.7$		V_{DD}	
	$V_{IH}3$	Port 87 small signal input	Output disable	2.5 to 6.0	$0.75V_{DD}$		V_{DD}	
	$V_{IH}4$	Port 70 Watchdog timer	Output disable	2.5 to 6.0	$0.9V_{DD}$		V_{DD}	
	$V_{IH}5$	XT1, XT2, CF1, $\overline{RES}$		2.5 to 6.0	$0.75V_{DD}$		V_{DD}	
Input low voltage	$V_{IL}1$	•Port 0, 3, 8 •Port A, B, C, D, E, F, L	Output disable	2.5 to 6.0	V_{SS}		$0.15V_{DD}+0.4$	
	$V_{IL}2$	•Port 1 •Port 71, 72, 73 •P70 port input / interrupt	Output disable	2.5 to 6.0	V_{SS}		$0.1V_{DD}+0.4$	
	$V_{IL}3$	Port 87 small signal input	Output disable	2.5 to 6.0	V_{SS}		$0.25V_{DD}$	
	$V_{IL}4$	Port 70 Watchdog timer	Output disable	2.5 to 6.0	V_{SS}		$0.8V_{DD}-1.0$	
	$V_{IL}5$	XT1, XT2, CF1, $\overline{RES}$		2.5 to 6.0	V_{SS}		$0.25V_{DD}$	
Operation cycle time	tCYC			4.5 to 6.0	0.294		200	µs
				2.5 to 6.0	0.735		200	
External system clock frequency	FEXCF1	CF1	•CF2 open •system clock divider : 1/1 •external clock DUTY = 50±5%	4.5 to 6.0	0.1		10	MHz
				2.5 to 6.0	0.1		4	
			•CF2 open •system clock divider : 1/2	4.5 to 6.0	0.2		20	
				2.5 to 6.0	0.2		8	
Oscillation frequency range (Note 1)	FmCF1	CF1, CF2	10MHz ceramic resonator oscillation Refer to figure 1	4.5 to 6.0		10		
	FmCF2	CF1, CF2	4MHz ceramic resonator oscillation Refer to figure 1	2.5 to 6.0		4		
	FmRC		RC oscillation	2.5 to 6.0	0.3	1.0	2.0	
	FmMRC		Frequency variable RC oscillation source oscillation	2.5 to 6.0		50		
	FsX'tal	XT1, XT2	32.768kHz crystal resonator oscillation Refer to figure 2	2.5 to 6.0		32.768		kHz

(Note 1) The port value of oscillation circuit is shown in table 1 and table 2.

Electrical Characteristics / Ta=-30°C to +70°C, $V_{SS}1=V_{SS}2=V_{SS}3=0V$

Parameter	Symbol	Pins	Conditions	V_{DD} [V]	min	typ	max	unit
High level input current	$I_{IH}1$	•Port 0, 1, 3, 7, 8 •Port A, B, C, D, E, F, L	•Output disabled •Pull-up resister OFF •$V_{IN}=V_{DD}$ (including OFF state leak current of the output Tr.)	2.5 to 6.0			1	μA
	$I_{IH}2$	$\overline{RES}$	$V_{IN}=V_{DD}$	2.5 to 6.0			1	
	$I_{IH}3$	XT1, XT2	When configured as an input port $V_{IN}=V_{DD}$	2.5 to 6.0			1	
	$I_{IH}4$	CF1	$V_{IN}=V_{DD}$	2.5 to 6.0			15	
	$I_{IH}5$	P87 / AN7 / MICIN small signal input	V_{IN}=VBIS + 0.5V (VBIS : Bias voltage)	2.5 to 6.0	4.2	8.5	15	
Low level input current	$I_{IL}1$	•Port 0, 1, 3, 7, 8 •Port A, B, C, D, E, F, L	•Output disabled •Pull-up resister OFF •$V_{IN}=V_{SS}$ (including OFF state leak current of the output Tr.)	2.5 to 6.0	-1			
	$I_{IL}2$	$\overline{RES}$	$V_{IN}=V_{SS}$	2.5 to 6.0	-1			
	$I_{IL}3$	XT1, XT2	When configured as an input port $V_{IN}=V_{SS}$	2.5 to 6.0	-1			
	$I_{IL}4$	CF1	$V_{IN}=V_{SS}$	2.5 to 6.0	-15			
	$I_{IL}5$	P87 / AN7 / MICIN small signal input	V_{IN}=VBIS - 0.5V (VBIS : Bias voltage)	2.5 to 6.0	-15	-8.5	-4.2	
High level output voltage	$V_{OH}1$	Port 0, 1, 3 : CMOS output option	I_{OH}=-1.0mA	4.5 to 6.0	V_{DD}-1			V
	$V_{OH}2$		I_{OH}=-0.1mA	2.5 to 6.0	V_{DD}-0.5			
	$V_{OH}3$	Port 7	I_{OH}=-0.4mA	2.5 to 6.0	V_{DD}-1			
	$V_{OH}4$	Port A, B, C, D, E, F	I_{OH}=-1.0mA	4.5 to 6.0	V_{DD}-1			
	$V_{OH}5$		I_{OH}=-0.1mA	2.5 to 6.0	V_{DD}-0.5			
Low level output voltage	$V_{OL}1$	Port 0, 1, 3	I_{OL}=10mA	4.5 to 6.0			1.5	
	$V_{OL}2$		I_{OL}=1.6mA	2.5 to 6.0			0.4	
	$V_{OL}3$	Port 30, 31	I_{OL}=30mA	4.5 to 6.0			1.5	
	$V_{OL}4$	Port 7, 8	I_{OL}=1mA	4.5 to 6.0			0.4	
	$V_{OL}5$		I_{OL}=0.5mA	2.5 to 6.0			0.4	
	$V_{OL}6$	Port A, B, C, D, E, F	I_{OL}=8mA	4.5 to 6.0			1.5	
	$V_{OL}7$		I_{OL}=1.4mA	2.5 to 6.0			0.4	
LCD output voltage regulation	VODLS	S0 to S47	I_O=0mA VLCD, 2/3VLCD, 1/3VLCD level output Refer to figure 8	2.5 to 6.0	0		±0.2	
	VODLC	COM0 to COM3	I_O=0mA VLCD, 2/3VLCD, 1/2VLCD, 1/3VLCD level output Refer to figure 8	2.5 to 6.0	0		±0.2	
LCD bias resistor	RLCD1	Resistance per one bias resistor	Refer to figure 8	2.5 to 6.0		60		kΩ
	RLCD2	•Resistance per one bias resistor •1/2R mode	Refer to figure 8	2.5 to 6.0		30		
Resistance of pull-up MOS Tr.	Rpu	•Port 0, 1, 3, 7 •Port A, B, C, D, E, F	$V_{OH}=0.9V_{DD}$	4.5 to 6.0	15	40	70	
				2.5 to 4.5	25	70	150	
Hysterisis voltage	VHIS1	•Port 1, 7 • $\overline{RES}$		2.5 to 6.0		$0.1V_{DD}$		V
	VHIS2	Port 87 small signal input		2.5 to 6.0		$0.1V_{DD}$		

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Parameter	Symbol	Pins	Conditions	V_{DD} [V]	min	typ	max	unit
Pin capacitance	CP	All pins	•All other terminals connected to V_{SS}. •f=1MHz •Ta=25°C	2.5 to 6.0		10		pF
Input sensitivity	Vsen	Port 87 small signal input		2.5 to 6.0	0.12V_{DD}			Vp-p

Serial Input / Output Characteristics / Ta=-30°C to +70°C, $V_{SS}1=V_{SS}2=V_{SS}3=0V$

Parameter	Symbol	Pins	Conditions	V_{DD} [V]	min	typ	max	unit
[Serial clock]								
[Input clock]								
Cycle time	tSCK1	SCK0(P12)	Refer to figure 6	2.5 to 6.0	4/3			tCYC
Low level pulse width	tSCKL1				2/3			
	tSCKLA1				2/3			
High level pulse width	tSCKH1				2/3			
	tSCKHA1				5			
Cycle time	tSCK2	SCK1(P15)	Refer to figure 6	2.5 to 6.0	2			
Low level pulse width	tSCKL2				1			
High level pulse width	tSCKH2				1			
[Output clock]								
Cycle time	tSCK3	SCK0(P12)	•CMOS output •Refer to figure 6	2.5 to 6.0	4/3			tCYC
Low level pulse width	tSCKL3					1/2		tSCK
	tSCKLA2					3/4		
High level pulse width	tSCKH3					1/2		
	tSCKHA2					2		
Cycle time	tSCK4	SCK1(P15)	•CMOS output •Refer to figure 6	2.5 to 6.0	2			tCYC
Low level pulse width	tSCKL4					1/2		tSCK
High level pulse width	tSCKH4					1/2		
[Serial input]								
Data set-up time	tsDI	SI0(P11), SI1(P14), SB0(P11), SB1(P14)	•Measured with respect to SIOCLK leading edge •Refer to figure 6	4.5 to 6.0	0.03			µs
				2.5 to 6.0	0.1			
Data hold time	thDI			4.5 to 6.0	0.03			
				2.5 to 6.0	0.1			
[Serial output]								
Output delay time	tdDO	SO0(P10), SO1(P13), SB0(P11), SB1(P14)	•When port is open drain: Time delay from SIOCLK trailing edge to the SO data change •Refer to figure 6	4.5 to 6.0			1/3tCYC +0.05	µs
				2.5 to 6.0			1/3tCYC +0.25	

Pulse Input Conditions / Ta=-30°C to +70°C, $V_{SS}1=V_{SS}2=V_{SS}3=0V$

Parameter	Symbol	Pins	Conditions	V_{DD} [V]	min	typ	max	unit
High / low level pulse width	tPIH1 tPIL1	INT0(P70), INT1(P71), INT2(P72), INT4(P30 to P33), INT5(P34 to P35)	•Condition that interrupt is accepted •Condition that event input to timer 0 or 1 is accepted	2.5 to 6.0	1			tCYC
	tPIH2 tPIL2	INT3(P73) (Noise rejection ratio is 1/1.)	•Condition that interrupt is accepted •Condition that event input to timer 0 is accepted	2.5 to 6.0	2			
	tPIH3 tPIL3	INT3(P73) (Noise rejection ratio is 1/32.)	•Condition that interrupt is accepted •Condition that event input to timer 0 is accepted	2.5 to 6.0	64			
	tPIH4 tPIL4	INT3(P73) (Noise rejection ratio is 1/128.)	•Condition that interrupt is accepted •Condition that event input to timer 0 is accepted	2.5 to 6.0	256			
	tPIH5 tPIL5	MICIN(P87)	•Condition that signal is accepted to small signal detection counter	2.5 to 6.0	1			
	tPIL6	$\overline{RES}$	•Condition that reset is accepted	2.5 to 6.0	200			µs

AD Converter Characteristics / Ta=-30°C to + 70°C, $V_{SS}1=V_{SS}2=V_{SS}3=0V$

Parameter	Symbol	Pins	Conditions	V_{DD} [V]	min	typ	max	unit
Resolution	N	AN0(P80) to AN7(P87), AN8(P70), AN9(P71), AN10(XT1), AN11(XT2), AN12(V1), AN13(V2), AN14(V3)		3.0 to 6.0		8		bit
Absolute precision	ET		(Note 2)	3.0 to 6.0			±1.5	LSB
Conversion time	TCAD		AD conversion time = 32 × tCYC (ADCR2=0) (Note 3)	4.0 to 6.0	15.62 (tCYC= 0.488µs)		97.92 (tCYC= 3.06µs)	µs
				3.0 to 6.0	23.52 (tCYC= 0.735µs)		97.92 (tCYC= 3.06µs)	
			AD conversion time = 64 × tCYC (ADCR2=1) (Note 3)	4.5 to 6.0	18.82 (tCYC= 0.294µs)		97.92 (tCYC= 1.53µs)	
				3.0 to 6.0	47.04 (tCYC= 0.735µs)		97.92 (tCYC= 1.53µs)	
Analog input voltage range	VAIN			3.0 to 6.0	V_{SS}		V_{DD}	V
Analog port input current	IAINH		VAIN=V_{DD}	3.0 to 6.0			1	µA
	IAINL		VAIN=V_{SS}	3.0 to 6.0	-1			

(Note 2) Absolute precision does not include quantizing error (±1/2 LSB).

(Note 3) Conversion time means time from executing AD conversion instruction to loading complete digital value to register.

Current Consumption Characteristics / Ta=-30°C to +70°C, $V_{SS}1=V_{SS}2=V_{SS}3=0V$

Parameter	Symbol	Pins	Conditions	V_{DD} [V]	min	typ	max	unit
Current consumption during normal operation (Note 4)	IDDOP1	$V_{DD}1=V_{DD}2=V_{DD}3$	•FmCF=10MHz Ceramic resonator oscillation •FsX'tal=32.768kHz crystal oscillation •System clock: CF 10MHz oscillation •Internal RC oscillation stopped •Frequency variable RC oscillation stopped •Divider : 1/1	4.5 to 6.0		10.8	30	mA
	IDDOP2		•CF1=20MHz external clock •FsX'tal=32.768kHz crystal oscillation •System clock: CF1 oscillation •Internal RC oscillation stopped •Frequency variable RC oscillation stopped •Divider : 1/2	4.5 to 6.0		11.5	31	
	IDDOP3		•FmCF=4MHz Ceramic resonator oscillation •FsX'tal=32.768kHz crystal oscillation •System clock: CF 4MHz oscillation •Internal RC oscillation stopped •Frequency variable RC oscillation stopped •Divider : 1/1	4.5 to 6.0		5.1	17	
	IDDOP4			2.5 to 4.5		2.6	11	
	IDDOP5		•FmCF=0Hz (No oscillation) •FsX'tal=32.768kHz crystal oscillation •Frequency variable RC oscillation stopped •System clock: RC oscillation •Divider : 1/2	4.5 to 6.0		0.95	10	
	IDDOP6			2.5 to 4.5		0.45	6	
	IDDOP7		•FmCF=0Hz (No oscillation) •FsX'tal=32.768kHz crystal oscillation •Internal RC oscillation stopped •System clock: 1MHz with frequency variable RC oscillation •Divider : 1/2	4.5 to 6.0		2.0	12	
	IDDOP8			2.5 to 4.5		1.6	8	

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Parameter	Symbol	Pins	Conditions	V_{DD} [V]	min	typ	max	unit
Current consumption during normal operation (Note 4)	IDDOP9	$V_{DD}1=V_{DD}2=V_{DD}3$	•FmCF=0Hz (No oscillation) •FsX'tal=32.768kHz crystal oscillation •System clock: 32.768kHz •Internal RC oscillation stopped •Frequency variable RC oscillation stopped •Divider : 1/2	4.5 to 6.0		42	140	μA
	IDDOP10			2.5 to 4.5		18	60	
Current consumption during HALT mode (Note 4)	IDDHALT1	$V_{DD}1=V_{DD}2=V_{DD}3$	HALT mode •FmCF=10MHz Ceramic resonator oscillation •FsX'tal=32.768kHz crystal oscillation •System clock: CF 10MHz oscillation •Internal RC oscillation stopped •Frequency variable RC oscillation stopped •Divider : 1/1	4.5 to 6.0		3.7	12	mA
	IDDHALT2		HALT mode •CF1=20MHz for external clock •FsX'tal=32.768kHz crystal oscillation •System clock: CF1 oscillation •Internal RC oscillation stopped •Frequency variable RC oscillation stopped •Divider : 1/2	4.5 to 6.0		4.1	13	
	IDDHALT3		HALT mode •FmCF=4MHz Ceramic resonator oscillation •FsX'tal=32.768kHz crystal oscillation •System clock: CF 4MHz oscillation •Internal RC oscillation stopped •Frequency variable RC oscillation stopped •Divider : 1/1	4.5 to 6.0		1.8	6	
	IDDHALT4			2.5 to 4.5		1.0	5	
	IDDHALT5		HALT mode •FmCF=0Hz (Oscillation stop) •FsX'tal=32.768kHz crystal oscillation •Internal RC oscillation stopped •Frequency variable RC oscillation stopped •Divider : 1/2	4.5 to 6.0		500	1600	μA
	IDDHALT6			2.5 to 4.5		250	1300	

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Parameter	Symbol	Pins	Conditions	V_{DD} [V]	min	typ	max	unit
Current consumption during HALT mode (Note 4)	IDDHALT7	$V_{DD}1=V_{DD}2=V_{DD}3$	HALT mode •FmCF=0Hz (No oscillation) •FsX'tal=32.768kHz crystal oscillation •Internal RC oscillation stopped •System clock: 1MHz with frequency variable RC oscillation •Divider : 1/2	4.5 to 6.0		1500	3600	μA
	IDDHALT8			2.5 to 4.5		1250	3300	
	IDDHALT9		HALT mode •FmCF=0Hz (Oscillation stop) •FsX'tal=32.768kHz crystal oscillation •System clock: 32.768kHz •Internal RC oscillation stopped • Frequency variable RC oscillation stopped •Divider : 1/2	4.5 to 6.0		25	100	
	IDDHALT10			2.5 to 4.5		12	60	
Current consumption during HOLD mode	IDDHOLD1	$V_{DD}1$	HOLD mode •CF1=V_{DD} or open (when using external clock)	4.5 to 6.0		0.05	25	μA
	IDDHOLD2			2.5 to 4.5		0.015	20	
Current consumption during Date / time clock HOLD mode	IDDHOLD3	$V_{DD}1$	Date / time clock HOLD mode •CF1=V_{DD} or open (when using external clock) •FmX'tal=32.768kHz crystal oscillation	4.5 to 6.0		20	90	
	IDDHOLD4			2.5 to 4.5		8	50	

(Note 4) The currents through the output transistors and the pull-up MOS transistors are ignored.

Main system clock oscillation circuit characteristics

The characteristics in the table bellow is based on the following conditions:

1. Use the standard evaluation board SANYO has provided.
2. Use the peripheral parts with indicated value externally.
3. The peripheral parts value is a recommended value of oscillator manufacturer.

Table 1. Main system clock oscillation circuit characteristics using ceramic resonator

Frequency	Manufacturer	Oscillator	Circuit parameters			Operating supply voltage range [V]	Oscillation stabilizing time		Notes
			C1 [pF]	C2 [pF]	Rd1 [Ω]		typ [mS]	max [mS]	
10MHz	Murata	CSTLS10M0G53-B0	(15)	(15)	220	4.5 to 6.0	0.05	0.25	Built-in C1, C2
		CSTCE10M0G52-R0	(10)	(10)	220	4.5 to 6.0	0.05	0.25	Built-in C1, C2
4MHz	Murata	CSTLS4M00G53-B0	(15)	(15)	470	2.5 to 6.0	0.05	0.25	Built-in C1, C2
		CSTCR4M00G53-R0	(15)	(15)	1k	2.5 to 6.0	0.06	0.3	Built-in C1, C2

The oscillation stabilizing time is a period until the oscillation becomes stable after V_{DD} becomes higher than minimum operating voltage. (Refer to Figure 4)

Subsystem clock oscillation circuit characteristics

The characteristics in the table bellow is based on the following conditions:

1. Use the standard evaluation board SANYO has provided.
2. Use the peripheral parts with indicated value externally.
3. The peripheral parts value is a recommended value of oscillator manufacturer.

Table 2. Subsystem clock oscillation circuit characteristics using crystal oscillator

Frequency	Manufacturer	Oscillator	Circuit parameters				Operating supply voltage range [V]	Oscillation stabilizing time		Notes
			C3 [pF]	C4 [pF]	Rf [Ω]	Rd2 [kΩ]		typ [S]	max [S]	
32.768kHz	SEIKO EPSON	MC-306	18	18	OPEN	390	2.5 to 6.0	1.1	3.0	Applicable CL value = 12.5pF

The oscillation stabilizing time is a period until the oscillation becomes stable after executing the instruction which starts the sub-clock oscillation or after releasing the HOLD mode. (Refer to Figure 4)

(Notes) • Since the circuit pattern affects the oscillation frequency, place the oscillation-related parts as close to the oscillation pins as possible with the shortest possible pattern length.

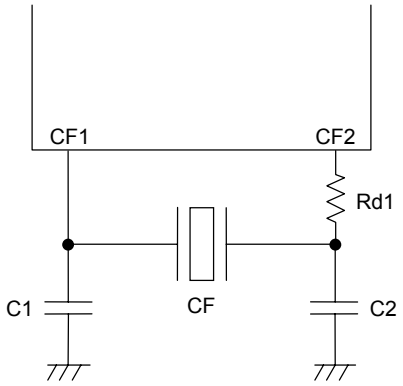


Figure 1 Ceramic oscillation circuit

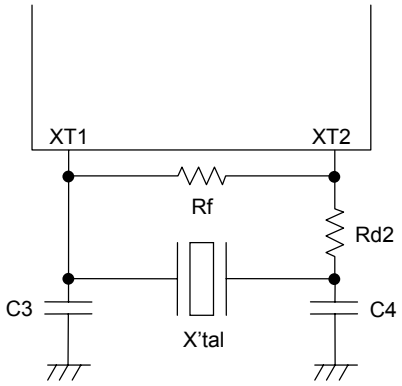


Figure 2 Crystal oscillation circuit

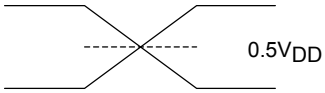
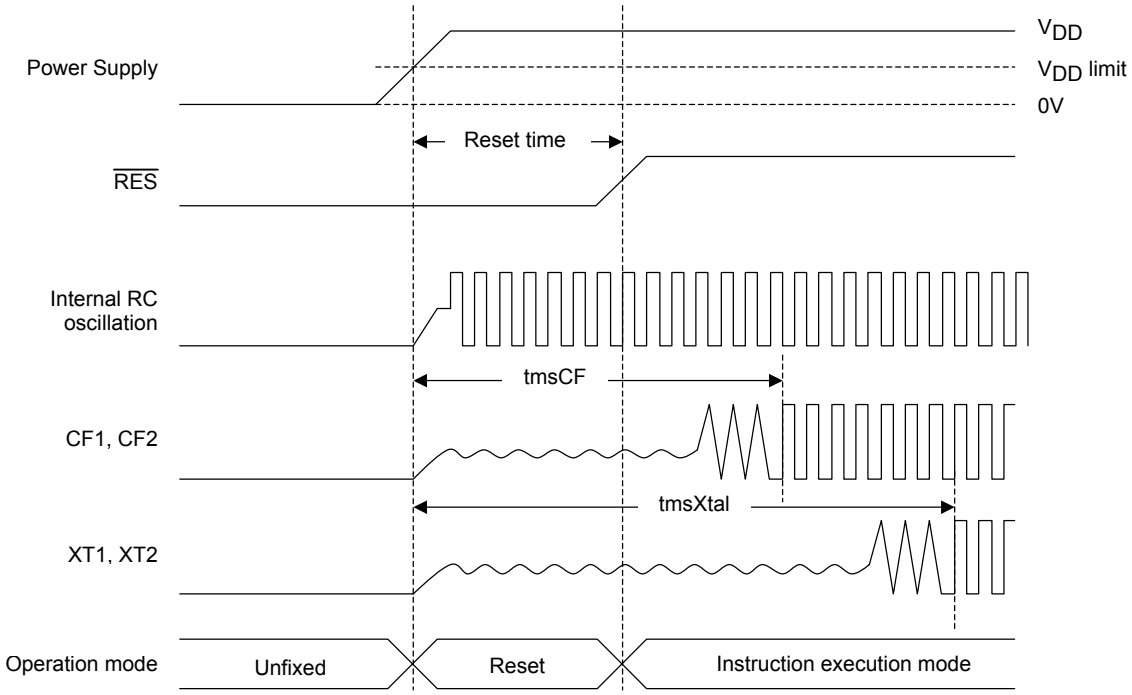
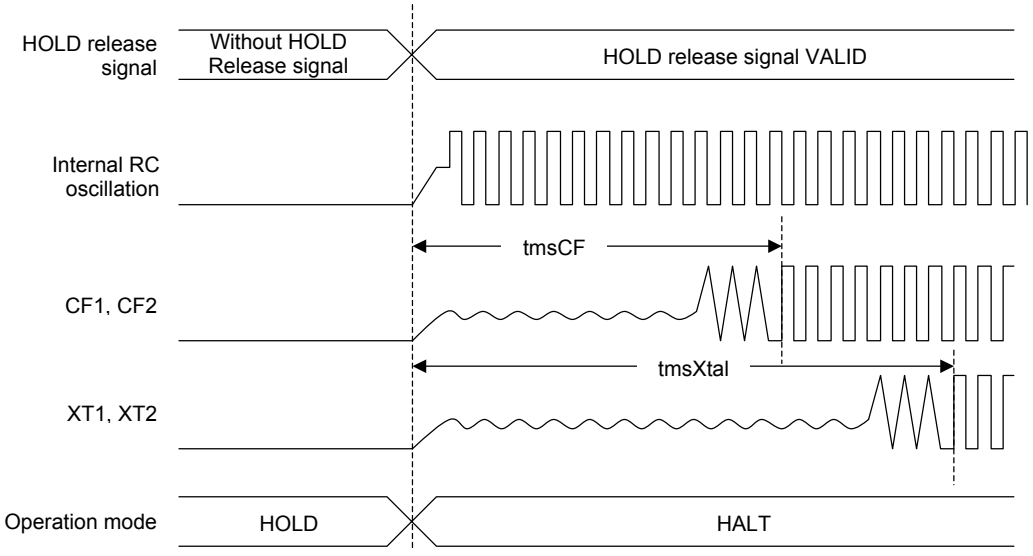


Figure 3 AC timing measurement point

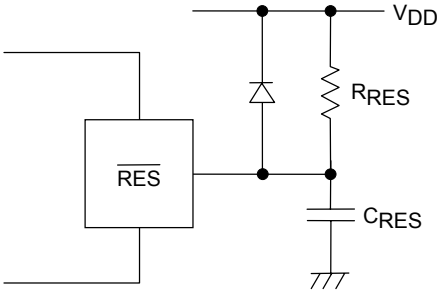


Reset time and oscillation stable time



HOLD release signal and oscillation stable time

Figure 4 Oscillation stabilizing time



(Note)
Select C_{RES} and R_{RES} value to assure that at least 200μs reset time is generated after the V_{DD} becomes higher than the minimum operating voltage.

Figure 5 Reset circuit

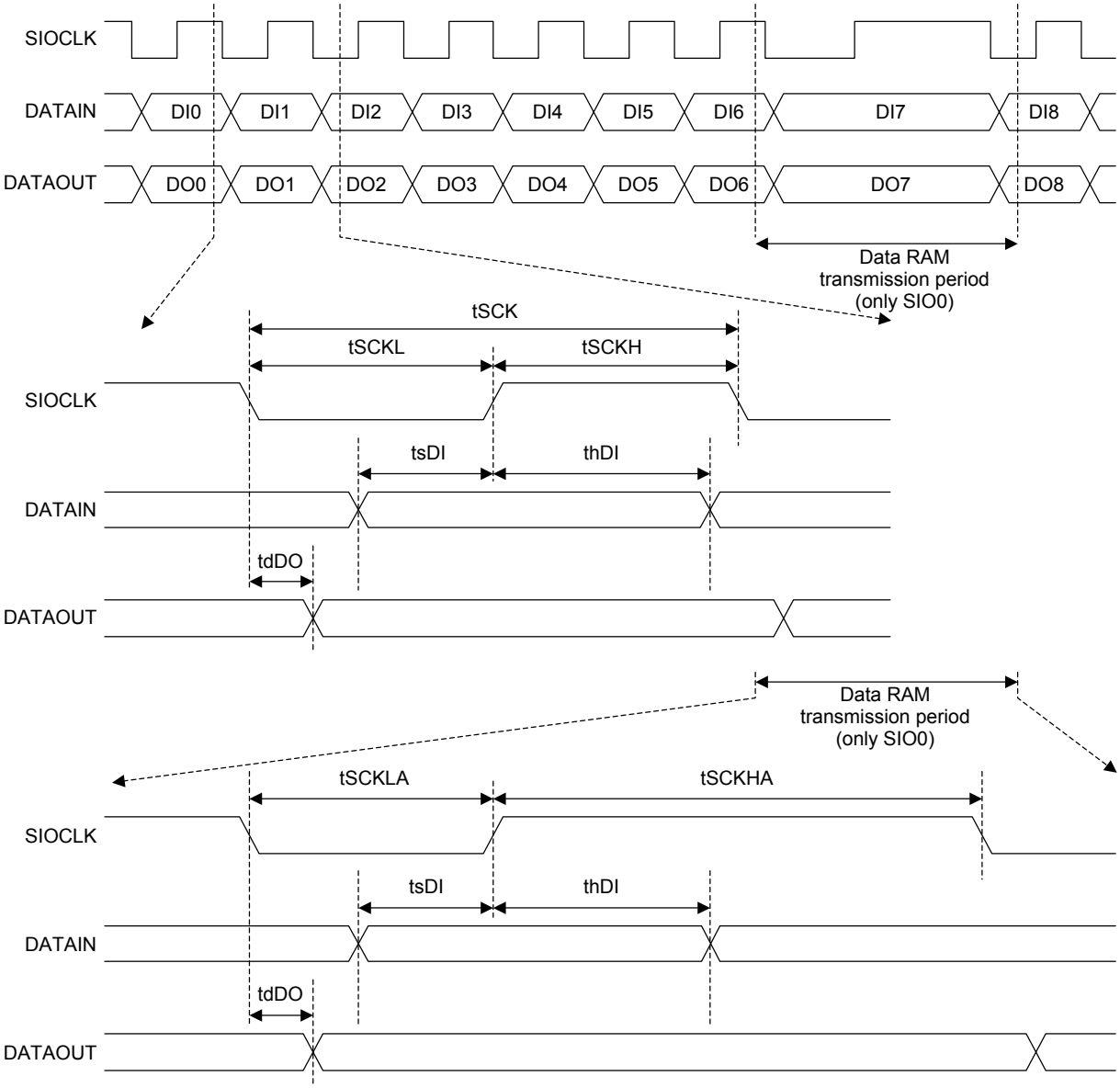


Figure 6 Serial input / output wave form

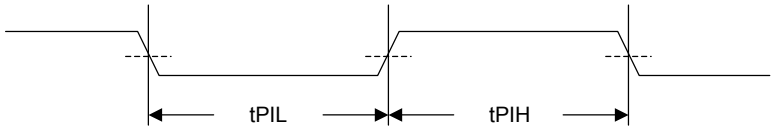


Figure 7 Pulse input timing

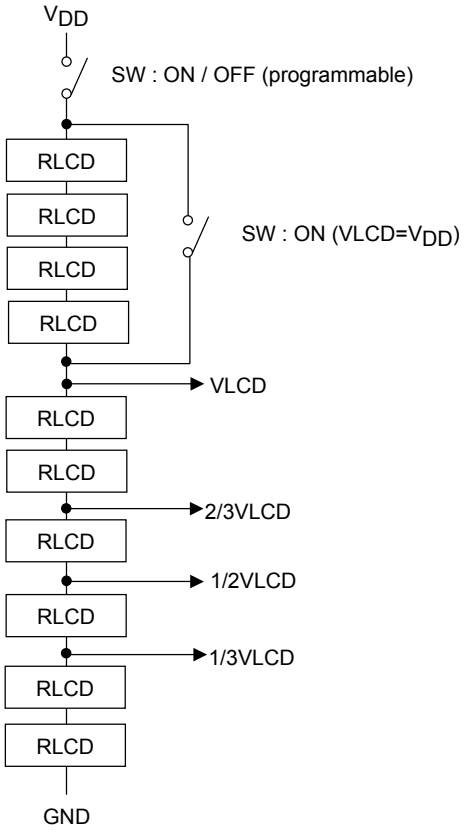


Figure 8 LCD bias resistor