M61250BFP

NTSC 1 chip TV signal processor

REJ03F0088-0100Z
Rev.1.0
Sep.23.2003

Description

The M61250BFP is a single-chip semiconductor integrated circuit that contains the signal processing for NTSC color television.

All of the signal processing circuits for video intermediate frequencies, vocal intermediate frequencies, video, color, and polarization, as well as I^2C bus control, are built in, and television sets ranging from popular-class to medium-grade sets are supported. Moreover, the M37150 8-bit microcomputer for the television and the interconnection pin are opposite each other, so that less space is required for mounting.

Features

- No VCO coil for VIF required
- Internal unregulated vocal demodulator
- PLL-SPLIT SIF system for FM radio
- Fsc output
- ACL or ABCL can be selected
- Internal horizontal oscillation probe
- Internal perpendicular sawtooth wave generator
- Internal self-diagnosis function
- Internal black peak hold, AFC2, killer filter
- H & V pulse output for OSD
- Internal reset circuit and clock output for microcomputer use
- Internal 5 V and 8 V regulators

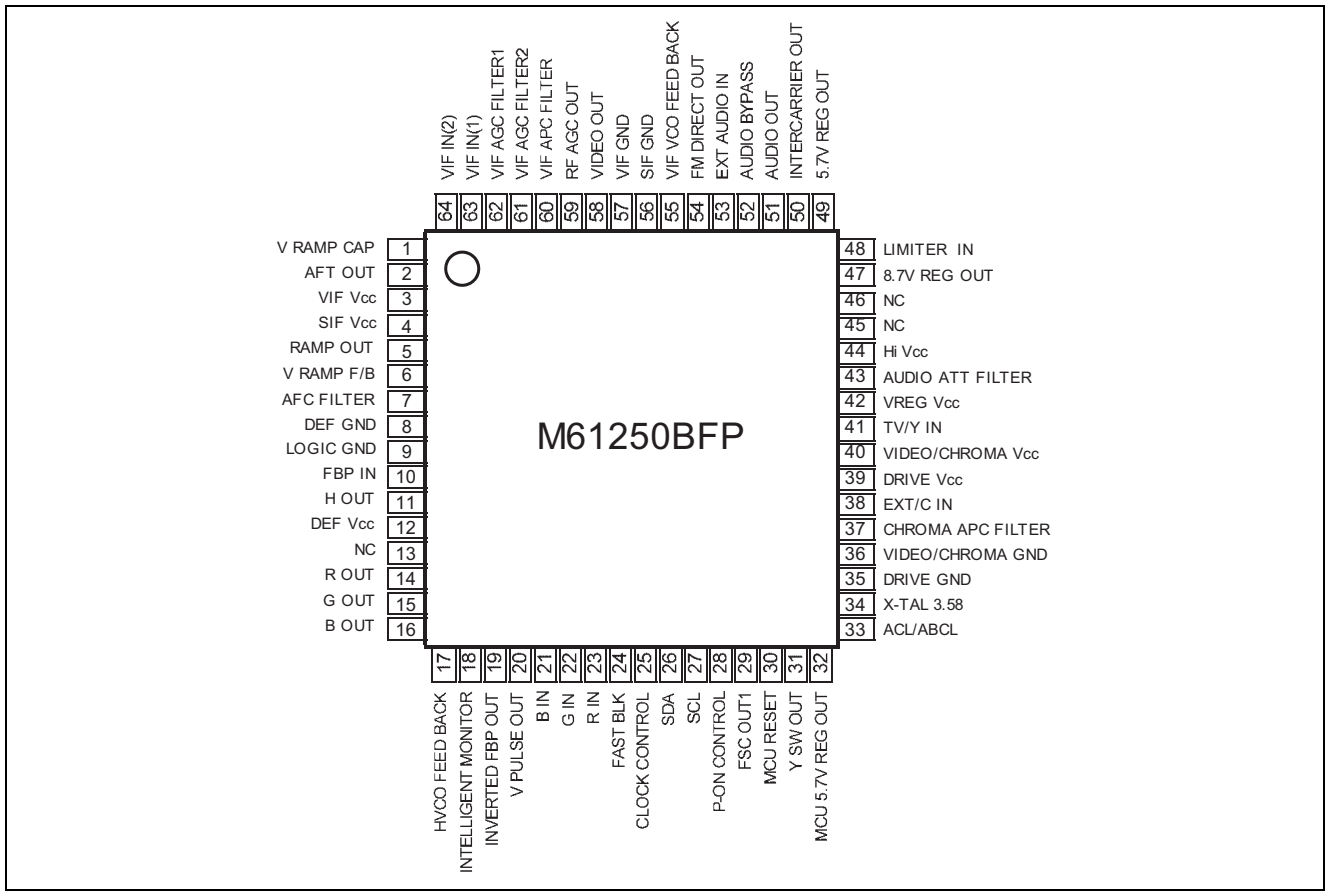
Applications

- NTSC color television receivers

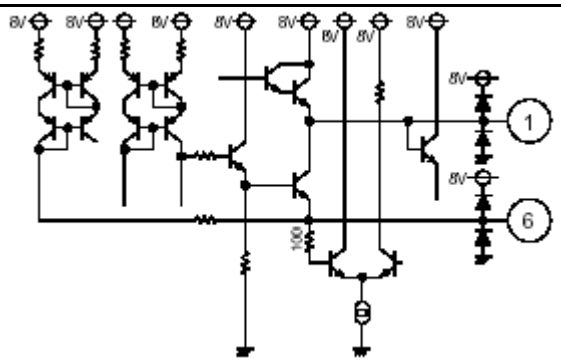
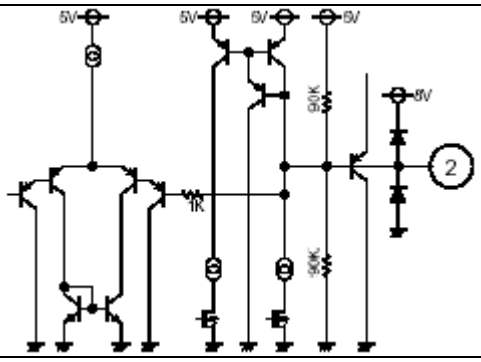
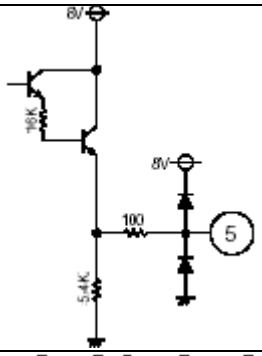
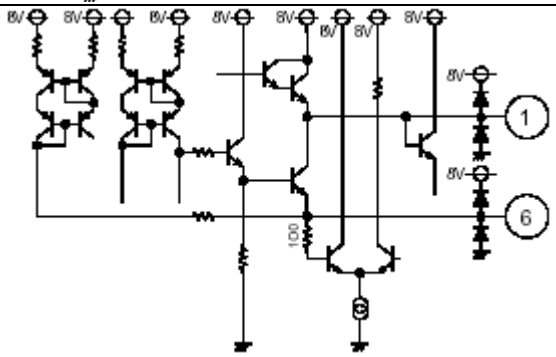
Recommended Operating Conditions

- Power supply voltage range:
  4.75 V to 5.25 (Pins 3, 4, 39, 40)
  7.6 V to 8.4 V (Pins 12, 44)
  8.3 V to 9.1 V (Pin 42)
- Recommended power supply voltage:
  5.0 V (Pins 3, 4, 39, 40)
  8.0 V (Pins 12, 44)
  8.7 V (Pin 42)

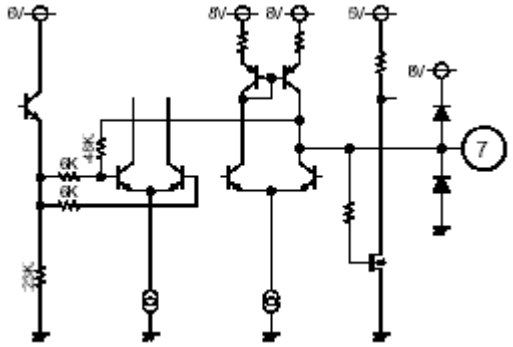
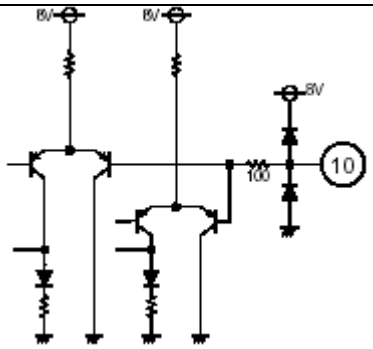
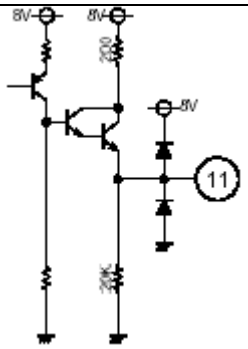
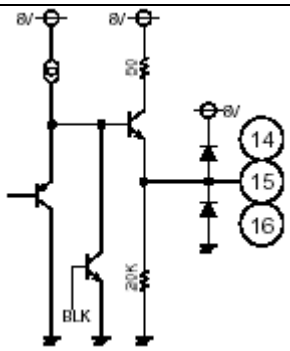
Pin Configuration (Top View)



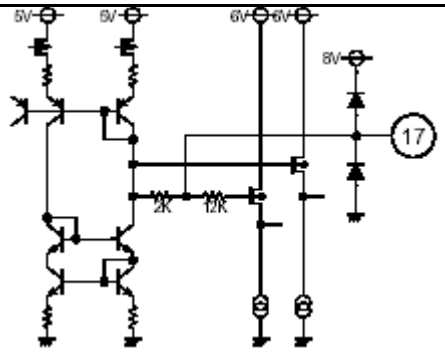
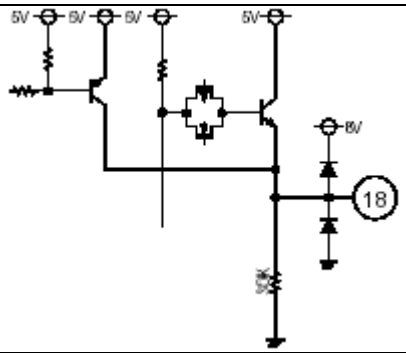
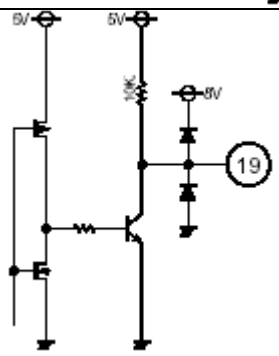
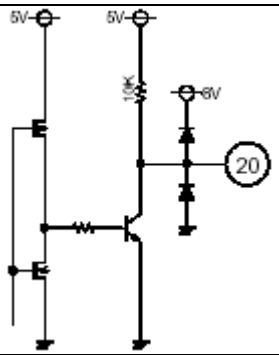
Pin Explanations

Pin No.	Name	Pin peripheral circuit	DC voltage (V)
1	V RAMP CAP		
2	AFT OUT		0.3 to 4.7
3	VIF V_{CC}		5.0 V
4	SIF V_{CC}		
5	RAMP OUT		4.6
6	V RAMP FEED BACK		

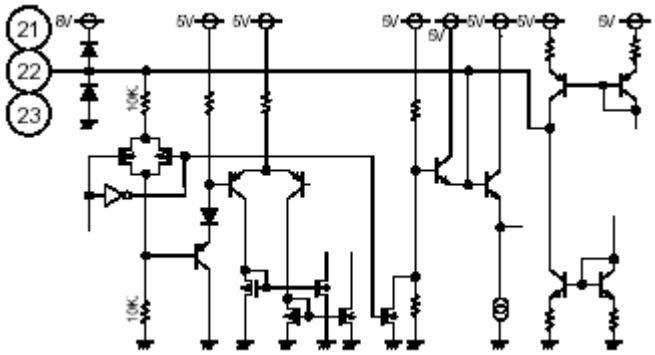
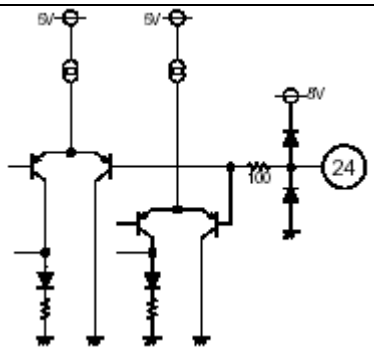
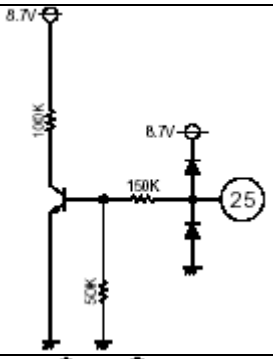
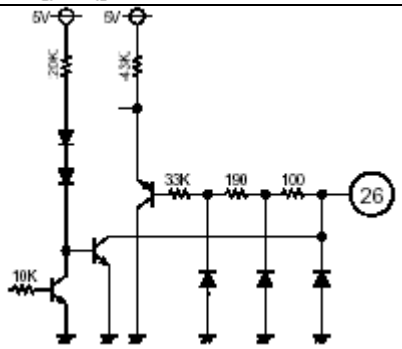
Pin Explanations (cont)

Pin No.	Name	Pin peripheral circuit	DC voltage (V)
7	AFC FILTER		3.5 V
8	DEF GND		
9	LOGIC GND		
10	FBP IN		V_{TH}: 2.0 V (FBP Vth L = OFF) V_{TH}: 1.0 V (FBP Vth L = ON)
11	H OUT		V_{OL}: 0.0 V V_{OH}: 5.4 V
12	DEF V_{CC}		
13	NC		
14 15 16	R OUT G OUT B OUT		

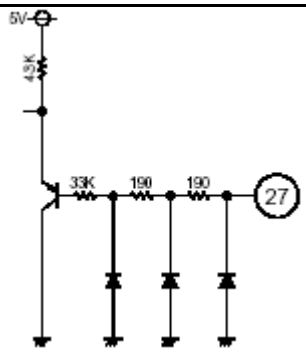
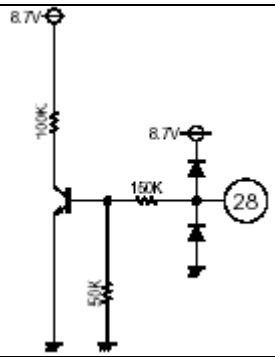
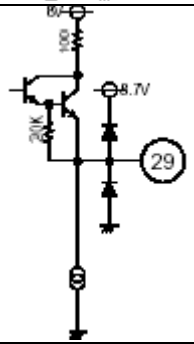
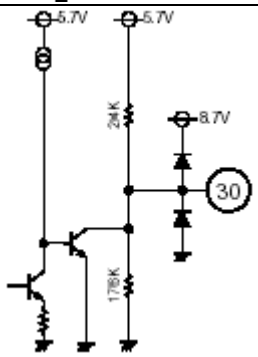
Pin Explanations (cont)

Pin No.	Name	Pin peripheral circuit	DC voltage (V)
17	H VCO FEEDBACK		3.0 V
18	INTELLIGENT MONITOR		
19	INV FBP OUT		V_{OL}: 0.0 V V_{OH}: 5.0 V
20	V PULSE OUT		V_{OL}: 0.0 V V_{OH}: 5.0 V

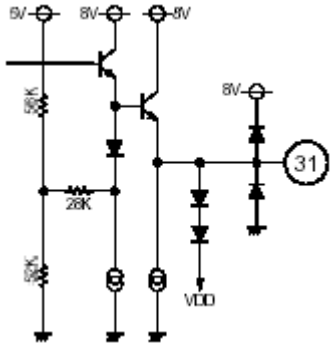
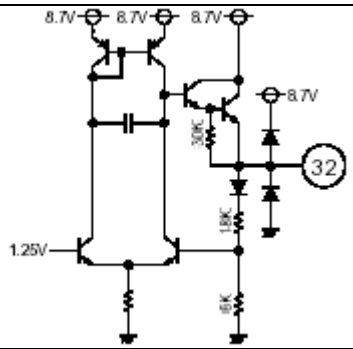
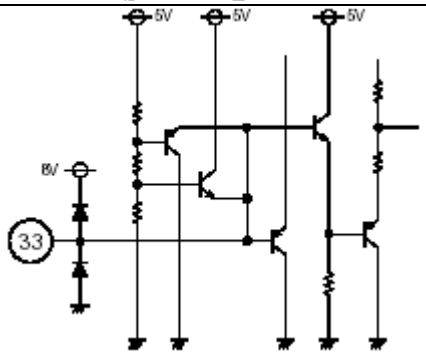
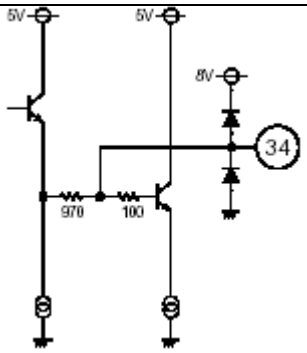
Pin Explanations (cont)

Pin No.	Name	Pin peripheral circuit	DC voltage (V)
21 22 23	B IN G IN R IN		(1) Digital OSD VIL: 0.0 V VIH: 3.0 V (2) Analog OSD 0.7 Vp-p
24	FAST BLK		0.0-0.5 V: INT RGB 1.5-3.0 V: H TONE 4.0-5.0 V: EXT RGB
25	CLK CONTROL		V_{TH}: 3.0 V
26	SDA		V_{IL}: 0.75 V V_{IH}: 4.25 V

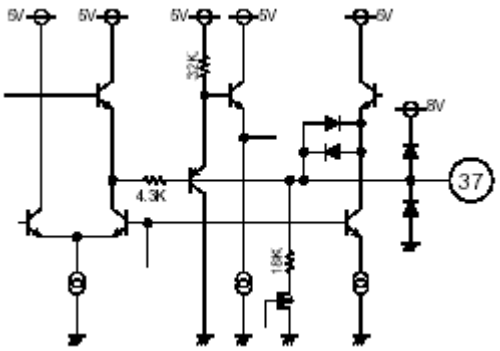
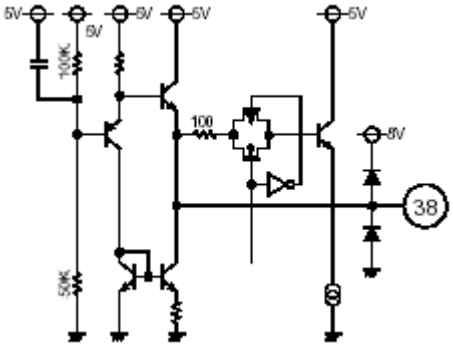
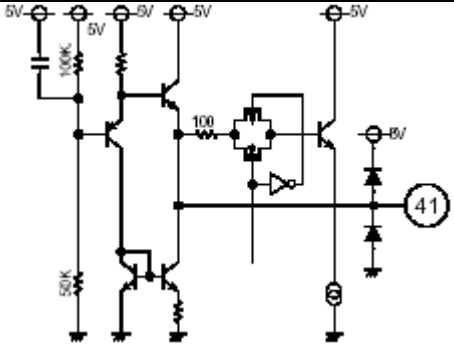
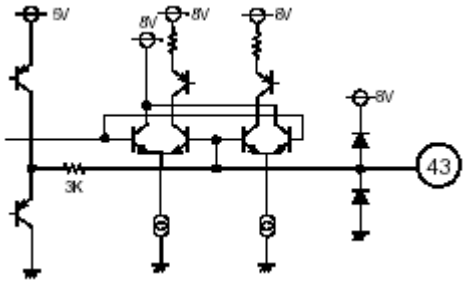
Pin Explanations (cont)

Pin No.	Name	Pin peripheral circuit	DC voltage (V)
27	SCL		V_{IL}: 0.75 V V_{IH}: 4.25 V
28	POWER ON CONTROL		V_{TH}: 3.0 V
29	fsc OUT 1		3.0 V
30	MCU RESET		H: 5.0 V L: 0.0 V

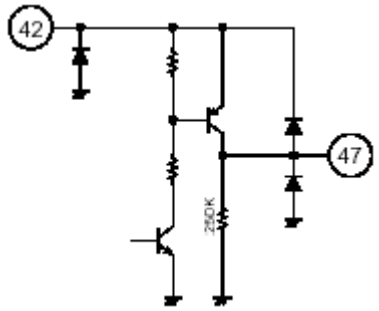
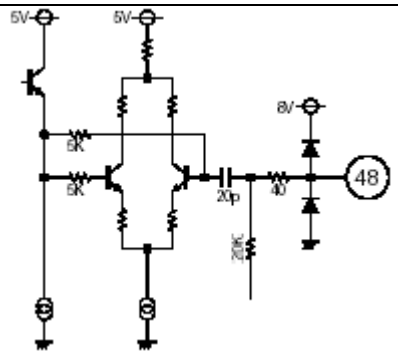
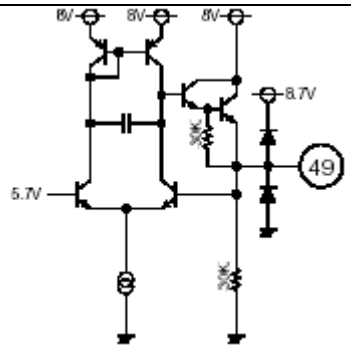
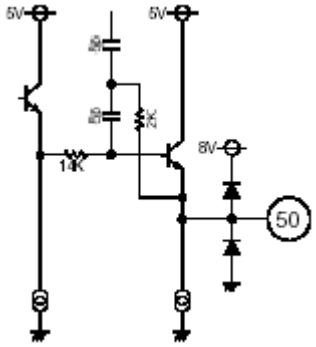
Pin Explanations (cont)

Pin No.	Name	Pin peripheral circuit	DC voltage (V)
31	Y SW OUT		1.7 V
32	MCU 5.7 VREG OUT		5.7 V
33	ACL/ABCL		
34	X-TAL 3.58		3.3 V
35	DRIVE GND		0.0 V
36	Video/Chroma GND		

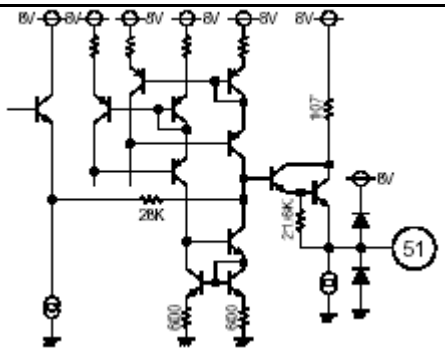
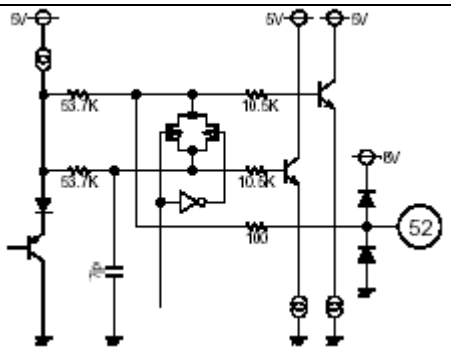
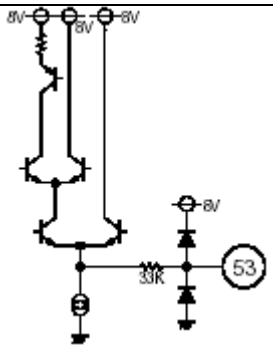
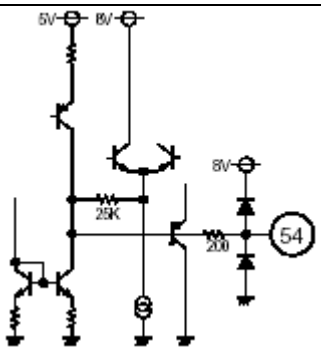
Pin Explanations (cont)

Pin No.	Name	Pin peripheral circuit	DC voltage (V)
37	CHROMA APC FILTER		3.2 V
38	EXT/C IN		1.7 V
39	DRIVE V_{CC}		5.0 V
40	Video/Chroma V_{CC}		
41	TV/Y IN		1.7 V
42	VREG V_{CC}		8.7 V
43	AUDIO ATT FILTER		2.75 V to 3.25 V
44	Hi V_{CC}		8 V
45	NC		
46			

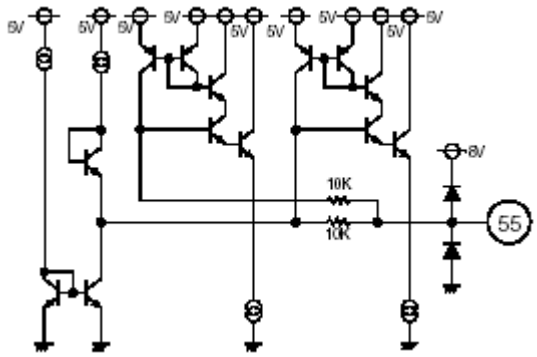
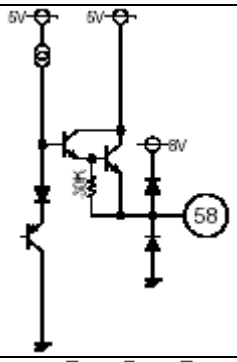
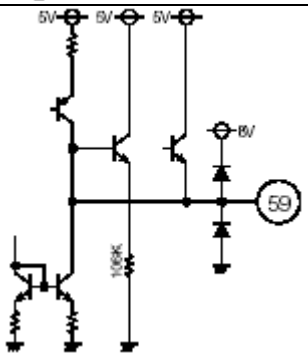
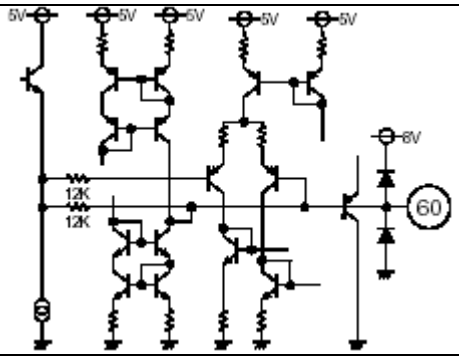
Pin Explanations (cont)

Pin No.	Name	Pin peripheral circuit	DC voltage (V)
47	8.7 VREG OUT		8.7 V
48	LIMITER IN		2.5 V
49	5.7 VREG OUT		5.7 V
50	INTER CARRIER OUT		2.3 V

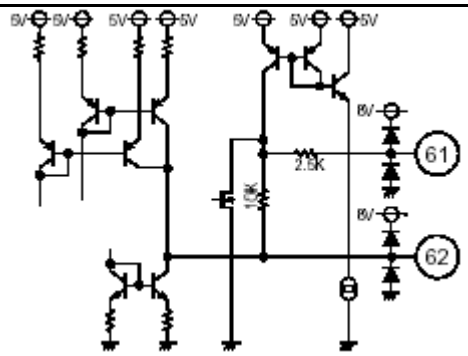
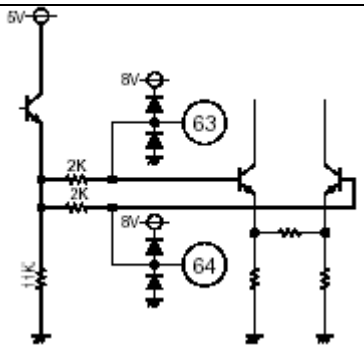
Pin Explanations (cont)

Pin No.	Name	Pin peripheral circuit	DC voltage (V)
51	AUDIO OUT		2.3 V
52	AUDIO BYPASS		2.3 V
53	EXT AUDIO IN		3.0 V
54	FM DIRECT OUT		3.0 V

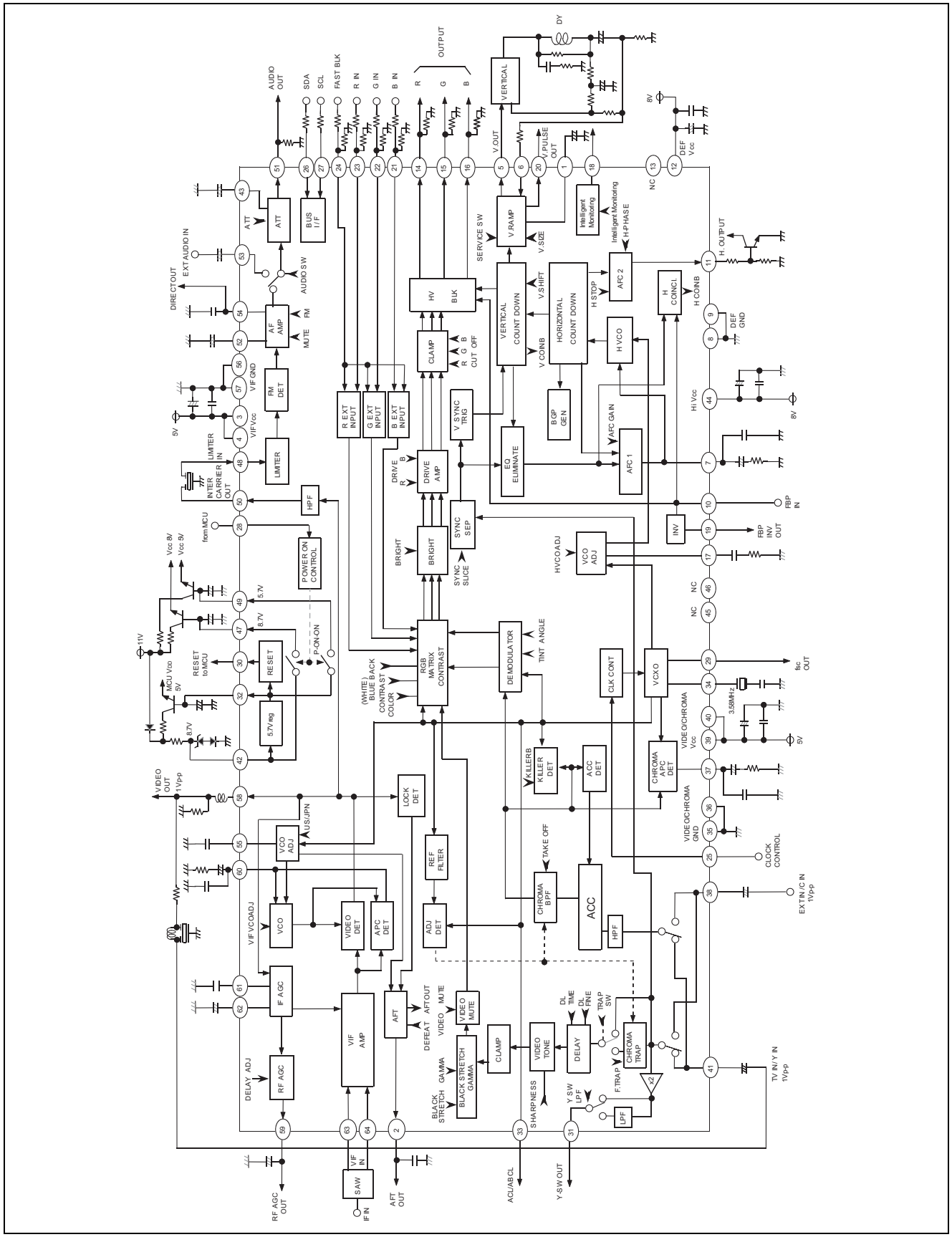
Pin Explanations (cont)

Pin No.	Name	Pin peripheral circuit	DC voltage (V)
55	VIF VCO FEEDBACK		3.0 V
56	SIF GND		
57	VIF GND		
58	VIDEO OUT		2.7 V
59	RF AGC OUT		0.3 to 4.7 V
60	VIF APC FILTER		3.0 V

Pin Explanations (cont)

Pin No.	Name	Pin peripheral circuit	DC voltage (V)
61 62	VIF AGC FILTER 2 VIF AGC FILTER 1		2.3 V
63 64	VIF IN (1) VIF IN (2)		1.6 V

Block Diagram

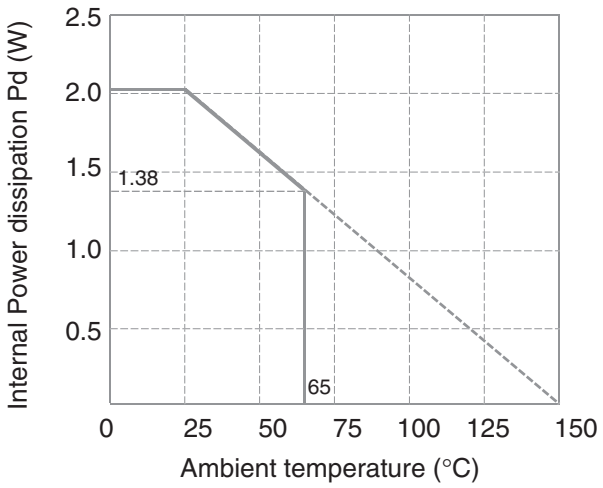


Absolute Maximum Ratings

(Ta = 25°C)

Item	Symbol	Rating	Unit
Power supply voltage	VCC	6.0, 10.0	V
Internal power dissipation	Pd	2026	mW
Thermal derating	Kt	16.2	mW/°C
Ambient operating temperature	Topr	–20 to +65	°C
Storage temperature	Tstg	–40 to +150	°C

Thermal Derating (Maximum Ratings)



I²C Bus Table

1. SLAVE ADDRESS= BAH(WRITE), BBH(READ)

A6	A5	A4	A3	A2	A1	A0	R/W
1	0	1	1	1	0	1	1/0

2. WRITE TABLE(input bytes)

SUB ADDRESS		DATA								
HEX	BIN	D7	D6	D5	D4	D3	D2	D1	D0	INITIAL
		(inhibited)	RF Delay Adj							
00H	00000000	0	1	0	0	0	0	0	0	40H
		(inhibited)	VIFFreq5875	VIF VCO ADJ						
01H	00000001	0	0	1	0	0	0	0	0	20H
		Video Mute	Audio EXT	C. Clip level	TRAP Off	Video T Sharp	ABCL	Black Stre. Off	Take Off	
02H	00000010	0	0	0	0	0	0	0	0	00H
		Audio Mute	Audio ATT							
03H	00000011	0	0	0	0	0	0	0	0	00H
		ABCL Gain	AFT Defeat	Video Tone						
04H	00000100	0	0	V1	V0	V0	V0	V0	V0	20H
		EXTRGB C. Clip	Contrast Control							
05H	00000101	V0	V1	V0	V0	V0	V0	V0	V0	40H
		VIF Video Out Gain			Y/C	EXT	Y DL Fine Adj	Y DL Time Adj		
06H	00000110	1	0	0	V0	V0	0	0	0	80H
		VIF Defeat	Tint Control							
07H	00000111	0	V1	V0	V0	V0	V0	V0	V0	40H
		Blue Back	Color Control							
08H	00001000	V0	V1	V0	V0	V0	V0	V0	V0	40H
		HV BLK OFF	VOUT STOP	FSC FREE	HTONE SW	(inhibited)				
09H	00001001	0	0	0	0	0	1	0	0	04H
		Brightness Control								
0AH	00001010	V1	V0	V0	V0	V0	V0	V0	V0	80H
		(inhibited)	Drive(R)							
0BH	00001011	0	1	0	0	0	0	0	0	40H
		(inhibited)	Drive(B)							
0CH	00001100	0	1	0	0	0	0	0	0	40H
		Cut Off(R)								
0DH	00001101	1	0	0	0	0	0	0	0	80H
		Cut Off(G)								
0EH	00001110	1	0	0	0	0	0	0	0	80H
		Cut Off(B)								
0FH	00001111	1	0	0	0	0	0	0	0	80H
		White Back	V-free	(inhibited)			H VCO Adj			
10H	00010000	0	0	1	0	0	1	0	0	24H
		(inhibited)		V-Size						
11H	00010001	0	0	1	0	0	0	0	0	20H
		Monitoring				Gamma Control		TRAP Fine Adj		
12H	00010010	0	0	0	0	0	0	0	0	00H
		H-free	V.1Window	YSW LPF	H Start	Service SW	V Shift			
13H	00010011	0	0	0	0	0	0	0	0	00H
		Black Strech Discharge		Black Strech Charge		S.Slice Down2	S.Slice Down1	(inhibited)		
14H	00010100	0	0	0	0	0	0	1	1	03H
		AFC1 Gain	AFC2 Gain	OSD level	Analog OSD	US/JPN SW			Killer level	
15H	00010101	0	0	0	0	0	0	0	0	00H
		VSYNCDET	Aoto slice down	FBP Vth L	AFC2 H Phase					
16H	00010110	1	0	0	1	0	0	0	0	90H
		(reserved)								
17H	00010111	0	V1	V0	V0	V0	V0	V0	V0	40H
		Test1		(inhibited)						
18H	00011000	0	0	0	0	0	0	0	0	00H
		BGPFBP OFF	Test2	(inhibited)						
19H	00011001	0	0	0	0	0	0	0	0	00H
		Test3		(inhibited)						
1AH	00011010	0	0	0	0	0	0	0	0	00H
		(inhibited)								
1BH	00011011	0	0	0	0	0	0	0	0	00H
		TEST4	VFREE INT	(inhibited)		VBLKSHIFT ON	VBLK SHIFT			
1CH	00011100	0	0	0	0	0	1	0	0	04H

NOTE: V0 / V1 ==> V- LATCH BIT

3. READ TABLE (output bytes)

SUB ADDRESS		D7	D6	D5	D4	D3	D2	D1	D0
00H	00000000	KILLERB	(not asigned)	VCOINB	STDETB	AFT0	AFT1	HCOINB	(not asigned)

Bus Functions

WRITE

	FUNCTION	BIT	SUB ADD	DATA	DISCRIPTION	INI-TIAL	NOTE
VIF SIF	RF delay adj	7	00H	D0-D6	RF AGC delay point adjustment	40H	
	VIF VCO adj	6	10H	D0-D5	VIF VCC free-running frequency adjustment (adjust by setting VIF Defeat = 1 to center the AFT output)	20H	
	VIF freq. 58.75	1	01H	D6	IF 45.75/58.75 switching; 0: 45.75, 1: 58.75 MHz	0	
	VIF Video out gain	3	06H	D5-D7	Pin 58 IVF video-detection-wave output level adjustment	80H	
	AFT defeat	1	04H	D6	AFT output on/off (defeat) switching; 0: AFT on (non defeat), 1: Defeat	0	
	VIF defeat	1	07H	D7	VIF AGC gain normal/minimum switching; 0: AGC function, 1: Defeat (minimum gain)	0	
	Audio ATT	7	03H	D0-D6	Pin 51 audio output level adjustment	00H	
	Audio EXT	1	02H	D6	Audio internal signal and external signal input switching; 0: internal, 1: external	0	
	Audio mute	1	03H	D7	Pin 53 audio direct output on/off (mute) switching; 0: audio on (non-muted), 1: mute	0	
VIDEO	Video tone	6	04H	D0-D5	Sharpness level control	20H	V Latch
	Contrast control	7	05H	D0-D6	Contrast level control	40H	V Latch
	EXTRGB contrast clip	1	05H	D7	EXT RGB contrast lower-limit clipping on/off; 0: clipping on, 1: clipping off	0	V Latch
	C. clip level	1	02H	D5	EXT RGB contrast lower-limit clipping level switching; 0: low (20H), 1: high (40H)	0	
	Y DL time adj	2	06H	D0-D1	Y signal delay adjustment	X0H	
	Y DL fine adj	1	06H	D2	Y signal delay fine adjustment	0	
	EXT	1	06H	D3	Video input pins 41/38 switching; 0: pin 41, 1: pin 38	0	V Latch
	Y/C	1	06H	D4	Pins 38/41 composite input/YC input switching; 0: composite, 1: Y/C mode	0	V Latch
	Y SW LPF	1	13H	D5	Pin 31 (Y SW OUT) output f-characteristic switching; 0: flat, 1: LPF (fc=700 kHz)	0	
	Video tone sharp	1	02H	D3	Video tone level two level (sharp/soft) switching; 0: standard (soft), 1: sharp	0	
	Video mute	1	02H	D7	Y signal output on/off (mute) switching; 0: mute off, 1: mute	0	
	TRAP off	1	02H	D4	Y signal chroma trap on/off switching; 0: trap on, 1: trap off	0	
	TRAP fine adj	2	12H	D0-D1	Chroma trap frequency fine adjust	X0H	
	Black stretch off	1	02H	D1	Black stretch circuit on/off switching; 0: black stretch on, 1: black stretch off	0	
	Black stretch charge	2	14H	D4-D5	Black stretch charge time constant adjustment	0XH	
	Black stretch discharge	2	14H	D6-D7	Black stretch discharge time constant adjustment	0XH	
	Gamma control	2	12H	D2-D3	Gamma level adjustment	X0H	
CHROMA	Tint control	7	07H	D0-D6	Hue control	40H	V Latch
	Color control	7	08H	D0-D6	Color level control	40H	V Latch
	Take off	1	02H	D0	Chroma BPF take-off function on/off switching; 0: BPF; 1: take off	0	
	US/JPN SW	1	15H	D1-D3	US mode/JPN mode switching; 100: US mode, 011: JPN mode	0	
	Killer level	1	15H	D0	Colorkiller sensitivity switching (active shallow direction); 0: 41 dB,1: 34 dB	0	
	Fsc	1	09H	D5	X'tal oscillation circuit forced free-running mode; 0: off, 1: free-running	0	

Bus Functions (cont)

WRITE (cont)

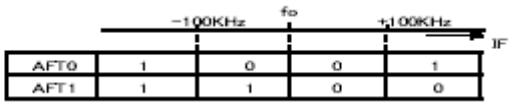
	FUNCTION	BIT	SUB ADD	DATA	DISCRIPTION	INI-TIAL	NOTE
RGB	Brightness control	8	0AH	D0-D7	Bright level control	80H	V Latch
	Driver (R)	7	0BH	D0-D6	R output level control	40H	
	Driver (B)	7	0CH	D0-D6	B output level control	40H	
	Cut off (R)	8	0DH	D0-D7	R output DC level control	80H	
	Cut off (B)	8	0EH	D0-D7	G output DC level control	80H	
	Cut off (B)	8	0FH	D0-D7	B output DC level control	80H	
	Blue back	1	08H	D7	Blue back screen on/off switching; 0: off, 1: blue back	0	
	White back	1	10H	D7	White raster on/off switching; 0: off, 1: white back	0	
	ABCL	1	02H	D2	ABCL on/off switching; 0: off, 1: ABCL on	0	
	ABCL gain	1	04H	D7	ABCL sensitivity low/high switching; 0: low, 1: hi	0	
	OSD level	1	15H	D5	OSD level (70%/90%) switching; 0: 70%, 1: 90%	0	
	HTONE SW	1	09H	D4	Halftone on/off switching; 0: off, 1: halftone	0	
	Analog OSD	1	15H	D4	OSD input digital/analog switching; 0: digital, 1: analog	0	
DEF	AFC2 H phase	5	16H	D0-D4	Screen horizontal position adjustment	90H	
	Ramp stop	1	09H	D6	Pin 5 VOUT (ramp/pulse) forced stop mode (when stopped, pin 5 at DC GND level); 0: VOUT, 1: STOP	0	
	Service SW	1	13H	D3	Vertical output on/off switching; 0: vertical output on, 1: vertical output off	0	
	H start	1	13H	D4	Horizontal output out/stop switching; 0: stop, 1: H out	0	
	AFC 1 gain	1	15H	D7	Horizontal AFC gain a high/low switching; 0: low, 1: hi	0	
	AFC 2 gain	1	15H	D6	Horizontal AFC2 gain high/low switching; 0: high, 1: low	0	
	H VCO adj	3	10H	D0-D2	H VCO free-running frequency adjustment	24H	
	V shift	3	13H	D0-D2	Vertical ramp start timing adjustment	X0H	
	V-size	6	11H	D0-D5	Vertical ramp amplitude adjustment	20H	
	H-free	1	13H	D7	Horizontal output forced free-running mode on/off switching; 0: off, 1: horizontal free-running	0	
	V-free	1	10H	D6	Vertical output forced free-running mode on/off switching; 0: off, 1: vertical free-running	0	
	S slice down 1	1	14H	D2	Sync detection slice level (50%/30%) switching; 0: 50%, 1: 30%	0	
	S slice down 2	1	14H	D3	Sync detection slice level (50%/40%) switching; 0: 50%, 1: 40%	0	
	Audio slice down	1	16H	D6	Sync detection slice level (50%/40%) switching during image period; 0: slice level fixed, 1: slice level reduced	0	
	FBP Vth L	1	16H	D5	Pin 10 (FBP in) slice level switching during image period; 0: Vth = 2V (HBLK width: narrow), 1: Vth = 1 V (HBLK width: wide)	0	
	HV BLK OFF	1	09H	D7	Horizontal/vertical blanking on/off switching; 0: blanking on, 1: blanking off	0	
	V SYNK DET	1	16H	D7	Vertical minimum sync detection width switching; 0: sync detect width =18 µs, 1: sync detect width =14 µs	90H	
	1 window	1	13H	D6	Vertical sync detection switching (1 window/2 window s); 0: 2 windows, 1: 1 window	0	
	BGPFBP OFF	1	19H	D7	Internal BGP on/off switching when no FBP input; 0: BGP on, 1: BGP off	0	
	VREF INT	1	1CH	D6	Interface/non-interface switching at vertical free-running	04H	
	VBLK SHIFT ON	1	1CH	D3	0: Normal (VBLK shifts by VSHIFT), 1: Vertical blanking width can be setted by un-interlocking VSHIFT	04H	
	VBLK SHIFT	3	1CH	D0-D2	D0-D2: VBLK SHIFT (Initial value: 100=4)	04H	
	Monitoring	4	12H	D4-D7	Pin 18 intelligent monitoring mode switching	0XH	
	Test1	1	18H	D6-D7	NO use for Customer (Test bit)	0	
	Test2	1	19H	D6	NO use for Customer (Test bit)	0	
	Test3	1	1AH	D6-D7	NO use for Customer (Test bit)	0	
	Test4	1	1CH	D6	NO use for Customer (Test bit)	04H	

READ

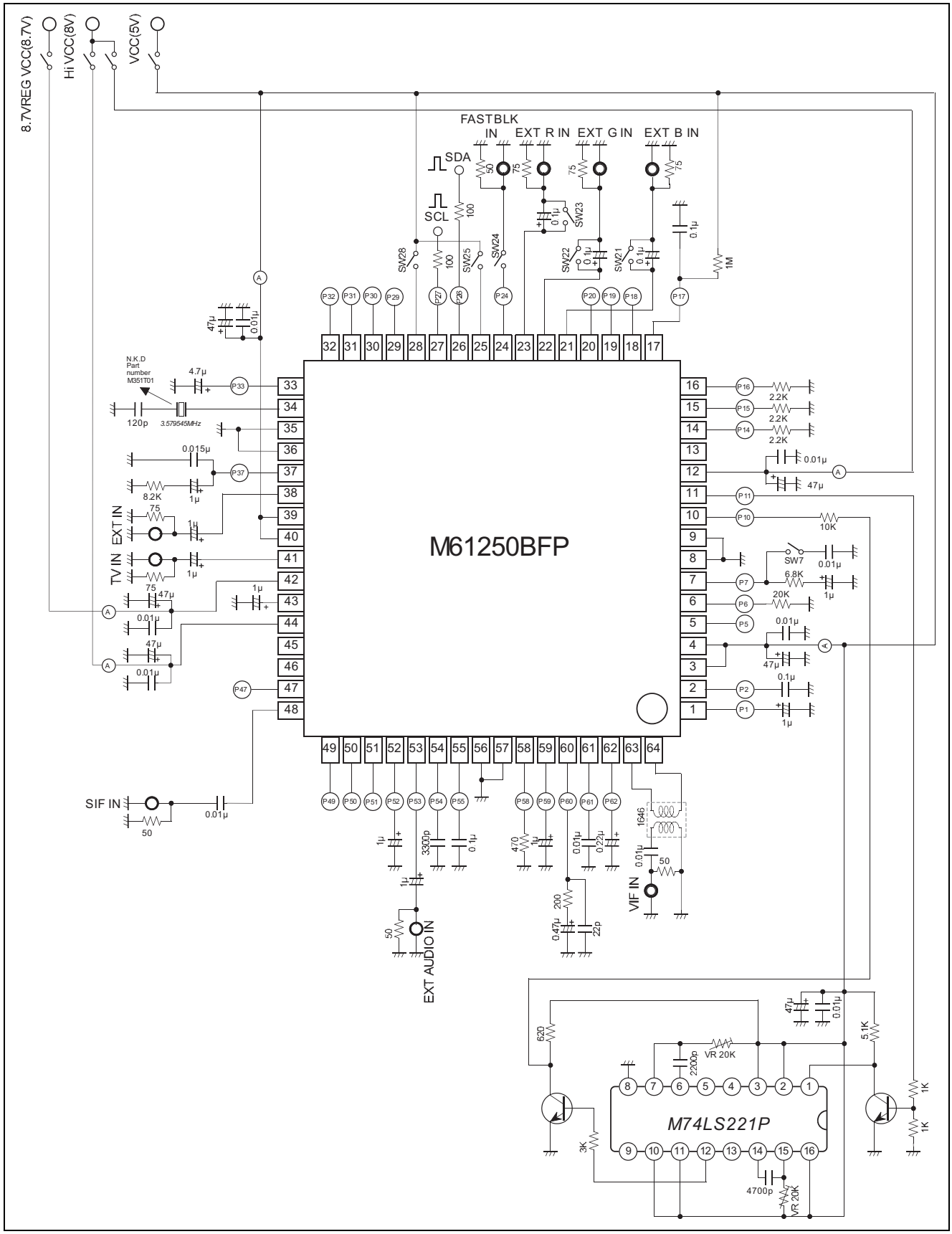
FUNCTION	BIT	SUB ADD	DATA	DISCRIPTION
KILLERB	1	00H	D7	Colorkiller information output; "1" when killer off
AFT0	1	00H	D3	AFT information output (See note 1)
AFT1	1	00H	D2	AFT information output (See note 1)
HCOINB	1	00H	D1	Horizontal sync detection; "1" when asynchronous
FM STDETB	1	00H	D6	FM radio mode detection; "1" when not detected
VCOINB	1	00H	D5	Vertical sync detection; "1" when asynchronous
STDETB	1	00H	D4	TF mode detection; "1" when not detected

Note: 1. <READ BYTE: AFT OUTPUT>

AFT0/AFT1



Test Circuits

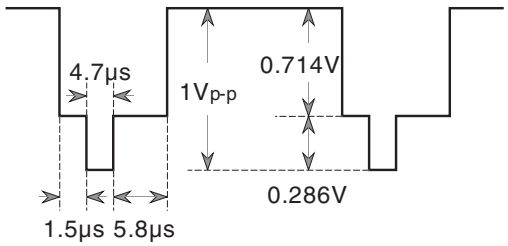
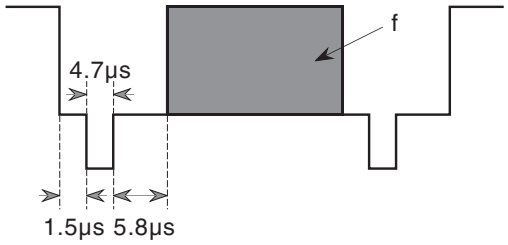
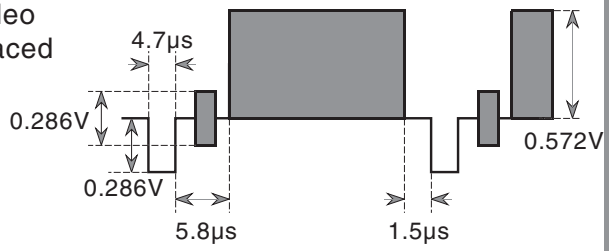
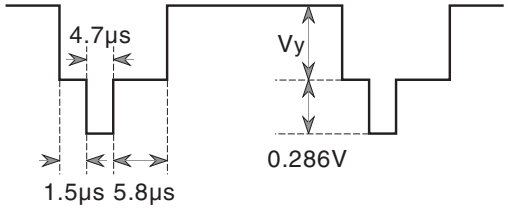
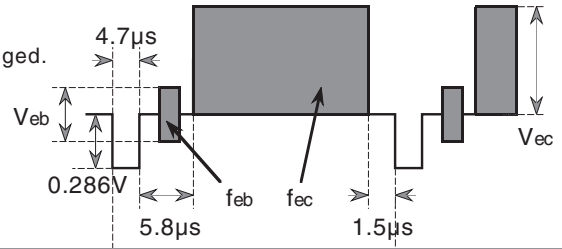
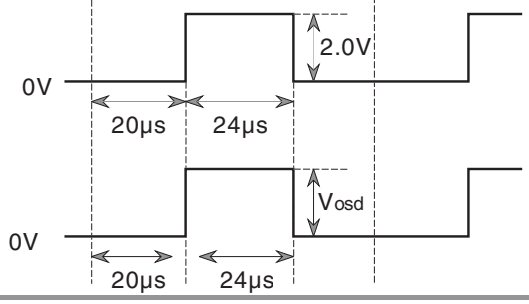


Input Signals

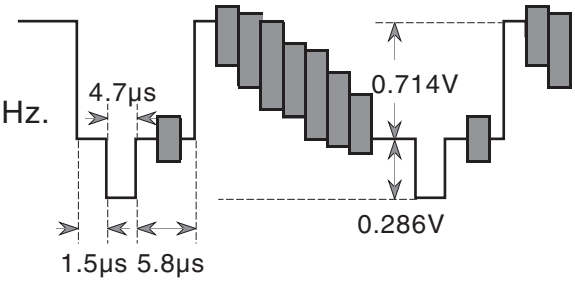
1. 10.1 VIF/SIF Block

SG No.	Signal description (50 Ω termination)
SG1	fo = 45.75 MHz, 90 dBμ, fm = 20 kHz, AM 77.8%
SG2	fo = 58.75 MHz, 90 dBμ, fm = 20 kHz, AM 77.8%
SG3	fo = 45.75 MHz, 90 dBμ, CW
SG4	f1 = 45.75 MHz, 90 dBμ, CW f2 = 45.75 ± 4.5MHz, 70 dBμ, CW
SG5	fo = 45.75 MHz, amplitude width variable, fm = 20 kHz, AM 77.8%
SG6	fo = 45.75 MHz, amplitude width variable, fm = 20 kHz, AM 16%
SG7	fo = 45.75 MHz, 80 dBμ, fm = 20 kHz, CW
SG8	fo = 45.75 MHz, 110 dBμ, fm = 20 kHz, CW
SG9	fo = 40.75 to 50.75 MHz (frequency variable), 90 dBμ, CW
SG10	fo = 45.75 MHz, 90 dBμ, CW
SG11	fo = 45.75 MHz, 90 dBμ, CW
SG12	fo = 53.75 to 63.75 MHz (frequency variable), 90 dBμ, CW
SG13	f1 = 45.75 MHz, 90 dBμ, RED raster signal, AM = 87.5% video modulation, f2 = 4.5 ± 4.5MHz, CW, P/S = 20 dB
SG14	fo = 45.75 MHz, standard 10-step wave, sync rate: 28.6%, AM = 87.5% video modulation, sync chip level: 90 dBμ
SG15	fo = 45.75 MHz, 93 dBμ, CW
SG16	fo = 45.75 MHz, 73 dBμ, CW
SG17	fo = 4.5 MHz, 100 dBμ, fm = 400 Hz, FM ±25 kHz dev.
SG18	fo = 4.5 MHz, 100 dBμ, fm = 400 kHz, AM 30%
SG19	fo = 4.5 MHz, 100 dBμ, CW
SG20	fo = 400 Hz, 500 mVrms, CW
SG21	fo = 0.5 to 8.5 MHz, 100 dBμ, fm = 400 kHz, FM ±25 kHz dev.

2. Video/Chroma/RGB/DEF Block

SG No.	Signal description (75Ω termination)
SG. A	NTSC format APL 100% typical video signal. Vertical signal is interlaced at 60 Hz. 
SG. B	In the SG.A signal, the Lumi. signal frequency and amplitude can be changed. However, typical amplitude is 0.714 Vp-p. In the figure on the right, the Lumi. signal is represented by f. 
SG. C	NTSC typical monochrome video signal. Vertical signal is interlaced at 60 Hz. 
SG. D	NTSC format video signal; APL variable. Vertical signal is interlaced at 60 Hz. 
SG. E	NTSC format monochrome video signal. In the SG.C signal, the burst and chroma part frequency and amplitude can be changed. Vertical signal is interlaced at 60 Hz. (Typical state: Veb=0.286V, Vec=0.572V feb=fec=3.579545MHz) 
SG. F	Fast blanking signal; synchronized with video input signal. Fast blanking signal; synchronized with video input signal. 

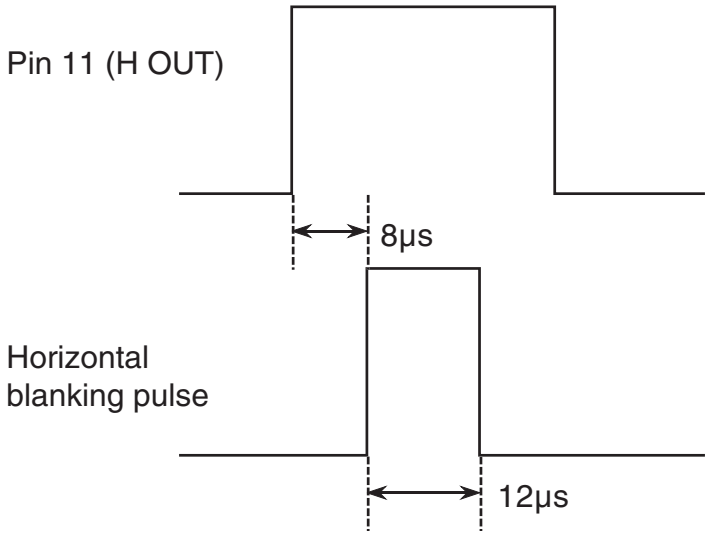
2. Video/Chroma/RGB/DEF Block (cont)

SG No.	Signal description (75Ω termination)
SG. G	NTSC format rainbow color bar video signal. Vertical signal is interlaced at 60 Hz.
SG. H	Duty 90%, variable frequency, variable level. (Typical: 1 Vp-p) 
SG. I	Duty variable (typical 95%), frequency variable, level variable (Typical: 1 Vp-p) 
SG. J	NTSC format typical color bar video signal; vertical signal is interlaced at 60 Hz. 
SG. K	NTSC format, typical 8-step wave signal; vertical signal is interlaced at 60 Hz.

Setup instruction for evaluation PCB

1. Horizontal blanking pulse adjustment

The horizontal blanking pulse timing and pulse width are adjusted using the variable resistances of a one-shot multivibrator, as shown below.

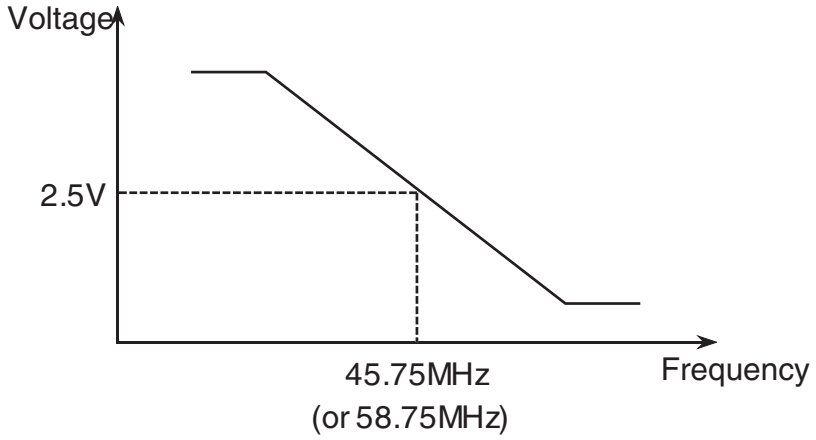


The timing is adjusted to 8 µs using the pin 15 variable resistance of the M74LS221P TTL IC. Also, the pulse width is adjusted to 12 µs using the pin 7 variable resistance.

2. VIF VOC adjustment

Before carrying out the M61250BFP measurements, the VIF VCO should be adjusted using the following procedure.

(1) Input the I^2C bus data for the VIF frequency (01H D6) based on the IF frequency. (45.75 MHz: 0, 58.75 MHz: 1)
(2) Input the I^2C bus data for VIF Defeat ON (07H D7 = 1).
(3) Adjust the I^2C bus data for the VCO control (01H D0 – D5) so that the voltage of Pin 2 (AFT OUT) is closest to 2.5 V.
(4) Input the I^2C bus data for VIF Defeat OFF (07H D7 = 0).



3. H VCO adjustment

Prior to measurement of the M61250BFP, the following method is used for H VCO adjustment.

(1) The H VCO control I^2C bus data (1 CH D0-D3) is adjusted, and the pin 11 (H OUT) frequency is set to approx. 15.734 kHz.

Electrical Characteristics

(Ta = 25°C)

Symbol	Item	Input signal		Test point	Limits			Unit	Notes	Subaddress																						
		Pin	SG		Min.	Typ.	Max			00H	01H	02H	03H	04H	05H	06H	07H	08H	09H	0AH	0BH	0CH	0DH	0EH	0FH	10H	11H	12H	13H	14H	15H	16H	17H	18H	19H	1AH	1BH	1CH
ICC	Typical conditions								Pin 28=5 V, pin 25=5 V, pin 24=0 V	40	20	02	00	20	40	80	40	40	00	80	40	40	80	80	80	24	20	00	10	00	00	88	40	00	00	00	00	00
ICC5V	5V current drawn by the circuit (pins 3, 4, 39, 40)	-	-	3,4,39,40	95	115	135	mA	VIF/SIF/VIDEO/Chroma Vcc																													
ICC34	*Pins 3 and 4 current drawn by the circuit*	-	-	*3,4*	-	*57*	-	*mA*	*Reference data VIF/SIF/Vcc*																													
ICC3940	*Pins 39 and 40 current drawn by the circuit*	-	-	*39,40*	-	*57*	-	*mA*	*Reference data VIDEO/Chroma Vcc*																													
ICC8V	8V current drawn by the circuit	-	-	12,44	32	42	52	mA	Deflection/RGB Drive 8V Vcc																													
ICC12	*Pin 12 current drawn by the circuit*	-	-	*12*	-	*25*	-	*mA*	*Reference data Deflection Vcc*																													
ICC44	*Pin 44 current drawn by the circuit*	-	-	*44*	-	*17*	-	*mA*	*Reference data RGB Drive 8V Vcc*																													
ICC42	Pin 42 current drawn by the circuit	-	-	42	4	6	8	mA	8.7 VREG Vcc																													
Power	Power supply circuit typical conditions								Pin 28=5 V, pin 25=0 V, pin 24=0 V	40	adj	02	00	20	40	80	40	40	00	80	40	40	80	80	80	24	20	00	10	00	00	88	40	00	00	00	00	00
Vth28	Power on control threshold voltage	-	-	28	2.6	3	3.4	V																														
V47H	8.7 VREG output voltage 1		-	47	8.3	8.7	9.1	V	Pin 28=5 V																													
V47L	8.7 VREG output voltage 2		-	47	-	0	0.3	V	Pin 28=0 V																													
V49	5.7 VREG output voltage 1		-	49	5.5	5.75	6.0	V	Pin 28=5 V																													
V32H1	MCU 5.7 VREG output voltage 1	-	-	32	5.4	5.65	5.9	V	Pin 28=5 V																													
V32H2	MCU 5.7 VREG output voltage 2	-	-	32	5.4	5.65	5.9	V	Pin 28=0 V																													
Reset	Reset typical conditions								Pin 28=5V, pin 25=5V	40	adj	02	00	20	40	80	40	40	00	80	40	40	80	80	80	24	20	00	10	00	00	88	40	00	00	00	00	00
V30H	Maximum reset output voltage	-	-	30	4.5	5	5.5	V																														
V30L	Minimum reset output voltage	-	-	30	-	0	0.5	V																														
TH32	Reset threshold voltage	-	-	32	4	4.2	4.4	V																														
IIC	IIC typical conditions	-	-	-	-	-	-	-		40	adj	02	00	20	40	80	40	40	00	80	40	40	80	80	80	24	20	00	10	00	00	88	40	00	00	00	00	00
IACK	*ACK current*	-	-		-	*1*	-	*mA*	*Reference data*																													
VIL	SCL/SDA VTH(L)	-	-	26,27	0.0	0.75	1.5	V																													
VIH	SCL/SDA VTH(H)	-	-	26,27	3.5	4.25	5.0	V																													
FSCL	Clock frequency	-	-	27	-	-	100	kHz																													

Symbol	Item	Input signal		Test point	Limits			Unit	Notes	Subaddress																															
		Pin	SG		Min.	Typ.	Max.			00H	01H	02H	03H	04H	05H	06H	07H	08H	09H	0AH	0BH	0CH	0DH	0EH	0FH	10H	11H	12H	13H	14H	15H	16H	17H	18H	19H	1AH	1BH	1CH
VIF	IF typical conditions								Pin 28=5 V, pin 25=5 V, pin 24=0 V	40	adj	02	00	20	40	80	40	40	00	80	40	40	80	80	80	24	20	00	10	00	00	88	40	00	00	00	00	00
Vdc	Video-detection-waveform output direct current voltage	-	-	58	2.2	2.7	3.2	V	Pin 62=0 V																															
Vo4575	Video-detection-waveform output (45.75 MHz)	63,64	SG1	58	0.8	1.2	1.5	Vpp																															
Vo5875	Video-detection-waveform output (48.75 MHz)	63,64	SG2	58	0.8	1.2	1.5	Vpp			+40																												
P/N	Video S/N	63,64	SG3	58	43	50	-	dB																															
Vf	Video frequency characteristics	63,64	SG4	58	4	5.4	-	MHz																															
Vin min	Input sensitivity	63,64	SG5	58	-	45	50	dBμ																															
Vin max	Maximum allowable input	63,64	SG6	58	100	108	-	dBμ																															
GR	AG control range	-	-	-	50	-	-	dB	Vo max - Vo min																															
V63H	IF AGC maximum voltage	-	-	62	3.8	4.3	4.8	V																															
V63T	IF AGC voltage (80 dBμ)	63,64	SG7	62	2.3	2.8	3.3	V																															
V63L	IF AGC minimum voltage	63,64	SG8	62	1.3	1.8	2.3	V																															
Vdefeat	VIF DETEAT function	63,64	SG1	58	0	0.1	0.2	V_{pp}								80																							
μAFT	AFT-detection-waveform sensitivity	63,64	SG9	2	7	10	13	mV/kHz																															
V60H	AFT maximum voltage	63,64	SG10	2	4.2	4.7	-	V																															
V60L	AFT minimum voltage	63,64	SG11	2	-	0.3	0.8	V																															
V60D	AFT DETEAT function	-	-	2	2.0	2.5	3.0	V								80																							
VCU45	Capture range (45.75MHz upper)	63,64	SG9	58	1.5	2.2	-	MHz	Center frequency=45.75MHz																															
VCL45	Capture range (45.75MHz lower)	63,64	SG9	58	-	-1.8	-1.1	MHz	Center frequency=45.75MHz																															
VCT45	Capture range (45.75MHz total)	-	-	58	2.6	4.0	-	MHz	VCU45-VCL45																															
VCU58	Capture range (58.75MHz upper)	63,64	SG12	58	1.5	2.2	-	MHz	Center frequency=58.75MHz		+40																												
VCL58	Capture range (58.75MHz lower)	63,64	SG12	58	-	-1.8	-1.1	MHz	Center frequency=58.75MHz		+40																												
VCT58	Capture range (58.75MHz total)	-	-	58	2.6	4.0	-	MHz	VCU58-VCL58																															
IM	*Inter modulation*	*63,64*	*SG13*	*58*	-	*42*	-	*dB*	*Reference data*																															

Symbol	Item	Input signal		Test point	Limits			Unit	Notes	Subaddress																															
		Pin	SG		Min.	Typ.	Max.			00H	01H	02H	03H	04H	05H	06H	07H	08H	09H	0AH	0BH	0CH	0DH	0EH	0FH	10H	11H	12H	13H	14H	15H	16H	17H	18H	19H	1AH	1BH	1CH
DG	*DG*	*63,64*	*SG14*	*58*	-	*3*	-	*%*	*Reference data*																															
DP	*DP*	*63,64*	*SG14*	*58*	-	*3*	-	*deg*	*Reference data*																															
V62H	RF AG maximum voltage	63,64	SG15	59	4.3	4.8	-	V																																
V62L	RF AG minimum voltage	63,64	SG16	59	-	0.2	0.7	V																																
DLPH	RF AG delay maximum point	63,64	SG5	59	95	108	-	dBμ		00																														
DLPL	RF AG delay minimum point	63,64	SG5	59	-	58	71	dBμ		7F																														
DLP	RF AG delay point adjustment range	-	-	-	33	43	-	dBμ	DLPH-DLPL	00-7F																														
SPN	Sync rate	63,64	SG14	58	25	28	33	%																																
SIF	SIF typical conditions								Pin 28=5 V, pin 25=5 V, pin 24=0 V	40	adj	02	00	20	40	80	40	40	00	80	40	40	80	80	80	24	20	00	10	00	00	88	40	00	00	00	00	00
VAF	AF direct output DC voltage	-	-	54	2.2	3.0	3.8	V					80																											
VoAF	AF direct output voltage	48	SG17	54	280	400	520	mV_{rms}																																
THD AF	AF distortion rate output	48	SG17	54	-	0.5	3	%																																
LIM	Input limit sensitivity	48	SG17	54	-	46	58	dBμ																																
AMR	AMR	48	SG18	54	48	54	-	dB																																
AFSN	AF S/N	48	SG19	51	49	55	-	dB					7F																											
GEAu	EXT Audio gain	53	SG20	51	-4.1	-2.1	-0.1	dB				40	7F																											
SCFU	SIF capture range (upper)	48	SG21	54	5.5	7.5	-	MHz	Variable input frequency																															
SCFL	SIF capture range (lower)	48	SG21	54	-	3	4.0	MHz	Variable input frequency																															
VOL-max	Audio output maximum amplitude	48	SG17	51	280	400	550	mV_{rms}					7F																											
VOL-min	Audio output maximum attenuation	48	SG17	51	-	-80	-69	dB																																

Symbol	Item	Input signal		Test point	Limits			Unit	Notes	Subaddress																																	
		Pin	SG		Min.	Typ.	Max.			00H	01H	02H	03H	04H	05H	06H	07H	08H	09H	0AH	0BH	0CH	0DH	0EH	0FH	10H	11H	12H	13H	14H	15H	16H	17H	18H	19H	1AH	1BH	1CH
VIDEO	Video typical conditions	-	-	-	-	-	-	-	Pin 28=5 V, pin 25=5 V, pin 24=0 V	40	adj	02	00	20	40	80	40	40	00	80	40	40	80	80	80	24	20	00	10	00	00	88	40	00	00	00	00	00
2AGTV	Video SW output level (TV input)	41	SG.A	31	1.6	2.0	2.6	V_{pp}																																	
2AGEV	Video SW output level (External input)	38	SG.A	31	1.6	2.0	2.6	V_{pp}							8C																									
Ymax	Maximum video output	38	SG.A	14,15, 16	2.9	4.2	5.6	V						7F	8C		00																						
GY	Video gain	38	SG.A	14,15, 16	12	15	18	dB						7F	8C		00																						
FBY	Video frequency characteristic	38	SG.B	14,15, 16	-4	-1	-	dB	f=5MHz, C-trap : OFF			10			7F	8C		00																						
CRF1	Chroma trap attenuation 1	38	SG.C	14,15, 16	-	-	-18	dB							8C			00											02										
TRF	Chroma trap maximum attenuation	38	SG.C	14,15, 16	-	-	-20	dB	At Trap fine adj. adjustment						8C			00											00-03										
YDL1	YDL time 1	38	SG.A	14,15, 16	190	260	330	nS							8C			00																					
YDL2	YDL time 2	38	SG.A	14,15, 16	120	200	280	nS	YDL2=measured value -YDL1 measured value							8D		00																						
YDL3	YDL time 3	38	SG.A	14,15, 16	120	200	280	nS	YDL3=measured value -YDL2 measured value							8E		00																						
YDL4	YDL time 4	38	SG.A	14,15, 16	120	200	280	nS	YDL4=measured value -YDL3 measured value							8F		00																						
GTnor	Video tone control characteristic 1	38	SG.B	14,15, 16	1.0	1.4	1.8	V	f=2.5MHz							8C		00																						
GTmax	Video tone control characteristic 2	38	SG.B	14,15, 16	7	10	14	dB	f=2.5MHz					3F		8C		00																						
GTmin	Video tone control characteristic 3	38	SG.B	14,15, 16	-6	-2	2	dB	f=2.5MHz					00		8C		00																						
GT2M	Video tone control characteristic 4	38	SG.B	14,15, 16	-1	2	5	dB	f=2MHz							8C		00																						
GT5M	Video tone control characteristic 5	38	SG.B	14,15, 16	-9	-5	-1	dB	f=5MHz							8C		00																						
BLS	Black expansion characteristic	38	SG.K	14,15, 16	0.01	0.03	0.05	V							adj	8C		00		adj										80									
VMF	Video mute function	38	SG.A	14,15, 16	-	-45	-35	dB				80			7F	8C		00																					

Symbol	Item	Input signal		Test point	Limits			Unit	Notes	Subaddress																															
		Pin	SG		Min.	Typ.	Max.			00H	01H	02H	03H	04H	05H	06H	07H	08H	09H	0AH	0BH	0CH	0DH	0EH	0FH	10H	11H	12H	13H	14H	15H	16H	17H	18H	19H	1AH	1BH	1CH
CHROMA	Chroma typical conditions	-	-	-	-	-	-	-	Pin 28=5 V, pin 25=5 V, pin 24=0 V	40	adj	02	00	20	40	80	40	40	00	80	40	40	80	80	80	24	20	00	10	00	00	88	40	00	00	00	00	00
CnorR	Chroma typical output (R-Y)	38	SG.C	59	390	560	790	mV								88																		C0	40			
CnorB	Chroma typical output (B-Y)	38	SG.C	59	640	920	1290	mV								88																		80	40			
ACC1	ACC characteristic 1	38	SG.E	59	-3	0	3	dB	Veb, Vec: typical input level +6 dB							88																		80	40			
ACC2	ACC characteristic 2	38	SG.E	59	-4.5	0	1.5	dB	Veb, Vec: typical input level -20 dB							88																		80	40			
OV	Chroma overload characteristic	38	SG.E	59	-3	2	5	dB	V = 800 mV							88																		80	40			
VikN	Killer operation input level	38	SG.E	59	-	-43	-35	dB	Veb, Vec: variable							88																		80	40			
KillP	Color remaining on colorkilling	38	SG.E	59	-	-45	-30	dB	V_{eb} = 0mV							88																		80	40			
APCU	APC pull-in range (upper)	38	SG.E	59	-	-600	-300	Hz	feb=fec: variable							88																		80	40			
APCL	APC pull-in range (lower)	38	SG.E	59	300	600	-	Hz	feb=fec: variable							88																		80	40			
R/BN	Demodulation ratio	38	SG.E	59	0.40	0.57	0.80	-	f_{ec}=f_{eb}+50kHz							88																		C0/80	40			
R/BU	*Demodulation ratio (US mode)*	*38*	*SG.J*	*14,15*	-	1.33	-	-	*Reference data*						20	88				FF												08			C0/80	40			
G/BU	*Demodulation ratio (US mode)*	*38*	*SG.J*	*15,16*	-	0.43	-	-	*Reference data*						20	88				FF												08			C0/80	40			
R/BJ	*Demodulation ratio (JPN mode)*	*38*	*SG.J*	*14,15*	-	1.31	-	-	*Reference data*						20	88				FF												06			C0/80	40			
G/BJ	*Demodulation ratio (JPN mode)*	*38*	*SG.J*	*15,16*	-	0.47	-	-	*Reference data*						20	88				FF												06			C0/80	40			
R-YN1	Demodulation angle 1	38	SG.E	59	86	103	120	deg	f_{ec}=f_{eb}+50kHz							88																		C0/80	40			
R-YN2	Demodulation angle 2	38	SG.E	59	73	90	107	deg	f_{ec}=f_{eb}+50kHz							88																02			C0/80	40			
TC1	TINT control characteristic 1	38	SG.E	59	30	45	60	deg	f_{eb}=f_{ec}+50kHz							88	F7																	80	40			
TC2	TINT control characteristic 2	38	SG.E	59	30	45	60	deg	f_{eb}=f_{ec}+50kHz							88	00																	80	40			
Ffsc	fsc output frequency	38	SG.C	29	3.5793	3.5796	3.5799	MHz								88																							
Vfsc	fsc output amplitude 1	38	SG. C	29	1.4	2	2.6	V_{pp}								88																							
Ffscfree	fsc output frequency in fsc free mode	38	SG.C	29	3.5790	3.5795	3.5810	MHz								88			20																				
Vfsc	fsc output amplitude 1 in fsc free mode	38	SG.C	29	1.4	2	2.6	V_{pp}								88			20																				

Symbol	Item	Input signal		Test point	Limits			Unit	Notes	Subaddress																													
		Pin	SG		Min.	Typ.	Max.			00H	01H	02H	03H	04H	05H	06H	07H	08H	09H	0AH	0BH	0CH	0DH	0EH	0FH	10H	11H	12H	13H	14H	15H	16H	17H	18H	19H	1AH	1BH	1CH
RGB	RGB typical conditions	-	-	-	-	-	-	-	Pin 28=5 V, pin 25=5 V, pin 24=0 V	40	adj	02	00	20	40	80	40	40	00	80	40	40	80	80	80	24	20	00	10	00	00	88	40	00	00	00	00	00
VBLK	Output blanking voltage	38	SG.A	14,15, 16	0	0.1	0.3	V								88		00																					
GYtyp	Contrast control characteristic 1	38	SG.B	14,15, 16	2.2	2.8	3.3	V_{pp}	f=100kHz							88		00																					
GYmin	Contrast control characteristic 2	38	SG.B	14,15, 16	-	200	300	mV	f=100kHz						00	88		00																					
GYEnor	Contrast control characteristic 3	38	SG.A	14,15, 16	2.2	2.8	3.3	V	Pin 33 =2.9 V							88		00																					
GYEmin	Contrast control characteristic 4	38	SG.A	14,15, 16	-	100	200	mV	Pin 33 =0.0 V							88		00																					
GYEclip	Contrast control characteristic 5	21,22, 23	SG.F	14,15, 16	0.50	0.65	0.80	V	Pin 24 =2.5 V						00	88		00																					
Lum nor	Brightness control characteristic 1	38	SG.D	14,15, 16	1.7	2.1	2.5	V	V_y = 0.0V							88		00																					
Lum max	Brightness control characteristic 2	38	SG.D	14,15, 16	2.3	3	-	V	V_y = 0.0V							88		00		FF																				
Lum min	Brightness control characteristic 3	38	SG.D	14,15, 16	-	1.3	2	V	V_y = 0.0V							88		00		00																				
D(R)1	R driving control characteristic 1	38	SG.A	14	2.0	4.0	6.0	dB								88		00		00	7F																	
D(B)1	B driving control characteristic 1	38	SG.A	16	2.0	4.0	6.0	dB								88		00		00		7F																
D(R)2	R driving control characteristic 2	38	SG.A	14	-5.0	-3.0	-1.0	dB								88		00		00	00																	
D(B)2	B driving control characteristic 3	38	SG.A	16	-5.0	-3.0	-1.0	dB								88		00		00		00																
EXD1(R)	Digital OSD (R) I/O characteristic 1	23,24, 38	SG.F, SG.A	14	1.0	1.5	2.0	V_{pp}	V_{osd} = 1.0V, SW23=ON							88		00																				
EXD1(G)	Digital OSD (G) I/O characteristic 1	22,24, 38	SG.F, SG.A	15	1.0	1.5	2.0	V_{pp}	V_{osd} = 1.0V, SW22=ON							88		00																				
EXD1(B)	Digital OSD (B) I/O characteristic 1	21,24, 38	SG.F, SG.A	16	1.0	1.5	2.0	V_{pp}	V_{osd} = 1.0V, SW21=ON							88		00																				
EXD2(R)	Digital OSD (R) I/O characteristic 2	23,24, 38	SG.F, SG.A	14	200	300	400	mV	Vosd = 1.0V, SW23=ON EXD2(R)=Measured value- EXD1(R)							88		00																20						
EXD2(G)	Digital OSD (G) I/O characteristic 2	22,24, 38	SG.F, SG.A	15	200	300	400	mV	Vosd = 1.0V, SW22=ON EXD2(G)=Measured value- EXD1(G)							88		00																20						
EXD2(B)	Digital OSD (B) I/O characteristic 2	21,24, 38	SG.F, SG.A	16	200	300	400	mV	Vosd = 1.0V, SW21=ON EXD2(B)=Measured value - EXD1(B)							88		00																20						
EXD1(R-G)	Digital OSD (R-G) amplitude difference	-	-	-	-350	0	350	mV								88																							
EXD1(G-B)	Digital OSD (G-B) amplitude difference	-	-	-	-350	0	350	mV								88																							
EXD1(B-R)	Digital OSD (B-R) amplitude difference	-	-	-	-350	0	350	mV								88																							
EXA(R)	Analog OSD (R) I/O characteristic	23,24, 38	SG.F, SG.A	14	1.2	2.1	3.0	V_{pp}	V_{osd} = 0.7V						40	88		00														10						
EXA(G)	Analog OSD (G) I/O characteristic	22,24, 38	SG.F, SG.A	15	1.2	2.1	3.0	V_{pp}	V_{osd} = 0.7V						40	88		00														10						
EXA(B)	Analog OSD (B) I/O characteristic	21,24, 38	SG.F, SG.A	16	1.2	2.1	3.0	V_{pp}	V_{osd} = 0.7V						40	88		00														10						

Symbol	Item	Input signal		Test point	Limits			Unit	Notes	Subaddress																															
		Pin	SG		Min.	Typ.	Max.			00H	01H	02H	03H	04H	05H	06H	07H	08H	09H	0AH	0BH	0CH	0DH	0EH	0FH	10H	11H	12H	13H	14H	15H	16H	17H	18H	19H	1AH	1BH	1CH
EXA(R-G)	Analog OSD (R-G) amplitude difference	–	–	–	-350	0	350	mV								88															10							
EXA(G-B)	Analog OSD (G-B) amplitude difference	–	–	–	-350	0	350	mV								88															10							
EXA(B-R)	Analog OSD (B-R) amplitude difference	–	–	–	-350	0	350	mV								88															10							
OFRG	Offset voltage (R-G)	38	SG.D	14,15	-100	0	100	mV	V_y = 0.0V							88		00																				
OFBG	Offset voltage (B-G)	38	SG.D	15,16	-100	0	100	mV	V_y = 0.0V							88		00																				
C(R)1	R cutoff control characteristic 1	38	SG. D	14	2.6	2.9	3.2	V	V_y = 0.0V							88		00					FF														
C(G)1	G cutoff control characteristic 1	38	SG. D	15	2.6	2.9	3.2	V	V_y = 0.0V							88		00						FF													
C(B)1	B cutoff control characteristic 1	38	SG. D	16	2.6	2.9	3.2	V	V_y = 0.0V							88		00							FF												
C(R)1	R cutoff control characteristic 2	38	SG. D	14	1.1	1.4	1.7	V	V_y = 0.0V							88		00					00														
C(G)1	G cutoff control characteristic 2	38	SG. D	15	1.1	1.4	1.7	V	V_y = 0.0V							88		00						00													
C(B)2	B cutoff control characteristic 2	38	SG. D	16	1.1	1.4	1.7	V	V_y = 0.0V							88		00							00												
Ccon 1	Color control characteristic 1	38	SG. C	14,15, 16	2	5	8	dB				80				88		7F																			
Ccon 2	Color control characteristic 2	38	SG. C	14,15, 16	-	-15	-10	dB				80				88		01																			
Ccon 3	Color control characteristic 3	38	SG. C	14,15, 16	-	-40	-35	dB				80				88		00																			
MTXRB	Matrix ratio R/B	38	SG.G	14,16	0.81	0.98	1.08	-								88																				
MTXGB	Matrix ratio G/B	38	SG.G	15,16	0.29	0.37	0.45	-								88																				
DOSD1	Digital OSD switching characteristic 1	23,24, 38	SG.F, SG.A	14	-	0.05	0.13	us	V_{osd} = 1.0V, SW23=ON						7F	88																				
DOSD2	Digital OSD switching characteristic 2	23,24, 38	SG.F, SG.A	14	-	0.05	0.13	us	V_{osd} = 1.0V, SW23=ON						7F	88																				
AOSD1	Analog OSD switching characteristic 1	23,24, 38	SG.F, SG.A	14	-	0.05	0.13	us	V_{osd} = 1.0V						7F	88																10						
AOSD2	Analog OSD switching characteristic 2	23,24, 38	SG.F, SG.A	14	-	0.05	0.13	us	V_{osd} = 1.0V						7F	88																10						
BB(R)	Blue background function (R)	38	SG.A	14	1.7	2.1	2.5	V								88		80																			
BB(G)	Blue background function (G)	38	SG.A	15	1.7	2.1	2.5	V								88		80																			
BB(B)	Blue background function (B)	38	SG.A	16	2.7	3.7	4.7	V								88		80																			
WB	White raster function	38	SG.A	14,15, 16	2.7	3.7	4.7	V								88										A0											

Symbol	Item	Input signal		Test point	Limits			Unit	Notes	Subaddress																															
		Pin	SG		Min.	Typ.	Max.			00H	01H	02H	03H	04H	05H	06H	07H	08H	09H	0AH	0BH	0CH	0DH	0EH	0FH	10H	11H	12H	13H	14H	15H	16H	17H	18H	19H	1AH	1BH	1CH
DEF	Deflection system typical conditions	-	-	-	-	-	-	-	Pin 28=5 V, pin 25=5 V, pin 24=0 V	40	adj	02	00	20	40	80	40	40	00	80	40	40	80	80	80	24	20	00	10	00	00	88	40	00	00	00	00	00
fH1	Horizontal free-running frequency 1	-	-	11	15.3	15.7	16.1	kHz																																
fH2	Horizontal free-running frequency 2	-	-	11	14.7	15.1	15.5	kHz																		20														
fH3	Horizontal free-running frequency 3	-	-	11	15.8	16.2	16.6	kHz																		26														
Hfree	Forced horizontal free-running operation	38	SG.A	11	15.3	15.7	16.1	kHz								88													90										
FPHU	Horizontal pull-in range (upper)	38	SG.H	11	250	500	-	Hz	Variable input frequency							88																							
FPHL	Horizontal pull-in range (lower)	38	SG.H	11	-	-500	-250	Hz	Variable input frequency							88																							
HPT1	Horizontal pulse timing 1	38	SG. A	11	12.0	13.5	15.0	µs								88																80	80						
HPT2	Horizontal pulse timing 2	38	SG. A	11	2.5	4.0	5.5	µs								88																80	9F						
HPTW	Horizontal pulse width	-	-	11	21	25	29	µs																															
VH	Horizontal pulse amplitude	-	-	11	4.7	5.4	-	V																															
HSTA	Horizontal pulse start operation	-	-	11	-	0.0	0.5	V																					00										
AFCG	AFC gain operation	38	SG.A	7	2.0	3.0	10.0	dB								88															80								
fV	Vertical free-running frequency	-	-	5	55	60	65	Hz																															
Vfree	Forced vertical free-running operation	38	SG.A	5	55	60	65	Hz								88										64													
SVC	Service mode operation	-	-	5	1.0	1.5	2	V																					18										
FPVU	Vertical pull-in frequency (upper)	38	SG.H	5	63	67	-	Hz	Variable input frequency							88																							
FPVL	Vertical pull-in frequency (lower)	38	SG.H	5	-	55	57	Hz	Variable input frequency							88																							
VRsi 1	Vertical ramp size	38	SG.A	5	1.6	2.0	2.4	Vpp								88																							
VRsc 1	Vertical ramp size control range 1	38	SG.A	5	2.0	2.4	2.8	Vpp								88											30											
VRsc 2	Vertical ramp size control range 2	38	SG.A	5	0.8	1.2	1.6	Vpp								88											00											
VRpo 1	Vertical ramp position control range 1	38	SG.A	5	18	38	58	µs								88																							
VRpo 2	Vertical ramp position control range 2	38	SG.A	5	840	860	880	µs	Measured value - VRpo 1							88													17											

Symbol	Item	Input signal		Test point	Limits			Unit	Notes	Subaddress																													
		Pin	SG		Min.	Typ.	Max.			00H	01H	02H	03H	04H	05H	06H	07H	08H	09H	0AH	0BH	0CH	0DH	0EH	0FH	10H	11H	12H	13H	14H	15H	16H	17H	18H	19H	1AH	1BH	1CH
VW	Vertical pulse width	38	SG.A	20	0.35	0.53	0.65	ms								88																							
VBLKW	Vertical blanking width	38	SG.A	14,15, 16	1.32	1.47	1.62	ms								88		00																					
VBLKW VS1	Vertical blanking width VSHIFT1	38	SG.A	14,15, 16	1.35	1.50	1.65	ms								88		00																					08
VBLKW VS2	Vertical blanking width VSHIFT2	38	SG.A	14,15, 16	1.73	1.88	2.03	ms								88		00																					0C
VBLKW VS3	Vertical blanking width VSHIFT3	38	SG.A	14,15, 16	2.11	2.26	2.41	ms								88		00																					0F
WVSS	Vertical blanking width	38	SG.I	5	14	-	-	us	Variable input signal duty							88																							
MONITORING	Intelligent monitor system typical conditions	-	-	-	-	-	-	-	Pin 28=5 V, pin 25=5 V, pin 24=0 V	40	adj	02	00	20	40	80	40	40	00	80	40	40	80	80	80	24	20	00	10	00	00	88	40	00	00	00	00	00
MONI1	Intelligent monitor 1 (composite sync)	41	SG.A	18	4.0	4.9	5.0	Vpp	Note: This LSI cannot operate correctly if MONI1 is used while the H-free bus bit (13H-D7) is set to 1.																			00											
MONI2	Intelligent monitor 2 (AFT)	63,64	SG.7	18	2.0	2.5	3.0	V																				10										
MONI3-1	Intelligent monitor 3-1 (RF AGC1)	-	-	18	4.0	4.3	4.6	V	At RF AGC voltage high																			20										
MONI3-2	Intelligent monitor 3-2 (RF AGC2)	63,64	SG.7	18	0.88	0.93	0.98	-	Pin 18 voltage/pin 59 voltage																			20										
MONI6	Intelligent monitor 6 (video SW output)	41	SG.A	18	0.76	0.95	1.24	Vpp																				50										
MONI7	Intelligent monitor 7 (G out)	41	SG.A	18	1.5	2.0	2.5	Vpp	Amplitude measured from blanking level									00										60										
MONI8	Intelligent monitor 8 (R out)	41	SG.A	18	1.5	2.0	2.5	Vpp	Amplitude measured from blanking level									00										70										
MONI9	Intelligent monitor 9 (B out)	41	SG.A	18	1.5	2.0	2.5	Vpp	Amplitude measured from blanking level									00										80										
MONI10	Intelligent monitor 10 (ACL)	-	-	18	3.5	4.0	4.5	V																				90										
MONI11	Intelligent monitor 11 (V sync)	41	SG.A	18	3.5	4.0	4.5	Vpp																				A0										
MONI12	Intelligent monitor 12 (H out)	41	SG.A	18	3.6	4.0	4.4	Vpp																				B0										
MONI13	Intelligent monitor 13 (VIF Vcc)	-	-	18	2.30	2.50	2.70	V																				C0										
MONI14	Intelligent monitor 14 (Start-up Vcc)	-	-	18	2.55	2.70	2.85	V																				D0										
MONI15	Intelligent monitor 15 (video/chroma Vcc)	-	-	18	2.30	2.50	2.70	V																				E0										
MONI16	Intelligent monitor 16 (Hi Vcc)	-	-	18	2.55	2.70	2.85	V																				F0										
MONI1-C	Intelligent monitor I-C (Sync ratio at H free mode)	41	SG.A	18	50	100	-	%	Input SYNC ratio measured at H free mode																			00	90										

Method of Measurement of Electrical Characteristics

VIF block

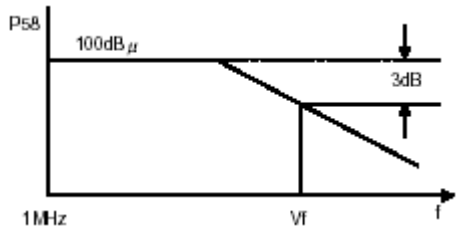
- P/N: Video S/N

1. Input SG3, and measure the rms value (noise value) for the signal output from pin 58.
2. The P/N is defined as follows.

$$P/N = 20 \log \frac{V_0 \text{ measured value (Vp-p)} \times 10^3 \times 0.7}{\text{Noise measured value (mVrms)}} \quad \text{(dB)}$$

- Vf: Video frequency characteristic

1. Input SG4, and adjust the f_2 frequency so that the 1 MHz beat component is output to pin 58.
2. Adjust the voltage applied to pin 62 so that the 1 MHz beat component at pin 62 is 100 dBμ.
3. Gradually reduce the f_2 frequency, and measure the frequency at which the beat component is 3 dB lower than the level at 1 MHz.



- Vin min: Input sensitivity

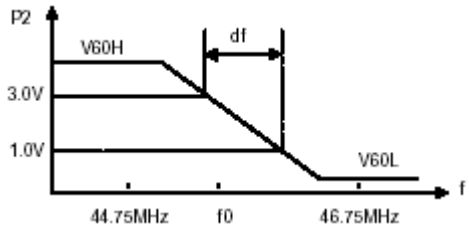
1. Lower the level of SG5 so that the input level is 3 dB lower than the value measured under video-detection-wave output" for the V_0 item.

- Vin max: Maximum allowable input

1. Input SG6 at 90 dBμ.
2. The output level of Pin 58 at this point should be V_A. Increase the amplitude of SG6 so that the input level indicates an output level for Pin 58 that is 3 dB lower than V_A.

- μAFT: AFT detection sensitivity

V2H: AFT maximum voltage
V2L: AFT minimum voltage



μAFT is defined as follows.

$$\mu AFT = \frac{(3.0 - 10.) \times 10^3 \text{ mV}}{\text{df KHz}} \quad \text{(mV/KHz)}$$

- IM: Inter-modulation

1. Input SG13 to Pins 63 and 64.
2. Measure the 0.92 MHz component and 3.58 MHz component of the pin 58 output.
3. IM is defined as follows.

$$IM = 20 \log \frac{\text{0.92 MHz component}}{\text{3.58 MHz component}} \quad (dB)$$

- DLPH: RF AGC delay maximum point
- DLPL: RF AGC delay minimum point

1. Input SG5 to pins 63 and 64.
2. Change the amplitude of SG5 and measure the level at which the voltage of pin 59 is 2.5 V.

SIF block

- LIM: Input limiting sensitivity
  Gradually decrease the input level of SG17, and measure the input level at the point when the 400 Hz component of Pin 58 is 3 dB lower than VoAF.

- AMR: AMR

1. Measure the 400 Hz component for Pin 54 and set it as Vam.
2. AMR is defined as follows.

$$AMR = 20 \log \frac{\text{VoAF (mVrms)}}{\text{Vam (mVrms)}} \quad (dB)$$

- AFSN: AF S/N

1. Measure the noise (20 Hz to 100 kHz) of the Pin 51 output.
2. AF S/N is defined as follows.

$$AF\ S/N = 20 \log \frac{\text{VoAF max}}{\text{Measured value}} \quad (dB)$$

Video clock

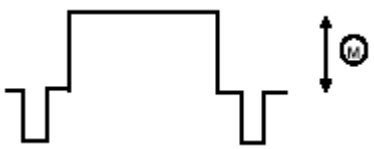
- 2AGTV: Video SW output level (TV input)
- 2AGEV: Video SW output level (External input)

1. Input SG.A to pin 41 (2AGTV) or pin 38 (2AGEV).
2. The amplitude (p-p) at pin 31 is measured.

*In order to select TV or external input, use the subaddress 06H.

- Ymax: Maximum video output

1. Input SG.A to pin 38.
2. Measure the amplitude (p-p) other than the blanking part of the output of pins 14, 15, 16.



- FBY: Video frequency characteristic

1. Input SG.B (5 MHz, 0.4 Vp-p) to pin 38.
2. Measure the amplitude (p-p) other than the blanking part of the output of pins 14, 15, 16, take the result to be YB.
3. FYB is defined as follows.

$$FYB = 20 \log \frac{YB\ (Vp\text{-}p)}{GY\ (Vp\text{-}p)}\ (dB)$$

- CRF1: Chroma trap attenuation 1 (normal R/G/B output)

TRF maximum chroma trap attenuation

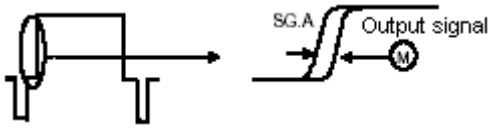
1. Input SG.C to pin 38, measure the 3.58 MHz frequency level with TRAP ON/OFF (02H D4) DATA 1, take this to be N_0.
2. Also measure the level with TRAP ON/OFF (02H D4) DATA 0.
3. CRF1 is defined as follows.

$$CRF1 = 20 \log \frac{\text{Measured value (mVp-p)}}{N_0\ (mVp\text{-}p)}\ (dB)$$

4. Take the minimum value of CRF1 when the I^2C BUS data of the TRAP fine ADJ (12H D0/D1) is adjusted to be TRF.

- YDL1: YDL time 1

1. Input SG.A to pin 38.
2. Measure the delay time relative to the input signal of pins 14, 15, 16.



The delay time at 50% rise level is measured.

- YDL2, 3, 4: YDL time 2, 3, 4

1. Input SG.A to pin 38.
2. Measure the delay time of the input signal and the pin 14, 15, 16 output signals.
3. YDL2, YDL3, YDL4 are defined as follows.

YDL2 = measured value (ns) - YDL1 (measured value)

YDL3 = measured value (ns) - YDL2 (measured value)

YDL4 = measured value (ns) - YDL3 (measured value)

- GTmax: Video tone control characteristic 2

1. Input SG.B (f = 2.5 MHz) to pin 38.
2. The output amplitude of pins 14, 15, 16 when the video tone data is at the center (20 H) is taken to be GTnor.
3. The output amplitude of pins 14, 15, 16 when the video tone data is maximum is measured.
4. GTmax is defined as follows.

$$GTmax = 20 \log \frac{\text{Measured value (Vp-p)}}{GTnor\ (mVp\text{-}p)}\ (dB)$$

- GTmin: video tone control characteristic 3

1. Input SG.B (f=2.5 MHz) to pin 38.
2. The output amplitude of pins 14, 15, 16 when the video tone data is at the center (20 H) is taken to be GTnor.
3. The output amplitude of pins 14, 15, 16 when the video tone data is minimum is measured.
4. GTmin is defined as follows.

$$GTmin = 20 \log \frac{\text{Measured value (Vp-p)}}{\text{GTnor (mVp-p)}} \quad \text{(dB)}$$

- GT2M: Video tone control characteristic 4

1. Take pin 14, 15, 16 output amplitude when input signal frequency is 2.5 MHz to be GTnor.
2. Input SG.B (f = 2 MHz) to pin 38.
3. Measure pin 14, 15, 16 output amplitude.
4. GT2M is defined as follows.

$$GT2M = 20 \log \frac{\text{Measured value (Vp-p)}}{\text{GTnor (mVp-p)}} \quad \text{(dB)}$$

- GT5M: Video tone control characteristic 5

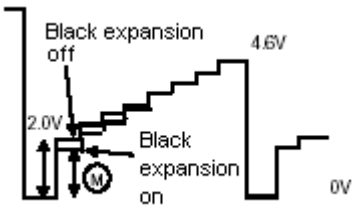
1. Take pin 14, 15, 16 output amplitude when input signal frequency is 2.5 MHz to be GTnor.
2. Input SG.B (f = 2 MHz) to pin 38.
3. Measure pin 14, 15, 16 output amplitude.
4. GT5M is defined as follows.

$$GT5M = 20 \log \frac{\text{Measured value (Vp-p)}}{\text{GTnor (mVp-p)}} \quad \text{(dB)}$$

- BLS: black stretch characteristic

1. Input SG.K to pin 38.
2. With black stretch off (02H D1 = 1), adjust the contrast (05H) and brightness (0AH), and set the pin 14, 15, 16 output level of the first stage (lowest stage) to 2.0 V, and the output level of the eighth stage (highest stage) to 4.6 V.
3. Change black stretch to on (02H D1 = 0), and measure the pin 14, 15, 16 first stage output level.
4. BLS is defined as follows.

   BLS = 2.0 - measured value (V)



- VMF: Video mute function

1. Input SG.A to pin 38.
2. With the mute switch (02H D7) on "VMFon", off "VMFoff", measure the output amplitude.
3. VMF is defined as follows.

$$VMF = 20 \log \frac{\text{VMFon (Vp-p)}}{\text{VMFoff (Vp-p)}} \quad \text{(dB)}$$

Chroma block

- CnorR: Chroma typical output (R-Y)
- CnorB: Chroma typical output (B-Y)

1. Input SG.C to pin 38.
2. When "test mode" I^2C data is 18H D6=1, 18H D7=1 and 19H D6=1 and when "test mode" I^2C data is 18H D6=0, 18H D7=1 and 19H D6=1, take the pin 59 output amplitude to be the chroma typical output (R-Y) and chroma typical output (B-Y), respectively.

- ACC1: ACC characteristic 1

1. Input SG.E (eb=570 mV: level + 6 dB) to pin 38.
2. Measure the pin 59 output amplitude.
3. ACC1 is defined as follows.

$$ACC1 = 20 \log \frac{\text{measured value (mVp-p)}}{\text{chroma typical output 1 (mVp-p)}} \quad \text{(dB)}$$

- ACC2: ACC characteristic 2

1. Input SG.E (input level: -18 dB) to pin 38.
2. Measure the pin 59 output amplitude.
3. ACC2 is defined as follows.

$$ACC2 = 20 \log \frac{\text{measured value (mVp-p)}}{\text{chroma typical output 1 (mVp-p)}} \quad \text{(dB)}$$

- OV: Chroma overload characteristic

1. Input SG.E (eb=800 mVp-p) to pin 38.
2. Measure the pin 59 output amplitude.
3. OV is defined as follows.

$$OV = 20 \log \frac{\text{measured value (mVp-p)}}{\text{chroma typical output 1 (mVp-p)}} \quad \text{(dB)}$$

- VikN: Killer operation input level

1. Input SG.E (variable level) at input level 0 dB to pin 38.
2. While monitoring the pin 59 output amplitude, lower the input level, and measure the input level when the output amplitude vanishes.

- KillP: Hue remaining with killer

1. Input SG.E (level: -40 dB) to pin 38.
2. Measure the pin 59 output amplitude.

- APCU: APC pull-in range (upper)
- APCL: APC pull-in range (lower)

1. Input SG.E (feb-fec-3.579545 MHz) to pin 38.
2. After raising the frequency until the output from pin 59 vanishes, lower the frequency, and take the point at which an output appears to be fu.
3. After lowering the frequency until the output from pin 59 vanishes, raise the frequency, and take the point at which an output appears to be fl.
4. APCU and APCL are defined as follows.

$$APCU = fu - 3579545 \text{ Hz}$$

$$APCL = fl - 3579545 \text{ Hz}$$

- R/BN: Demodulation ratio R-Y/B-Y

1. Input SG.E (eb = single chroma = ec + 50 kHz) to pin 38.
2. Take the pin 59 output amplitude when "test mode" I^2C data is 18H D6=1, D7=1 to be VRY.
3. Take the pin 59 output amplitude when "test mode" I^2C data is 18H D6=0, D7=1 to be VBY.
4. R/BN is defined as follows.

$$R/BN = \frac{VRY\ (mVp\text{-}p)}{VBY\ (Vp\text{-}p)} \quad (dB)$$

- R/BU, G/BU: Demodulation ratio
- R/BJ, G/BJ: Demodulation ratio

1. Input SG.J to pin 38.
2. Take the pins 14, 15, 16 output amplitude when video mute on (02H D7 = 1, D7 = 1) and US mode (15H D3 = 1) are specified to be URY, UGY, and UBY, respectively.
3. Take the pins 14, 15, 16 output amplitude when video mute on (02H D7 = 1, D7 = 1) and JPN mode (15H D1 = 1, D2=1) are specified to be JRY, JGY, and JBY, respectively.
4. R/BU, G/BU, R/BJ, and G/BJ are defined as follows.

$$R/BU = \frac{URY(Vp\text{-}p)}{UBY(Vp\text{-}p)} \qquad G/BU = \frac{UGY(Vp\text{-}p)}{UBY(Vp\text{-}p)}$$

$$R/BJ = \frac{JRY(Vp\text{-}p)}{JBY(Vp\text{-}p)} \qquad G/BJ = \frac{JGY(Vp\text{-}p)}{JBY(Vp\text{-}p)}$$

- R-YN: Demodulation angle

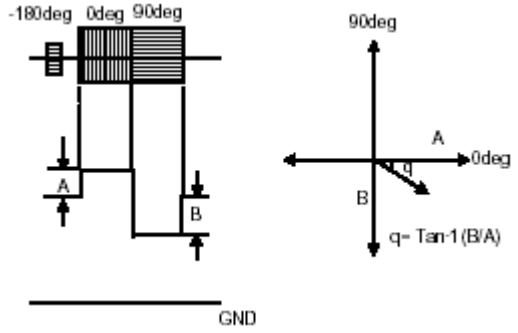
1. Input SG.E (eb = single chroma = ec + 5 kHz) to pin 38.
2. Take the pin 59 output amplitude when "test mode" I^2C data is 18H D6=1, D7=1 to be VRY.
3. Take the pin 59 output amplitude when "test mode" I^2C data is 18H D6=0, D7=1 to be VBY.
4. R/YN is defined as follows.

$$R\text{-}YN = \mathrm{Tan}^{-1}\ \frac{VRY \times 3.8}{(VBY \times 1.9) + 45}(deg)$$

*The vector is determined taking the demodulator gain into account.

- TC1: TINT control characteristic 1
- TC2: TINT control characteristic 2

1. Input SG.C (see figure below) to pin 38. Measure the absolute angle with reference to the pin 59 output voltage, referring to the figure below.



2. Take the TINT data center part (07H data 40H) to be reference angle "TC", determine the TINT DATA maximum and minimum values. TC1 and TC2 are defined as follows.

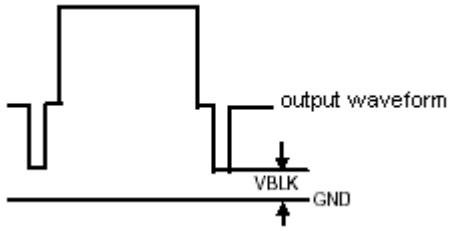
TC = TCmax – TC(deg)

TC = TC – TCmin (deg)

RGB interface block

- VBKL: Output blanking voltage

1. Input SG.A to pin 38.
2. Measure the voltage of the pin 14, 15, 16 pedestal and blanking parts.



- GYmax: Contrast control characteristic 1
- GYmin: Contrast control characteristic 2

1. Input SG.B (f=100 kHz) to pin 38.
2. Measure the pin 14, 15, 16 output amplitude.

- GYEnor: Contrast control characteristic 3
- GYEmin: Contrast control characteristic 4

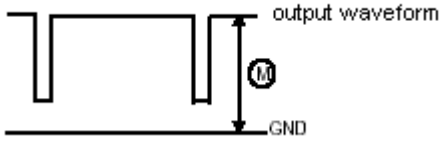
1. Input SG.A to pin 38.
2. Measure the pin 14, 15, 16 output amplitude when applying 2.9 V and 0 V to pin 33.

- GYEclip: Contrast control characteristic 5

1. Input SG.F to pins 21, 22, 23, 24.
2. Minimize the contrast control data, and measure the output amplitude at and above the pedestal part of pins 14, 15, 16.
   The amplitude of the blanking part is not measured.

- Lum nor: Brightness control characteristic 1
- Lum max: Brightness control characteristic 2
- Lum min: Brightness control characteristic 3

1. Input SG.D (Vy=0 V) to pin 38.
2. Measure the DC voltage other than the blanking part of the output of pins 14, 15, 16.



- D(R)1: R drive control characteristic 1

1. Input SG.A to pin 38.
2. Measure the pin 14 output amplitude when the drive control data is at center and is maximum, take the results to be DRnor and DRmax respectively.
3. D(R)1 is defined as follows.

$$D(R)1 = 20 \log \frac{DRmax\ (Vp\text{-}p)}{DRnor\ (Vp\text{-}p)} (dB)$$

- D(B)1: B drive control characteristic 1

1. Input SG.A to pin 38.
2. Measure the pin 16 output amplitude when the drive control data is at center and is maximum, take the results to be DBnor and DBmax respectively.
3. D(B)1 is defined as follows.

$$D(B)1 = 20 \log \frac{DBmax\ (Vp\text{-}p)}{DBnor\ (Vp\text{-}p)} (dB)$$

- D(R)2: R drive control characteristic 2

1. Input SG.A to pin 38.
2. Measure the pin 14 output amplitude when the drive control data is at center and is minimum, take the results to be DRnor and DRmin respectively.
3. D(R)2 is defined as follows.

$$D(R)2 = 20 \log \frac{DRmin\ (Vp\text{-}p)}{DRnor\ (Vp\text{-}p)} (dB)$$

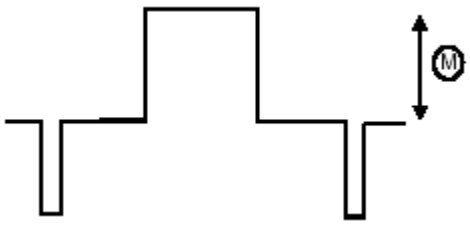
- D(B)2: R drive control characteristic 2

1. Input SG.A to pin 38.
2. Measure the pin 16 output amplitude when the drive control data is at center and is minimum, take the results to be DBnor and DBmin respectively.
3. D(B)2 is defined as follows.

$$D(B)2 = 20 \log \frac{DBmin\ (Vp\text{-}p)}{DBnor\ (Vp\text{-}p)} (dB)$$

- EXD(R): Digital OSD(R) input/output characteristic
- EXD(G): Digital OSD(G) input/output characteristic
- EXD(B): Digital OSD(B) input/output characteristic

1. Input SG.F (Vosd=1.0 V) to pins 21, 22, 23, 14.
2. Measure the output amplitude at and above the pedestal part in pins 14, 15, 16. The amplitude of the blanking part is not measured.



- EXD(R-G): Digital OSD (R-G) amplitude difference
- EXD(G-B): Digital OSD (G-B) amplitude difference
- EXD(B-R): Digital OSD (B-R) amplitude difference

1. EXD(R-G), EXD(G-B) and EXD(B-R) are defined as follows.

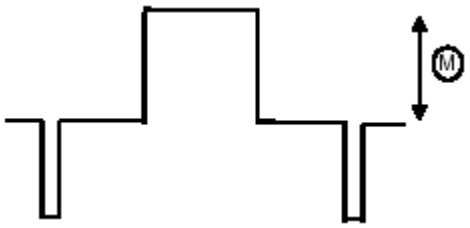
$$EXD(R–G) = EXD(R)–EXD(G)$$

$$EXD(G–B) = EXD(G)–EXD(B)$$

$$EXD(B–R) = EXD(B)–EXD(R)$$

- EXA(R): Analog OSD(R) input/output characteristic
- EXA(G): Analog OSD(G) input/output characteristic
- EXA(B): Analog OSD(B) input/output characteristic

1. Input SG.F (Vosd=1.0 V) to pins 21, 22, 23, 14.
2. Measure the output amplitude at and above the pedestal part in pins 14, 15, 16. The amplitude of the blanking part is not measured.



- EXA(R-G): Analog OSD (R-G) amplitude difference
- EXA(G-B): Analog OSD (G-B) amplitude difference
- EXA(B-R): Analog OSD (B-R) amplitude difference

1. EXA(R-G), EXA(G-B) and EXA(B-R) are defined as follows.

EXA(R–G) = EXA(R)–EXA(G)

EXA(G–B) = EXA(G)–EXA(B)

EXA(B–R) = EXA(B)–EXA(R)

- C(R)1: R cutoff characteristic 1
- C(G)1: G cutoff characteristic 1
- C(B)1: B cutoff characteristic 1
- C(R)2: R cutoff characteristic 2
- C(G)2: G cutoff characteristic 2
- C(B)2: B cutoff characteristic 2

1. Input SG.D (Vy=0 V) to pin 38.
2. Measure the DC voltage of other than the blanking part in the outputs of pins 14, 15, 16.

- Ccon1: color control characteristic 1
- Ccon2: color control characteristic 2
- Ccon3: color control characteristic 3

1. Input SG.C to pin 38.
2. Measure the output amplitudes of pins 14, 15, 16 when IIC DATA 08H=40h, take this to be Ccon0.
3. Measure the output amplitudes of pins 14, 15, 16 under each set of conditions.
4. Ccon1, Ccon2, Ccon3 are defined as follows.

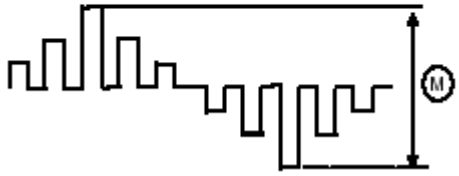
$$\text{Ccon1, Ccon2, Ccon3} = 20 \log \frac{\text{measured value (Vp-p)}}{\text{Ccon0 (Vp-p)}} \quad \text{(dB)}$$

- MTXRB: Matrix ratio R/B
- MTXGB: Matrix ratio G/B

1. Input SG.G (rainbow color bar) to pin 38.
2. Measure the output amplitude when pins 14, 15, 16 are respectively VR, VG, VB.
3. MTXRB, MTXGB are defined as follows.

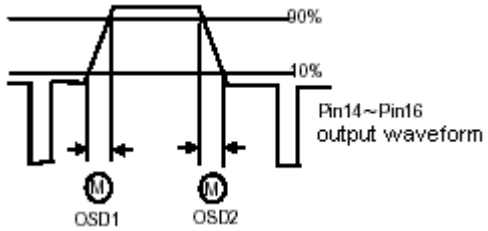
$$MTXRB = \frac{VR\ (Vp\text{-}p)}{VB\ (Vp\text{-}p)}$$

$$MTXGB = \frac{VG\ (Vp\text{-}p)}{VB\ (Vp\text{-}p)}$$



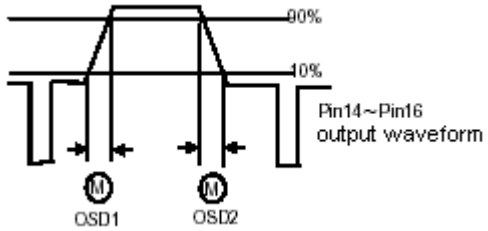
- DOSD1: Digital OSD switching characteristic 1
- DOSD2: Digital OSD switching characteristic 2

1. Input SG.F (Vosd=1.0 V) to pins 21, 22, 23, 24.
2. Measure the rise time and fall time of the output signals of pins 14, 15, 16 at and above pedestal level. The blanking part is not measured.



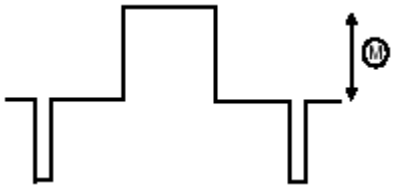
- AOSD1: Analog OSD switching characteristic 1
- AOSD2: Analog OSD switching characteristic 2

1. Input SG.F (Vosd=1.0 V) to pins 21, 22, 23, 24.
2. Measure the rise time and fall time of the output signals of pins 14, 15, 16 at and above pedestal level. The blanking part is not measured.



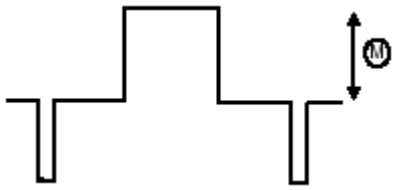
- BB(R): Blue back function (R)
- BB(G): Blue back function (G)
- BB(B): Blue back function (B)

1. Input SG.A to pin 38.
2. Measure the output amplitude (p-p) of pins 14, 15, 16 other than the blanking part.



- WB: White raster function

1. Input SG.A to pin 38.
2. Measure the output amplitude (p-p) of pins 14, 15, 16 other than the blanking part.



Deflection block

- fH1: Horizontal free-running frequency 1
- fH2: Horizontal free-running frequency 2
- fH3: Horizontal free-running frequency 3

Measure the frequency of pin 11 with no input.

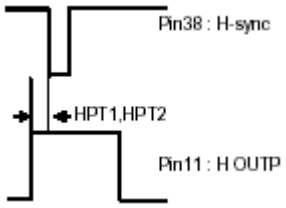
- Hfree: Forced horizontal free-running operation

1. Input SG.A to pin 38.
2. Set H-FREE CONTROL DATA to on, measure the frequency at pin 11.

- FPHU: Horizontal pull-in range (upper)
- FPHL: Horizontal pull-in range (lower)

1. Input SG.H to pin 38.
2. Change the frequency of SG.H, measure the frequency range for which the pin 11 output signal and pin 38 input signal are pulled in, with respect to the video signal horizontal frequency.

- HPT1: Horizontal pulse timing 1

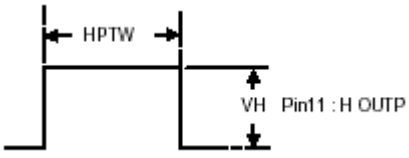


- HPT2: Horizontal pulse timing 2

1. Measure the horizontal pulse timing using the method for HPT1.
2. Typical

HPT2 = (measured value) - HPT1

- HPTW: Horizontal pulse width
- VH: Horizontal pulse amplitude



- HSTA: Horizontal pulse stop operation

Confirm that when H.START SW OFF (0FH:D7=0), the horizontal output goes low.

- AFCG: AFC gain operation

1. Measure the pin 7 output amplitude during AFC switching, taking the result during SW ON to be AFCon, and during SW OFF to be AFCoff.
2. AFCG is defined as follows.

$$AFCG = 20 \log \frac{AFCon\ (Vp\text{-}p)}{AFCoff\ (Vp\text{-}p)}\ (dB)$$

- fV: Vertical free-running frequency

Measure the pin 5 output frequency with no input.

- Vfree: Forced vertical free-running operation

1. Input SG.A to pin 38.
2. Set V-FREE CONTROL DATA to on, measure the pin 5 output amplitude.

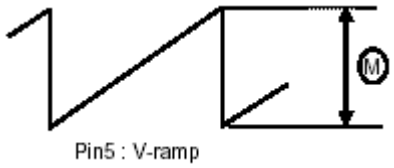
- SCV: Service mode operation

Measure the pin 5 output DC voltage with the service switch on.

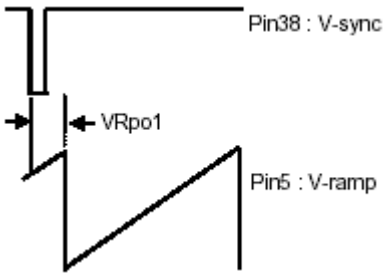
- FPVU: Vertical pull-in frequency (upper)
- FVPL: Vertical pull-in frequency (lower)

Change the SG.H vertical frequency, and measure the frequency when the pin 5 output waveform is pulled in.

- VRsi: Vertical ramp size
- VRsc1: Vertical ramp size control range 1
- VRsc2: Vertical ramp size control range 2



- VRpo1: Vertical ramp position control range 1

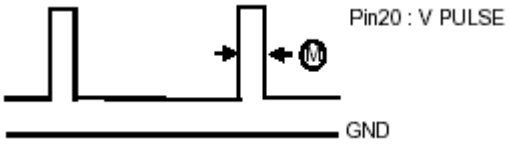


- VRpo2: Vertical ramp position control range 2

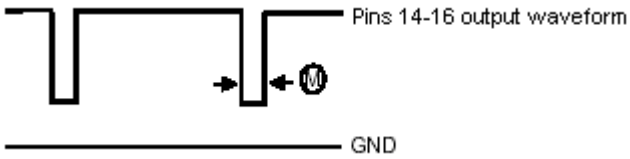
1. Measure the vertical ramp timing using the same method as for VRpo1.
2. VRpo2 is defined as follows.

VRpo2 = (measured value) –VRpo1

- VW: Vertical pulse width



- VBLKW: Vertical BLK width



- WVSS: Minimum width at minimum sync operation

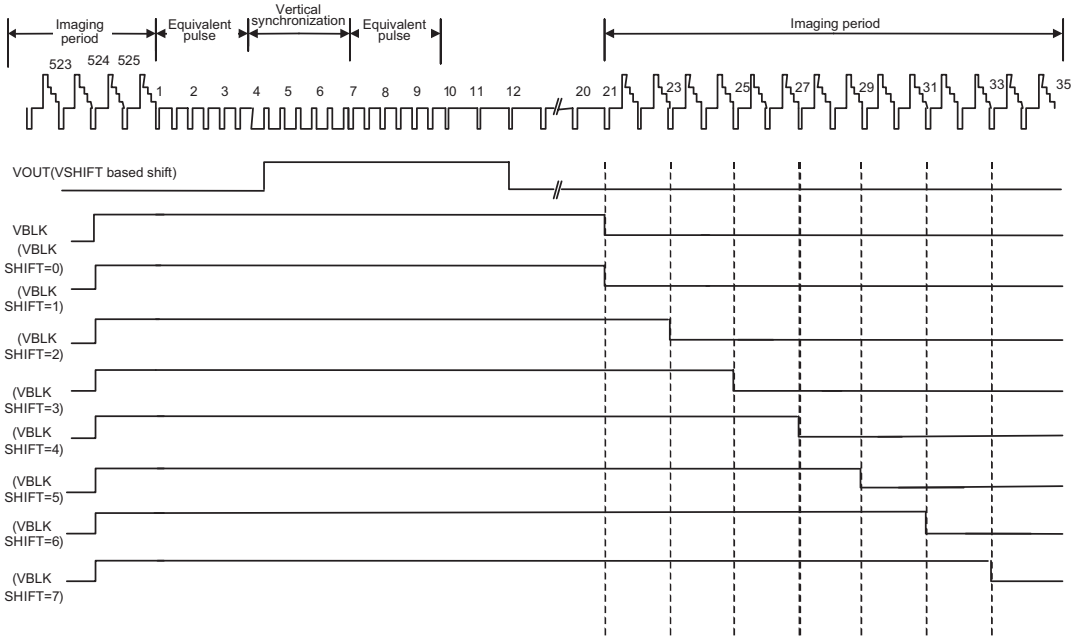
Reduce the width of the SG.I signal, and measure the input signal width when the pin 5 output waveform pull-in is lost.

The following function is added to the M61250BFP (VBLKWVS1 to VBLKWVS3)

The vertical blanking width can be specified independently of VSHIFT.
Note, however, that it operates in the same way as conventional products in the initial state.

The following bits are added to the I^2C register.

- VBLK SHIFT ON (1CH D3) Initial value = 0
  - 0: Shifts the VBLK based on the conventional SHIFT
  - 1: Shifts the VBLK based on the VBLK SHIFT.
- VBLK SHIFT (1CH D2 to 1CH D0) Initial value = 4
  - 0: VBLK period is 260 H to 21 H.
  - 1: VBLK period is 260 H to 21 H.
  - 2: VBLK period is 260 H to 23 H.
  - 3: VBLK period is 260 H to 25 H.
  - 4: VBLK period is 260 H to 27 H.
  - 5: VBLK period is 260 H to 29 H.
  - 6: VBLK period is 260 H to 31 H.
  - 7: VBLK period is 260 H to 33 H.

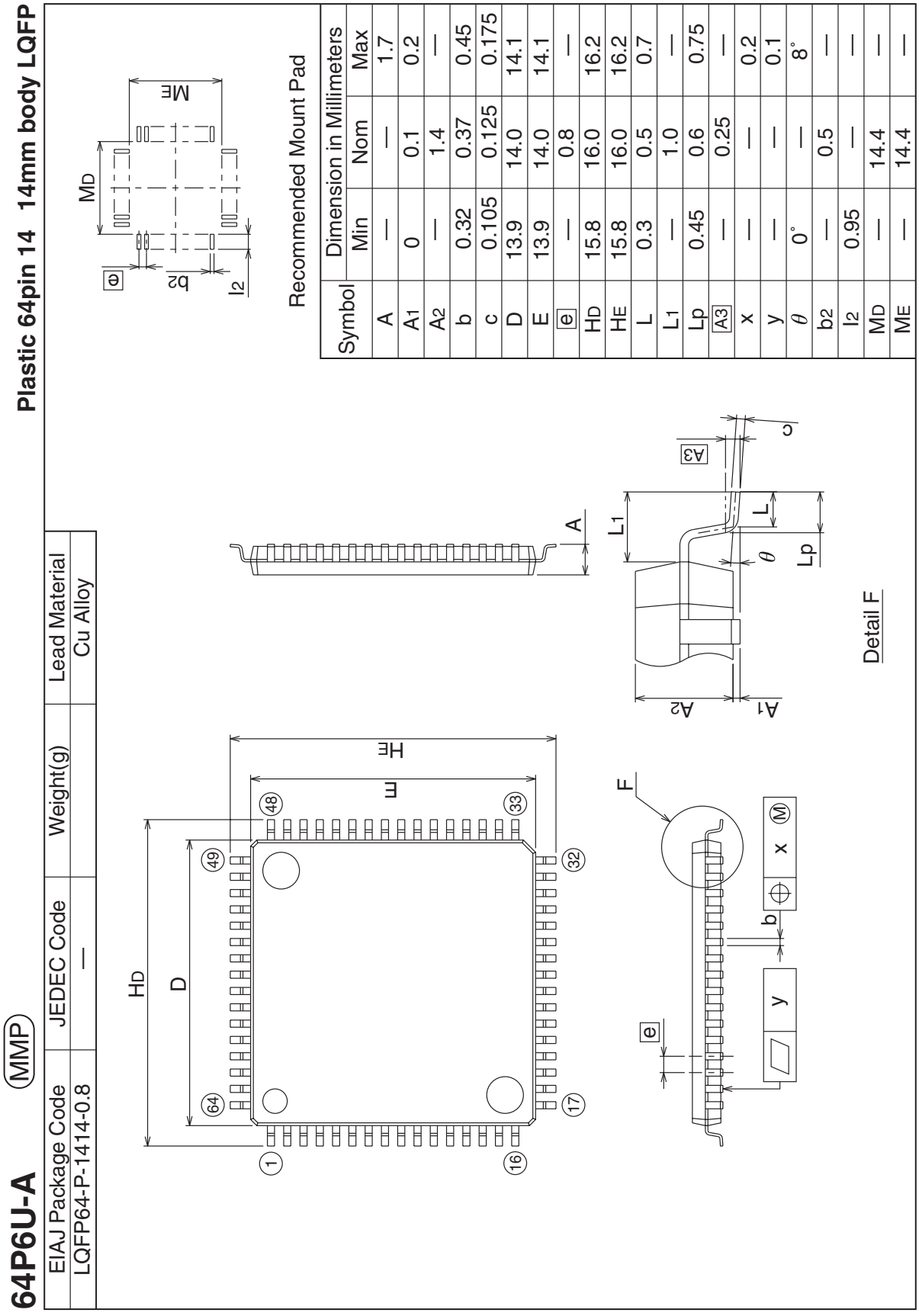


- An image may be output during the V blanking period according to the VSHIFT value.
  In this case, the VBLK should be shifted in order not to output the image during the blanking period. Carefully consider this because the output condition changes according to the circuit connected externally.

Important Information

- Each application should be thoroughly studied and evaluated before making a decision.
- 47 mF and higher electrolytic capacitors and 0.01 mF and higher ceramic capacitors should be connected in parallel between each of the power supply pins (3, 4, 12, 39, 42, 44) and ground pin. In addition, it is recommended that the connectors be made as close to the IC power supply pins as possible.
- The C-SYNC output operation of the intelligent monitor (18 pins) cannot be guaranteed at Hfree (13H: D7 = 1) .
- When purchasing I2C bus components, a license to use these components within a 12C bus system is provided under the 12C patent rights of Philips Corp.
  However, the bus system must conform to the 12C specifications stipulated by Philips.

Package Dimensions



Symbol	Dimension in Millimeters		
	Min	Nom	Max
A	—	—	1.7
A_1	0	0.1	0.2
A_2	—	1.4	—
b	0.32	0.37	0.45
c	0.105	0.125	0.175
D	13.9	14.0	14.1
E	13.9	14.0	14.1
e	—	0.8	—
H_D	15.8	16.0	16.2
H_E	15.8	16.0	16.2
L	0.3	0.5	0.7
L_1	—	1.0	—
Lp	0.45	0.6	0.75
A3	—	0.25	—
x	—	—	0.2
y	—	—	0.1
θ	0°	—	8°
b_2	—	0.5	—
l_2	0.95	—	—
M_D	—	14.4	—
M_E	—	14.4	—

Renesas Technology Corp. Sales Strategic Planning Div. Nippon Bldg., 2-6-2, Ohte-machi, Chiyoda-ku, Tokyo 100-0004, Japan

RENESAS SALES OFFICES

http://www.renesas.com

Renesas Technology America, Inc.
450 Holger Way, San Jose, CA 95134-1368, U.S.A
Tel: <1> (408) 382-7500 Fax: <1> (408) 382-7501

Renesas Technology Europe Limited.
Dukes Meadow, Millboard Road, Bourne End, Buckinghamshire, SL8 5FH, United Kingdom
Tel: <44> (1628) 585 100, Fax: <44> (1628) 585 900

Renesas Technology Europe GmbH
Dornacher Str. 3, D-85622 Feldkirchen, Germany
Tel: <49> (89) 380 70 0, Fax: <49> (89) 929 30 11

Renesas Technology Hong Kong Ltd.
7/F., North Tower, World Finance Centre, Harbour City, Canton Road, Hong Kong
Tel: <852> 2265-6688, Fax: <852> 2375-6836

Renesas Technology Taiwan Co., Ltd.
FL 10, #99, Fu-Hsing N. Rd., Taipei, Taiwan
Tel: <886> (2) 2715-2888, Fax: <886> (2) 2713-2999

Renesas Technology (Shanghai) Co., Ltd.
26/F., Ruijin Building, No.205 Maoming Road (S), Shanghai 200020, China
Tel: <86> (21) 6472-1001, Fax: <86> (21) 6415-2952

Renesas Technology Singapore Pte. Ltd.
1, Harbour Front Avenue, #06-10, Keppel Bay Tower, Singapore 098632
Tel: <65> 6213-0200, Fax: <65> 6278-8001

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