microelectronics group

Lucent Technologies
Bell Labs Innovations

W7020 *Bluetooth** Radio Module

Features

- Complete *Bluetooth* RF solution

- Compliant with *Bluetooth* specification version 1.0

- Highly integrated module including an RF transceiver IC, antenna filter, and transmit/receive baluns

- 0 dBm output power at 50 Ω

- 2.7 V operation enabling long battery life

- 3.2 kHz low-power idle-mode clock

- Digital receive signal strength indicator (RSSI)

- Small-outline module ceramic land grid array (MCLGA) package (9.7 x 14.0 x 1.6 mm)

Applications

- Cellular phones
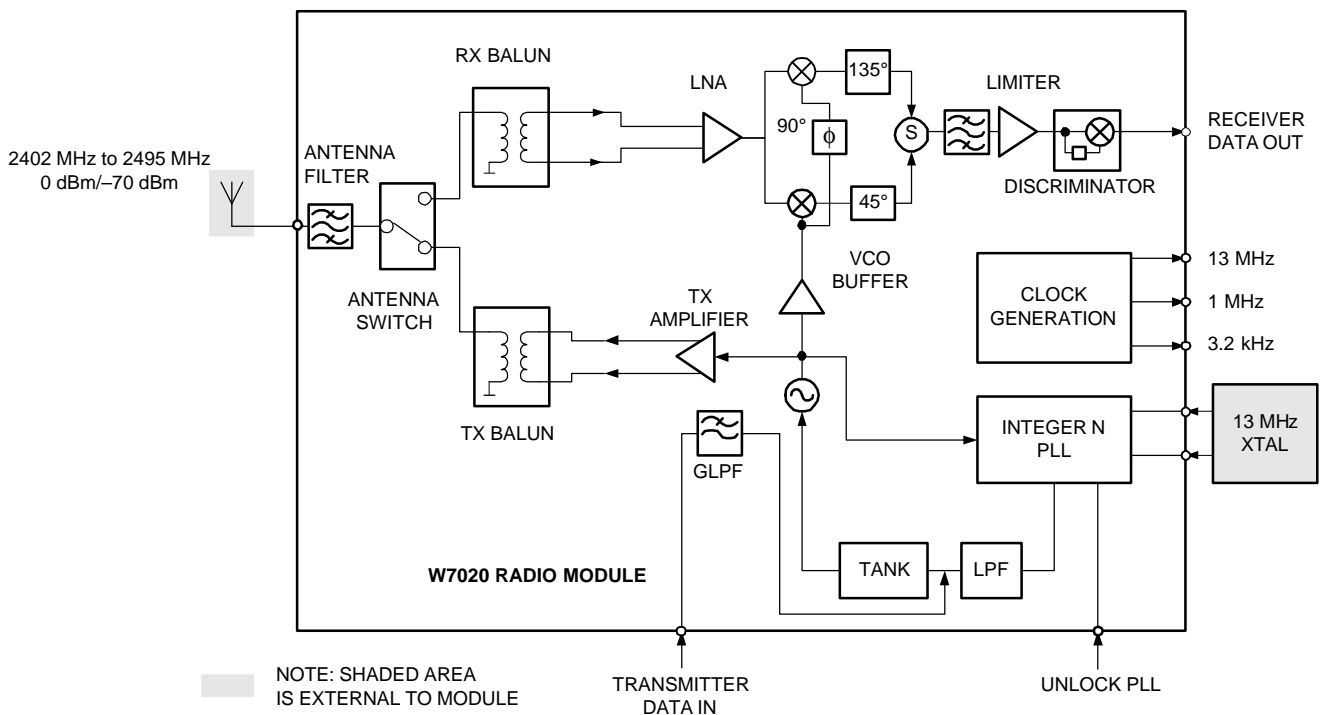
- PCs and peripherals

- PDAs

- Consumer appliances

Figure 1. Circuit Block Diagram

*Bluetooth is a trademark of Telefonaktiebolaget LM Ericsson.

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Description

The W7020 *Bluetooth* radio module is a short-range microwave-frequency radio transceiver for *Bluetooth* links. It operates in the globally available 2.4 GHz to 2.5 GHz ISM free band. The radio is based on a bipolar complementary metal-oxide semiconductor (BiCMOS) RFIC. The antenna filter and the RX and TX baluns are all integrated into the radio module.

As illustrated in Figure 2, the radio module requires only a baseband controller, an external antenna connected through a 50 Ω characteristic impedance line, and a 13 MHz crystal or reference clock signal. It is controlled by the digital baseband circuit through the serial interface bus and separate strobe signals. The TX and RX data pins also connect to the baseband with a maximum bit rate of 1 Mbit/s. The power supply is partitioned into two paths, one for the VCO circuit and one for all other module supply connections. Each of the supplies should be externally low-frequency decoupled.

Fast-frequency hopping (FFH) of 1600 hops/s is used with a channel spacing of 1 MHz so that the radio link is less sensitive to signal fading due to multipath; therefore, antenna diversity is not required. The modulation is Gaussian frequency shift keying (GFSK) with a BT product of 0.5. The channel bandwidth is 1 MHz and the modulation index is between 0.28 and 0.35. A binary one is indicated by a positive frequency deviation, and a binary zero is indicated by a negative frequency deviation.
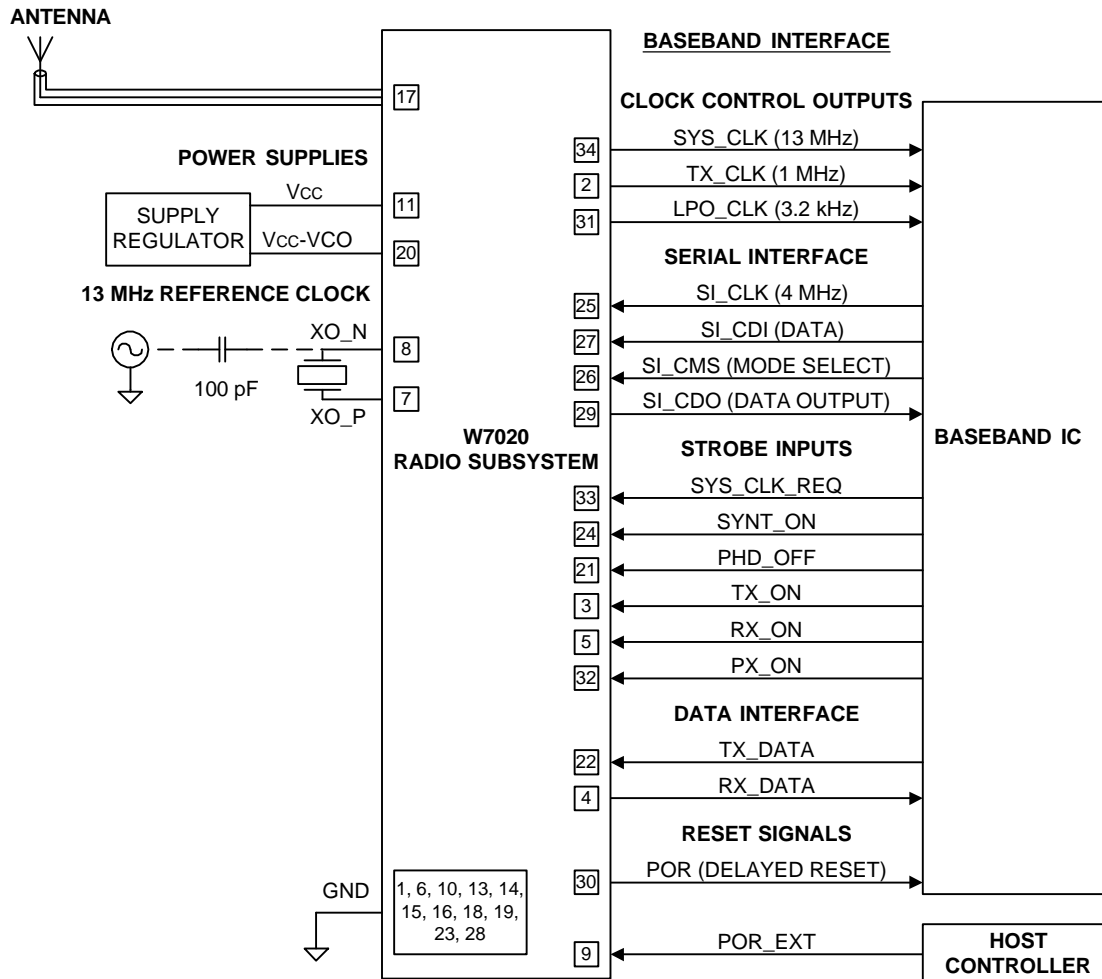

Figure 2. System Connections

Description (continued)

As shown in Figure 3, the antenna filter bandpass filters the radio signal to the antenna switch. The switch directs the signal to the RX balun or from the TX balun. The RX balun performs the transformation from unbalanced to balanced for the RX signal and connects to the low-noise amplifier (LNA). The LNA is followed by an image rejection mixer, so no additional image filter is needed before the mixer. The IF signal out of the mixer is filtered by a bandpass filter and followed by a limiting amplifier and frequency discriminator, giving the RX data output. This discriminator output is offset-corrected. The receiver IF and detection circuits are all integrated, requiring no external components. The RSSI level is available digitally through the serial interface.

The transmitter path utilizes direct modulation of the TX data-bit stream onto the VCO. The TX data is shaped by the Gaussian filter and then is applied to the VCO tank. The VCO is buffered internally and driven to the TX balanced output through another amplifier stage. The TX balun performs the transformation of the balanced to unbalanced signal and connects to the antenna switch.

The VCO frequency operating in the 2.4 GHz ISM band is controlled by the phase-locked loop (PLL) synthesizer through the loop filter. The reference clock oscillator is provided so that only a crystal resonator needs to be added externally to the module, or the reference clock input can be overdriven with an external signal such as from a TCXO or VCXO. The frequency accuracy requirement is ±20 ppm.
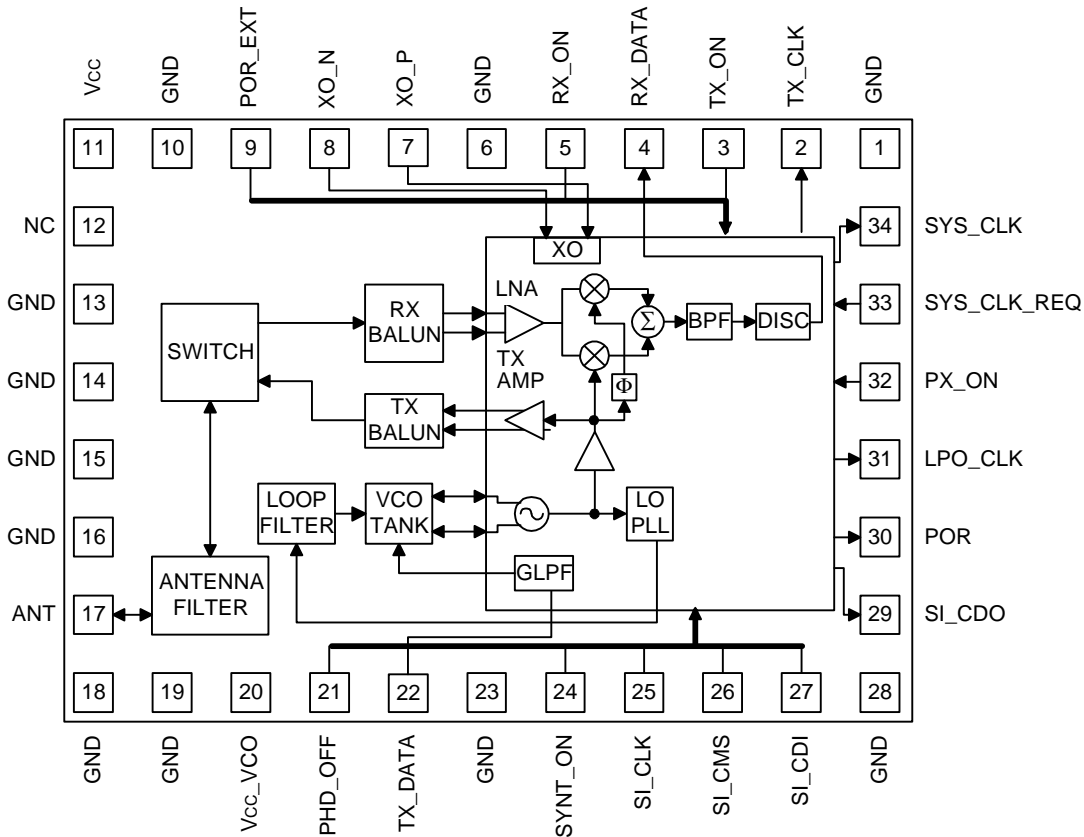

Figure 3. Module Block Diagram with Pinout

Pin Information

Table 1. Pin Descriptions

Pin #	Symbol	Type*	Description
1	GND	Ground	Common ground
2	TX_CLK	D Output	1 MHz clock
3	TX_ON	D Input	Transmit power on
4	RX_DATA	D Output	Received data input
5	RX_ON	D Input	Receiver power on
6	GND	Ground	Common ground
7	XO_P	A Input	Crystal positive input
8	XO_N	A Input	Crystal negative input or external clock input
9	POR_EXT	D Input	External power-on reset
10	GND	Ground	Common ground
11	Vcc	Power	Common power supply
12	NC	—	Not connected
13	GND	Ground	Common ground
14	GND	Ground	Common ground
15	GND	Ground	Common ground
16	GND	Ground	Common ground
17	ANT	RF 50 Ω	Antenna input/output
18	GND	Ground	Common ground
19	GND	Ground	Common ground
20	Vcc_VCO	Power	VCO power supply
21	PHD_OFF	D Input	Open PLL
22	TX_DATA	D Input	Transmit data input
23	GND	Ground	Common ground
24	SYNT_ON	D Input	Synthesizer (PLL) powerup
25	SI_CLK	D Input	Serial interface clock
26	SI_CMS	D Input	Serial interface mode select
27	SI_CDI	D Input	Serial interface data input
28	GND	Ground	Common ground
29	SI_CDO	D Output	Serial interface data output
30	POR	D Output	Power-on reset
31	LPO_CLK	D Output	3.2 kHz low-power clock
32	PX_ON	D Input	Packet on
33	SYS_CLK_REQ	D Input	System clock request
34	SYS_CLK	D Output	System clock

*A = analog; D = digital.

Absolute Maximum Ratings

Stresses in excess of the absolute maximum ratings can cause permanent damage to the device. These are absolute stress ratings only. Functional operation of the device is not implied at these or any other conditions in excess of those given in the operations sections of the data sheet. Exposure to absolute maximum ratings for extended periods can adversely affect device reliability.

Parameter	Symbol	Min	Typ	Max	Unit
Ambient Operating Temperature	T_A	−40	25	100	°C
Storage Temperature	T_{stg}	−65	—	150	°C
Lead Temperature (soldering, 10 s)	—	—	—	230	°C
Positive Supply Voltage	V_{CC}	0	—	4.5	V
Power Dissipation	P_D	—	—	350	mW
ac peak-to-peak Input Voltage	V_{p-p}	0	—	V_{CC}	V
Digital Voltages	—	−0.3	—	V_{CC} + 0.3	V

Handling Precautions

Although protection circuitry has been designed into this device, proper precautions should be taken to avoid exposure to electrostatic discharge (ESD) during handling and mounting. Lucent Technologies Microelectronics Group employs a human-body model (HBM) and a charged-device model (CDM) for ESD-susceptibility testing and protection design evaluation. ESD voltage thresholds are dependent on the circuit parameters used to define the model. No industry-wide standard has been adopted for CDM. However, a standard HBM (resistance = 1500 Ω, capacitance = 100 pF) is widely used and, therefore, can be used for comparison purposes. The HBM ESD threshold presented here was obtained by using these circuit parameters:

Parameter	Method	Rating	Unit
ESD Threshold Voltage	HBM	2000	V
ESD Threshold Voltage (corner pins)	CDM	500	V

Operating Range

Performance is not guaranteed over the full range of all conditions possible within this table. However, it lists the ranges of external conditions in which the W7020 provides general functionality, which may be useful in specific applications, without risk of permanent damage. The conditions for guaranteed performance are described in the Electrical Characteristics section.

Parameter	Min	Typ	Max	Unit
Operating Temperature	−35	25	85	°C
External Reference Clock Input Level	0.4	—	2.0	Vp-p
Nominal Operating Voltage	2.7	—	3.6	V

Operating Conditions

Parameter	Min	Typ	Max	Unit
Frequency Range	2.402	—	2.495	GHz
Reference Clock Frequency	12.999740	13.000000	13.000260	MHz
External Reference Clock Level*	0.4	—	1.0	Vp-p
Supply Voltage	2.7	2.8	3.0	V
Antenna Load (VSWR $\leq$ 2.0)	25	50	100	Ω
Operating Temperature	−30	25	75	°C

* Optional overdrive on XO_N pin, ac-coupled.

Digital Inputs/Outputs

Parameter	Min	Typ	Max	Unit
Logical Input Low (0)	−0.3	0	0.2 * Vcc	V
Logical Input High (1)	0.8 * Vcc	Vcc	Vcc + 0.3	V
Input Leakage Current	—	—	5	μA
Input Capacitance	—	—	15	pF
Crystal Input Capacitance (XO_IN)	—	2.5	—	pF
Rise/Fall Time of Digital Inputs	—	—	20	ns
Logical Output Low (0)	—	0	0.4	V
Logical Output High (1)	Vcc – 0.4	Vcc	—	V
LPO Clock Frequency, Trimmed[†]	—	3.2	—	kHz
LPO Clock Frequency Tolerance	—	—	±250	ppm

† Adjusted to 3.2 kHz by the baseband circuit.

Electrical Characteristics

Specifications are guaranteed for V_{CC} = 2.8 Vdc, T_A = 25 °C ± 10 °C.

Supply Currents

Parameter	Min	Typ	Max	Unit
Supply Current*:				
Standby	—	50	100	μA
Synthesizer On	—	22	—	mA
Receive Mode	—	40	52	mA
Transmit Mode	—	33	44	mA

*Currents reflect continuous operation, not TDD mode of operation.

Power Consumption

Mode	TX/RX Data Rate (kbits/s)	Typ	Max	Unit
TX	—	33	44	mA
RX	—	40	52	mA
SYNTH ON	—	22	—	mA
Standby	—	50	100	μA
DM1	14.4/14.4	18	—	mA
DM5	286.7/286.7	32	—	mA
DH1	172.8/172.8	18	—	mA
DH5	723.2/57.6	32	—	mA
HV1	64/64	30	—	mA
HV3	64/64	10	—	mA
Page Scan	—	511	—	μA
Park Mode (1 s interval)	—	108	—	μA

Electrical Characteristics (continued)

Specifications are guaranteed for V_{CC} = 2.8 Vdc ± 100 mV, T_A = 25 °C ± 10 °C.

Transmit Performance

Transmitter power and spectrum characteristics are measured in 100 kHz RBW, unless otherwise specified.

Parameter	Min	Typ	Max	Unit
Frequency Band	2402	—	2495	MHz
Frequency Accuracy*	—	—	±75	kHz
Frequency Drift: 1-slot Packet 3- and 5-slot Packets	— —	5 15	±25 ±40	kHz kHz
Frequency Deviation: 00001111 Pattern 01010101 Pattern	±140 ±115	±150 —	±175 —	KHz kHz
Transmit Power	–2	0	4	dBm
20 dB Signal BW (PN9 PRBS data, in 10 kHz RBW)	—	—	1	MHz
GFSK Modulation Spectrum: ±>550 kHz ±1.550 MHz—2.450 MHz (alternate channel) ±>2.550 MHz (second alternate channel) ±13 MHz	— — — —	–21 –57 –63 –70	–20 –30 –50 –50	dBc dBm dBm dBm
Spurious Emissions: 30 MHz—1 GHz (other than ranges listed below) 810 MHz—960 MHz 1 GHz—12.75 GHz (other than ranges listed below) 1.8 GHz—1.99 GHz 5.1 GHz—5.3 GHz	— — — — —	<–70 <–110 <–65 <–110 <–70	–36 –100 –30 –100 –47	dBm dBm dBm dBm dBm

* This parameter is determined by the accuracy of the reference crystal or external reference clock, specified as <±20 ppm.

Electrical Characteristics (continued)

Specifications are guaranteed for V_{CC} = 2.8 Vdc ± 100 mV, T_A = 25 °C ± 10 °C.

Receiver Performance

Receiver data BER ≤ 0.1%.

Parameter	Min	Typ	Max	Unit
Sensitivity (BER = 1E-3)	—	−78	−72	dBm
Maximum Signal Sensitivity (BER = 1E-3)	−20	−2	—	dBm
Spurious Free Input Dynamic Range	50	70	—	dB
Input 1 dB Compression	−27	−22	—	dBm
Input IP3	—	−14	—	dBm
C/I Co-channel	—	8	11	dB
C/I, ±1 MHz Interference	—	−3	0	dB
C/I, ±2 MHz Interference	—	−32	−30	dB
C/I, ≥3 MHz Interference	—	−42	−40	dB
C/I Image Interference (−6 MHz)	—	−17	−9	dB
C/I Adjacent 1 MHz to Image	—	−30	−20	dB
IM 2 Tone Blocking	−39	−34	—	dBm

Out-of-Band Blocking (CW interferer):
  30 MHz—2000 MHz (other than ranges listed below)
  824 MHz—960 MHz
  1710 MHz—1910 MHz
  2000 MHz—2400 MHz
  2500 MHz—3000 MHz
  3000 MHz—12.75 GHz
	
	−10
	4
	4
	−27
	−27
	−10
		
		10
		10
		10
		−12
		−9
		−4
			
			—
			—
			—
			—
			—
			—
				
				dBm
				dBm
				dBm
				dBm
				dBm
				dBm

Conducted Spurious: @100 kHz RBW:
  30 MHz—1 GHz (other than ranges listed below)
  810 MHz —960 MHz
  2.402 GHz—2.495 GHz
  1 GHz—12.75 GHz (other than ranges listed below)
  1805 MHz —1990 MHz
	
	—
	—
	—
	—
	—
		
		<−60
		<−90
		−60
		<−60
		<−90
			
			−57
			−100
			−47
			−47
			−100
				
				dBm
				dBm
				dBm
				dBm
				dBm

RSSI Sensitivity	—	−70	−60	dBm
Maximum RSSI Response Level	−40	−30	—	dBm
RSSI Absolute Accuracy	−4	—	4	dB

Synthesizer Performance

Parameter	Min	Typ	Max	Unit
Channel Switching Time	—	160	—	µs

SSB Phase Noise:
  Δf = 500 kHz
  Δf = 2 MHz
  Δf = 3 MHz
	
	—
	—
	—
		
		−107
		−122
		−126
			
			−88
			−114
			−124
				
				dBc/Hz
				dBc/Hz
				dBc/Hz

Interface Signal Description

Table 2. Data Interface: CMOS I/O Up to 1 Mbit/s

Pin No.	Pin Name	Function
4	RX_DATA	Connects to baseband and is synchronized to the SYS_CLK signal.
22	TX_DATA	TX data from baseband must be synchronized with TX_CLK signal.

Table 3. Digital Control Inputs: Strobe Signals to Control Various W7020 Features

Pin No.	Pin Name	Function
9	POR_EXT	Reset will occur on the positive edge of an external power-on-reset signal.
5	RX_ON	Logic high enables receiving of RX_DATA; low disables RX_DATA.
3	TX_ON	Logic high enables transmission of TX_DATA; low disables TX_DATA.
33	SYS_CLK_REQ	Logic high starts up SYS_CLK and TX_CLK outputs (if control register bit 2 set).
32	PX_ON	Logic high during synchronization at first data packet from master.
24	SYNT_ON	Logic high enables the VCO/PLL.
21	PHD_OFF	Logic high opens the VCO/PLL control loop.

Table 4. Digital Control Outputs: Output Clocking and Reset Control for the Baseband

Pin No.	Pin Name	Function
2	TX_CLK	1 MHz transmit clock output, available if POR_EXT & SYS_CLK_REQ are high.
34	SYS_CLK	13 MHz reference clock output, available if POR_EXT & SYS_CLK_REQ are high.
31	LPO_CLK	3.2 kHz adjustable low-power oscillator clock, available after Vcc applied.
30	POR	Delayed reset signal (<30 ms) (refer to Power-On Reset and XO Start-Up section).

Table 5. Analog Inputs: Connect XTAL Off-Module or External Oscillator Signal (0.4 Vp-p to 1.0 Vp-p)

Pin No.	Pin Name	Function
7	XO_P	Connect XTAL. Leave unconnected when using external clock.
8	XO_N	Connect XTAL or external signal, ac-coupled.

Table 6. Serial Interface: Based on the Boundary-Scan Architecture, *IEEE** 1149.1

Pin No.	Pin Name	Function
27	SI_CDI	Control data input; transports serial data to the W7020.
26	SI_CMS	Control mode select; determine transitions from one state to another with the CLK positive edge.
25	SI_CLK	Control clock; control timing of the serial interface.
29	SI_CDO	Control data out; transports serial data from the W7020 to baseband.

* *IEEE* is a registered trademark of the Institute of Electrical and Electronic Engineers, Inc.

Serial Interface

The serial interface implementation is based on the boundary-scan architecture, *IEEE* Std. 1149.1. Figure 4 shows a block diagram of the serial interface. It is identical to the boundary-scan architecture if the extra control signals from the controller access port (CAP) block are removed.

The interconnection between the serial interface and the external controller (baseband chip) consists of four 1-bit signals: control data input (CDI), control mode select (CMS), control clock (CLK), and control data output (CDO).

The CDI signal transports serial data to the W7020, while the CDO signal transports serial data out of the W7020.
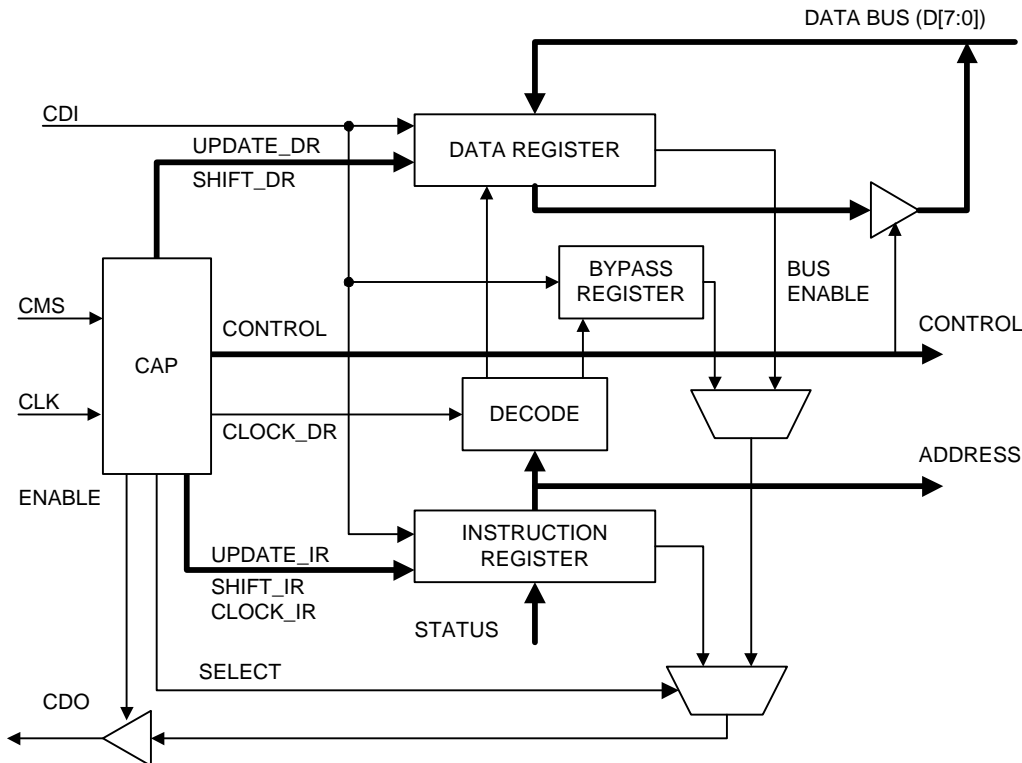
Figure 4. Slave Serial Interface (*IEEE* Std. 1149.1)

The CAP is a controller-state machine and is controlled by the CLK and CMS signals. The CAP, which consists of 16 states, determines whether an instruction register scan or a data register scan will be performed. In these two register scan cycles, data are exchanged between the interconnected units. The interface architecture contains three types of registers: instruction register (IR), bypass register (BYP), and data register (DR).

The structure of the instruction register is shown in Figure 5. The register has a serial data input (CDI) and serial data output (CDO), as well as parallel status inputs and outputs. During a scan period, serial data are shifted through the register. Shadow latches are needed to hold the parallel output at a steady value when shifting occurs. The width of the instruction register is 6 bits.

Serial Interface (continued)

STATUS

CDI → INSTRUCTION SHIFT REGISTER → CDO
CLOCKIR →
SHIFTIR →

UPDATEIR → SHADOW LATCHES
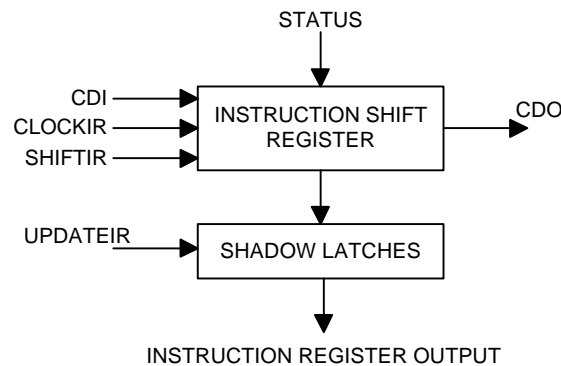
INSTRUCTION REGISTER OUTPUT

Figure 5. Instruction Register

The data register has a structure similar to the IR. The data width is 8 bits.

The bypass register consists of a single register bit and forms a scan path between CDI and CDO.

CAP State Diagram

The CAP state diagram is shown in Figure 6. Transitions from one state to another depend on the CMS input and occur at the rising edge of the CLK. The CMS and CDI inputs should change value on the falling edge of CLK. The CDO output changes on the negative edge of CLK.

An instruction register scan (IR-scan) period starts with a status information download (capture-IR). The status inputs to the instruction register are user-defined observability inputs. However, the two least significant status information bits are fixed to **01** during the capture-IR according to the standard. Afterward, the data can be shifted out (shift-IR) at the same time serial data is shifted in, or directly updated to the parallel output (exit1-IR, update-IR). It also is possible for the IR-scan period to be paused (pause-IR) before a new data shift. A data register scan period is identical, but there are no restrictions on the data during capture-DR.

The control-logic-reset state can always be reached from any other state by allowing the CMS input to be high for five clock cycles.

Serial Interface (continued)
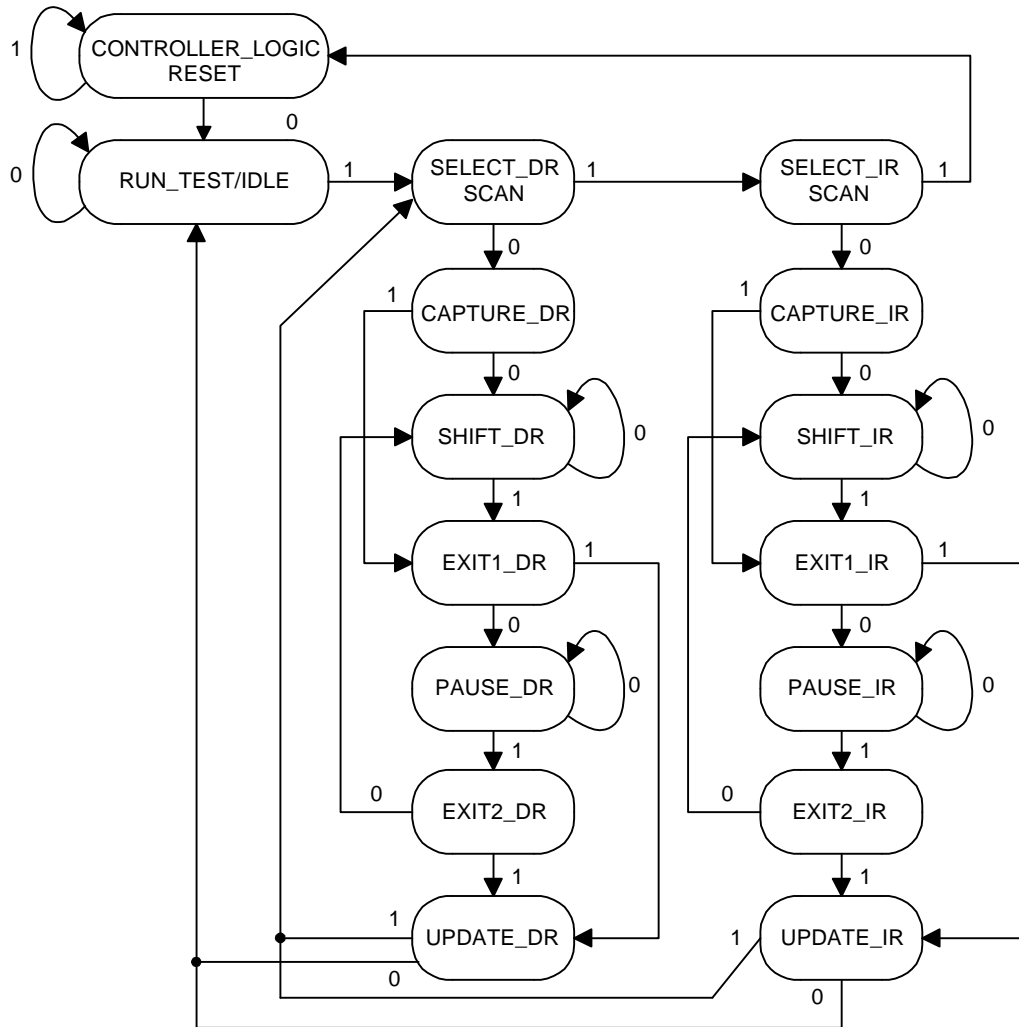
CAP State Diagram (continued)

Figure 6. CAP State Diagram

Serial Interface (continued)

Reserved Instructions

Two reserved instructions are implemented. The first is the bypass instruction. Its bit code is defined to be all ones. This instruction allows serial data to be transferred through the circuit from CDI to CDO with the bypass register connected between, one clock signal delayed. The second is the normal read/write instruction. This instruction selects a specific register to write to or read from. The bit code of this instruction is defined to be 01XXXX, where XXXX is the register address (see Table 7).

W7020 Registers

W7020 registers are accessed by the instruction register output. Every register has a unique address. Table 7 lists the various registers, their read or write status, and their addresses.

Table 7. W7020 Registers

Register Name	# of Bits	R/W	Address
VCO/DAFC Control	8	W	010001 = 17
Channel	8	W	010010 = 18
RSSI	5	R	
XO-Trim	6	W	010011 = 19
ID	8	R	
LPO-hi	1	W	010100 = 20
LPO-lo	8	W	010101 = 21
Control	7	W	010110 = 22
CHP and TX Control	8	W	010111 = 23
Current Control	3	W	011000 = 24
Enable	8	W	011001 = 25

The W7020 registers are explained in Table 8 through Table 18.

Serial Interface (continued)

W7020 Registers (continued)

Table 8. VCO/DAFC/Delay Control (Address = 17)*

Bit No.	Bit Name	Reset Value	Baseband Standard Setting	Function
7	DelP	0	1	Delays PHD_OFF negative edge by 6 μs—7 μs if DelP = 1.
6	DelS	0	1	Delays SYNT_ON negative edge by 6 μs—7 μs if DelS = 1.
5	Dtrim	0	1	Enables DAFC diode voltage trim: 1 = enable. 0 = default diode voltage.
4	DAFC1	0	1	Sets the diode voltage in 50 mV steps if Dtrim = 1.
3	DAFC0	0	1	
2	—	—	0	—
1	VCO1	0	1	Sets the VCO core current.
0	VCO0	0	1	

* — = not applicable.

Table 9. Channel Register (Address = 18)

Bit No.	Bit Name	Reset Value	Function
7	RX/TX	0	Receive or transmit channel: 1 = RX; 0 = TX.
6	C6	0	Channel value (0 dec—127 dec).
5	C5	0	
4	C4	0	
3	C3	0	
2	C2	0	
1	C1	1	
0	C0	0	

Serial Interface (continued)

W7020 Registers (continued)

Table 10. RSSI Register (Address = 18)*

Bit No.	Bit Name	Reset Value	Function
7	—	—	—
6	—	—	—
5	—	—	—
4	RS4	U	Received signal strength indicator. Lower input power gives lower RSSI value.
3	RS3	U	
2	RS2	U	
1	RS1	U	
0	RS0	U	

* — = not applicable; U = undefined.

Table 11. XO-Trim Register (Address = 19)*

Bit No.	Bit Name	Reset Value	Function
7	—	—	—
6	—	—	—
5	XO5	0	Trim value for the internal capacitor load of the crystal ($0 \longrightarrow$ max f_{XO}; $63 \longrightarrow$ min f_{XO}).
4	XO4	0	
3	XO3	0	
2	XO2	0	
1	XO1	0	
0	XO0	0	

* — = not applicable.

Serial Interface (continued)

W7020 Registers (continued)

Table 12. ID Register (Address = 19)*

Bit No.	Bit Name	Reset Value	Function
7	C13	0	—
6	C12	0	
5	C11	0	
4	C10	1	
3	V13	U	Version number (P4B = 0111, P5B = 1000).
2	V12	U	
1	V11	U	
0	V10	U	

* U = undefined.

Table 13. LPO-Hi Register (Address = 20)*

Bit No.	Bit Name	Reset Value	Function
7	—	—	—
6	—	—	—
5	—	—	—
4	—	—	—
3	—	—	—
2	—	—	—
1	—	—	—
0	L8	0	Most significant bit of the LPO adjust value: L8—L0 = 00 . . . 0 gives max f_{LPO}. L8—L0 = 11 . . . 1 —> min f_{LPO}.

* — = not applicable.

Table 14. LPO-Lo Register (Address = 21)

Bit No.	Bit Name	Reset Value	Function
7	L7	0	Eight least-significant bits of the LPO adjust value: L8—L0 = 000 . . . 0 gives maximum f_{LPO}. L8—L0 = 111 . . . 1 gives minimum f_{LPO}.
6	L6	0	
5	L5	0	
4	L4	0	
3	L3	0	
2	L2	0	
1	L1	0	
0	L0	0	

Serial Interface (continued)

W7020 Registers (continued)

Table 15. Control Register (Address = 22)*

Bit No.	Bit Name	Reset Value	Function
7	—	—	—
6	Ltr3	1	LPO course trimming. Lower value gives higher f_{LPO}.
5	Ltr2	0	
4	Ltr1	0	
3	Ltr0	0	
2	XOctr	0	XOctr crystal oscillator start-up control. After power-on reset, a 0 to 1 transition enables the XO to be controlled by SYS_CLK_REQ.
1	—	—	—
0	—	—	—

* — = not applicable.

Table 16. CHP and TX Control Register (Address = 23)

Bit No.	Bit Name	Reset Value	Baseband Standard Setting	Function
7	ChpTst	0	0	Must be programmed to 0.
6	TX2	0	1	Sets the frequency deviation amplitude
5	TX1	0	0	000 —> maximum deviation.
4	TX0	0	0	111 —> minimum deviation.
3	EnLo1	0	0	Must be programmed to 0.
2	CHP2	0	0	Must be programmed to 0.
1	CHP1	0	0	
0	CHP0	0	0	

Serial Interface (continued)

W7020 Registers (continued)

Table 17. Current Control Register (Address = 24)*

Bit No.	Bit Name	Reset Value	Function
7	RINT2	0	Default reset value is used for normal operation. Does not require programming by baseband.
6	RINT1	0	
5	RINT0	0	
4	—	—	—
3	—	—	—
2	—	—	—
1	—	—	—
0	—	—	—

* — = not applicable.

Table 18. Enable Register (Address = 25)*

Bit No.	Bit Name	Reset Value	Baseband Standard Setting	Function
7	PXen	0	1	Must be programmed to 1.
6	—	0	0	Must be programmed to 0.
5	—	0	1	Must be programmed to 1.
4	—	0	1	Must be programmed to 1.
3	—	0	1	Must be programmed to 1.
2	—	0	1	Must be programmed to 1.
1	DEn	0	1	Must be programmed to 1.
0	TXinv	0	1	Must be programmed to 1.

*— = not applicable.

Serial Interface (continued)

Channel Register Programming Example

The following example demonstrates how to program the W7020 for transmit channel 50. The first step is to point to the channel register by doing an IR-scan. The CMS signal is used to put the CAP (see Figure 7) in the SHIFT_IR state. After the CAP is in the SHIFT_IR state, the channel address value 010010 (18) should be shifted into the CDI input (LSB first). When the CAP returns to the RUN_TEST/IDLE state, the instruction register is updated.

The new channel value is entered by performing a DR-scan. The CMS signal is used to put the CAP in the SHIFT_DR state. The channel value of 50 is shifted in the CDI = 00110010 (50 decimal) LSB first. When the CAP is returned to RUN_TEST/IDLE, the channel register is updated.

If no other W7020 register has been addressed when a new channel value is required, only a new DR-scan needs to be done, because the IR already points to the channel register. When data is shifted in, previous data contained in the selected register will simultaneously be shifted out on the CDO. In the case of the channel register, the value of the RSSI will be shifted out on the CDO.

An example of programming the channel register is shown below. All input signals (CDI, CMS) to the serial interface should change on the negative edge of the serial interface clock (CLK) to eliminate setup and hold violations. The serial interface samples the CDI and CMS signals on the positive edge of CCK. The output signal (CDO) changes on the negative edge. In the final application, CDO is sampled on the positive CLK edge.

CMS	1	1	1	1	1	0	1	1	0	0	0	0	0	0	0	1	1	1	0	0	0	0	0	0	0	0	0	1	1	0	0
	CAP STATE SHIFT_IR										SHIFT_IR AND EXIT						UPDATE IR, SELECT _DR				SHIFT_DR AND EXIT								RUN_TEST IDLE		
CDI	X	X	X	X	X	X	X	X	X	X	0	1	0	0	1	0	X	X	X	X	0	1	0	0	1	1	0	0	X	X	X
	DON'T CARE										CHANNEL REGISTER 18										CHANNEL VALUE 50										
CDO	—	—	—	—	—	—	—	—	—	—	1	0	0	1	1	0	—	—	—	—	?	?	?	?	?	?	?	?	—	—	—
	HIGH IMPEDANCE																				RSSI VALUE										

Figure 7. Serial Interface Channel Register Programming Example Timing Information

Transmit and Receiver Application

Application Circuit Diagram
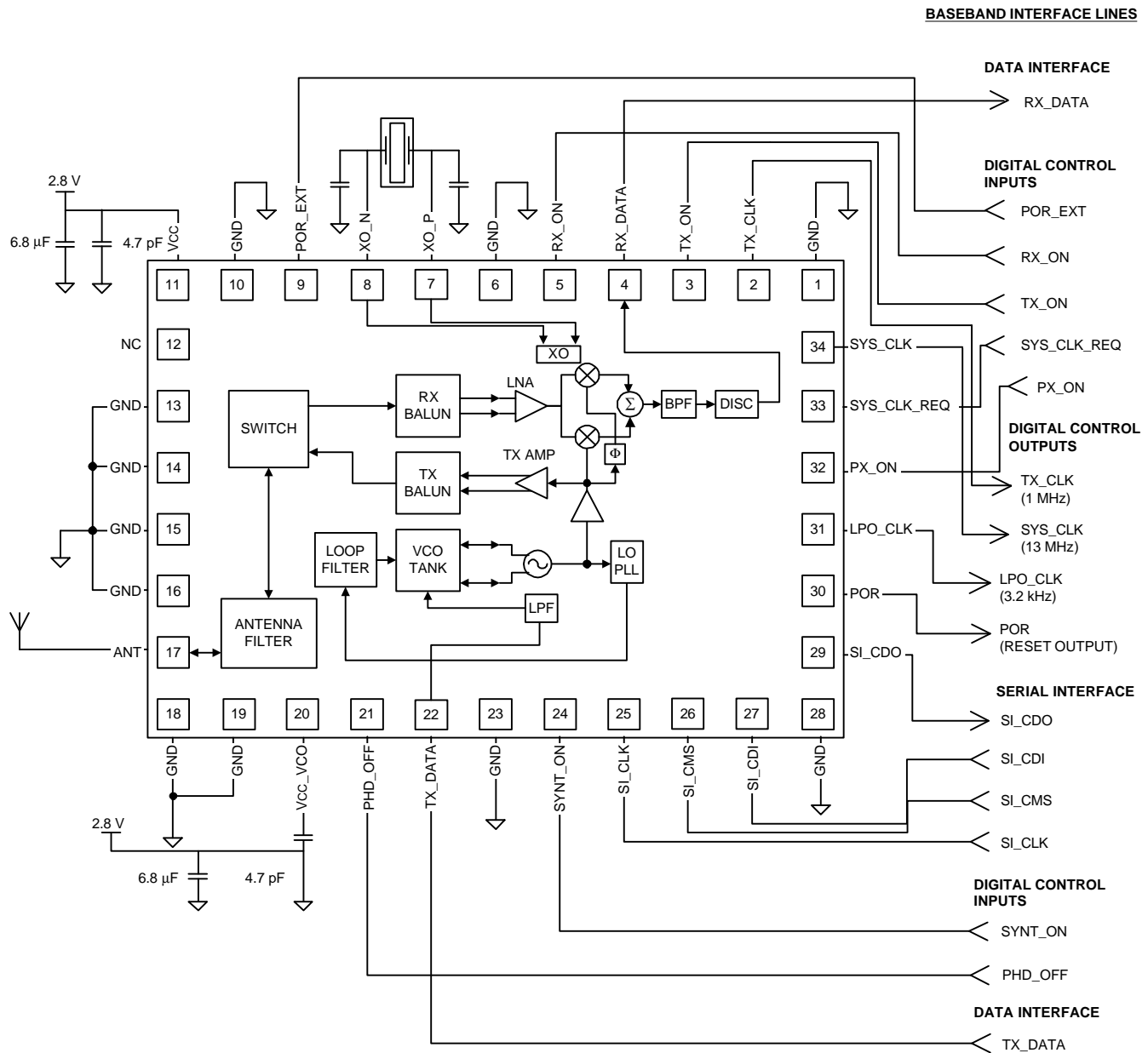
Figure 8. Application Circuit Diagram

Transmit and Receiver Application (continued)

Timing Information

Figure 9 shows the test conditions required to produce a transmit and receive slot with the W7020. (In addition, pins POR_EXT and SYS_CLK_REQ must be held HIGH.)

The transmit slot begins with taking SYNT_ON HIGH. This turns on the synthesizer and voltage-controlled oscillator (VCO). The synthesizer is programmed to the appropriate channel (see the Channel Register Programming Example section). A delay (t_{TO}) is required for the phase-lock loop (PLL) to settle before TX_ON is pulled HIGH. Modulation is achieved by first opening the PLL by taking PHD_OFF high. The transmit data from the baseband device is input into the W7020 TX_DATA pin. The W7020 Gaussian filter shapes the data, and then directly modulates the VCO. After the transmit slot is completed, the TX_ON, PHD_OFF, and SYNT_ON inputs are returned to a LOW for minimum current consumption.
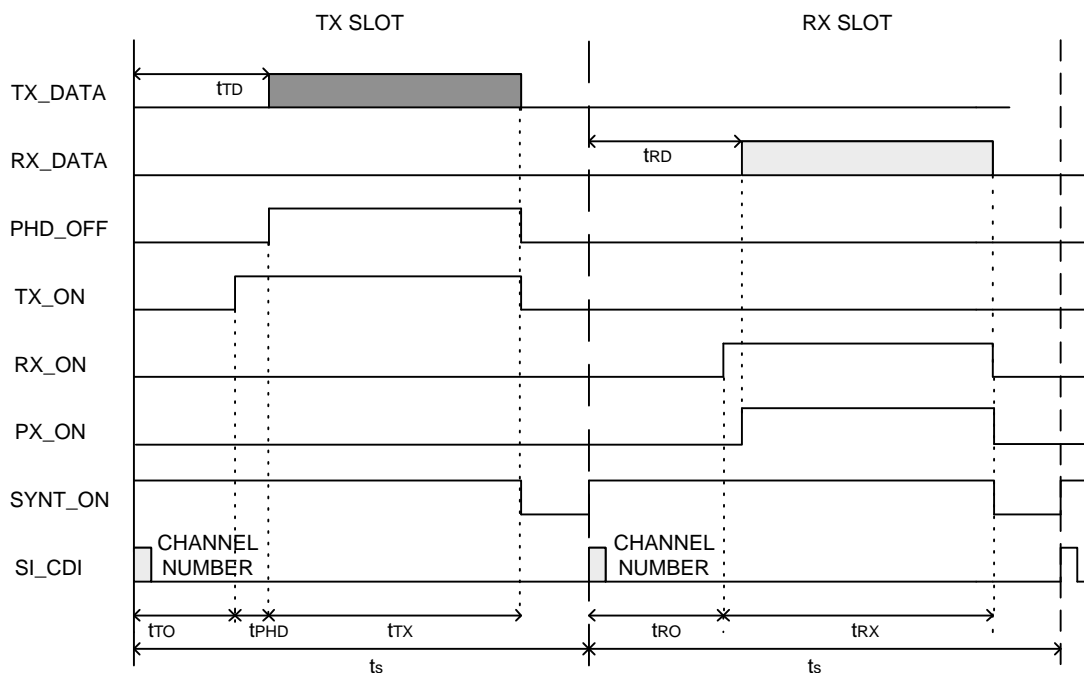
Figure 9. Timing Diagram

Transmit and Receiver Information (continued)

Timing Information (continued)

Table 19. Timing Table

Symbol	Parameter	Min	Typ	Max	Unit
TTX	Data Sending Period, 1-slot Packet	—	—	366	µs
TTX	Data Sending Period, 3-slot Packet	—	—	1622	µs
TTX	Data Sending Period, 5-slot Packet	—	—	2870	µs
TRX	Data Receiving Period, 1-slot Packet	—	—	366	µs
TRX	Data Receiving Period, 3-slot Packet	—	—	1622	µs
TRX	Data Receiving Period, 5-slot Packet	—	—	2870	µs
tPHD	Phase Detector Off Delay after tTO	—	104	—	µs
tRD	Delay Before Receiving Data	—	213	—	µs
tRO	Receiver On Delay	—	208	—	µs
ts	Slot Time, 1-slot Packet	—	625	—	µs
ts	Slot Time, 3-slot Packet	—	1875	—	µs
ts	Slot Time, 5-slot Packet	—	3125	—	µs
tTD	Delay Before Transmitting Data	—	214	—	µs
tTO	Transmitter On Delay	—	110	—	µs

Power-On Reset and XO Start-Up

The power-on reset is a block that creates a reset signal to the digital circuitry. The transition from low to high on the POR signal occurs when the LPO and the crystal oscillator, XO, are running and the POR_EXT signal is high. (See Table 20.) Both POR_EXT and POR are active-low signals.

Table 20. Reset Truth Table

POR_EXT (pin 9)	XO	LPO	POR (pin 30)
0	X	X	0
1	X	No osc.	0
1	No osc.	Osc.	0
1	Osc.	Osc.	1

A power supply drop below a certain voltage level that is caused by, for example, a glitch, will automatically cause a reset.

A 13 MHz crystal should be connected to the XO_N and XO_P pins, as shown in Figure 3. An internal (0 pF—8 pF) capacitive load of the crystal can be adjusted with the XO-trim register so that the crystal runs at 13 MHz within ±20 ppm. Alternatively, an external 13 MHz sinus signal (200 mV—500 mV peak) can be used instead of the external crystal. The clock should be ac-coupled into the XO_N pin.

Figure 10 and Figure 11 show typical powerup initialization and wake-up sequences.

Transmit and Receiver Application (continued)

Timing Information (continued)

Powerup Initialization
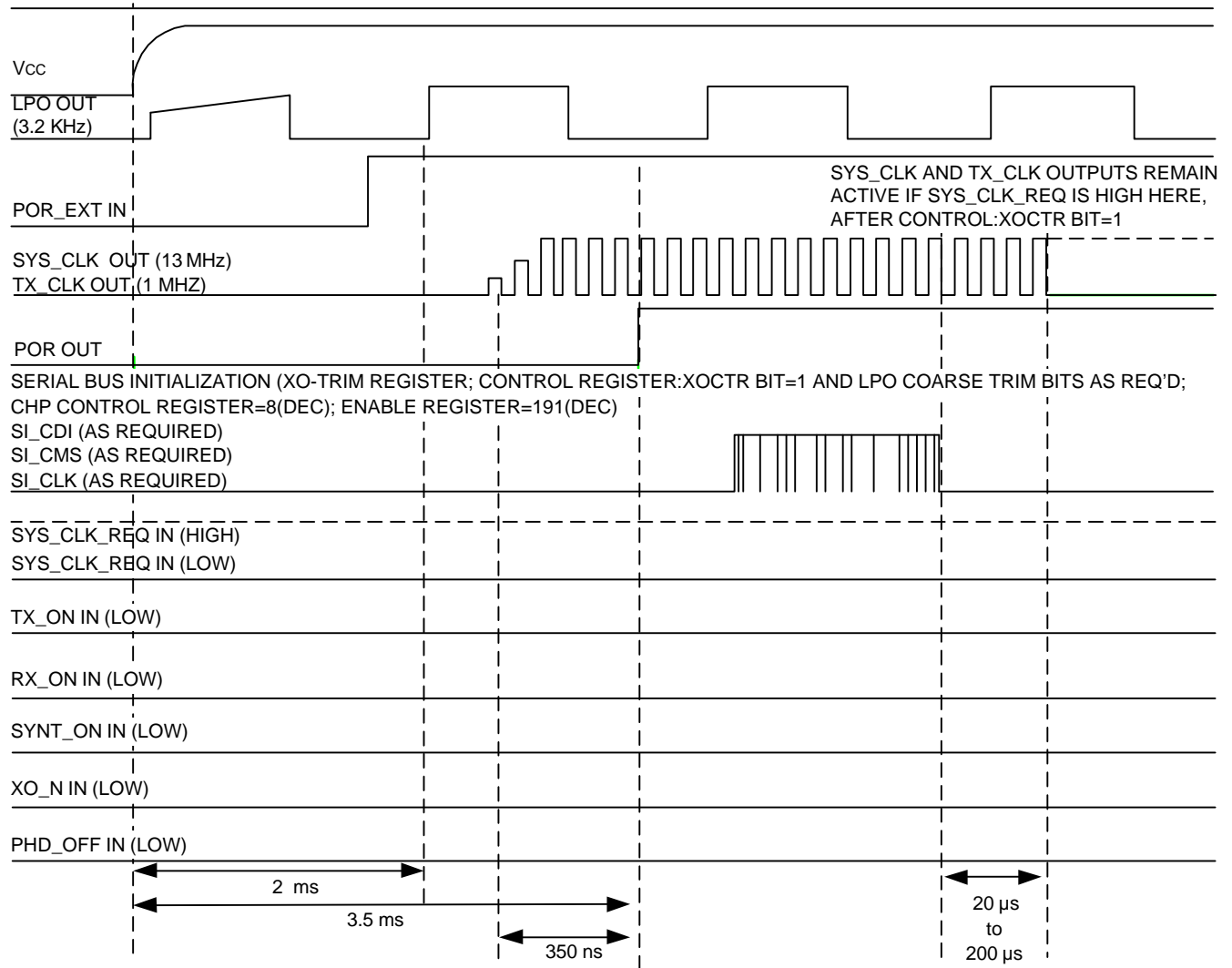
Figure 10. Powerup Initialization Sequence

Transmit and Receiver Application (continued)

Timing Information (continued)

Wake-Up for Connection
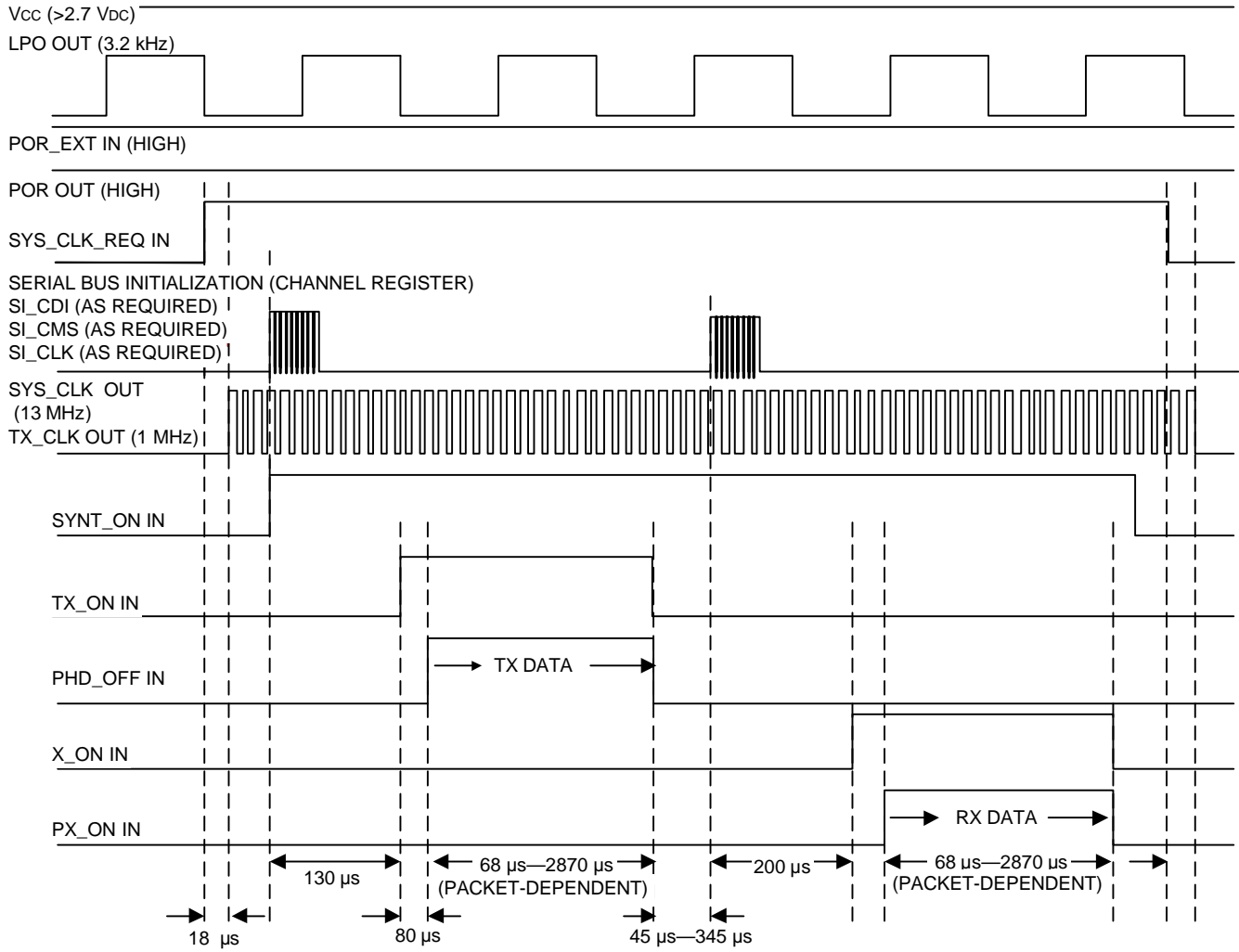
Figure 11. Typical Wake-up-for-Connection Sequence

Transmit and Receiver Information (continued)

RSSI

The RSSI value is a measure of the RF input power that is sampled on the low-high transition of the PX_ON signal. The RSSI value is sent out on the SI-CDO line when the channel register is accessed (same address).

Select, for example, receive channel 50 (channel register = 10110010) and input a GFSK modulated carrier (–60 dBm). Toggle PX_ON low-high-low and read out the RSSI value by accessing the channel register once again. The RSSI value will be in the 6 to 14 range. Input a higher power (–40 dBm). Toggle PX_ON and read out the RSSI value again. The RSSI value will be in the 20 to 28 range.

Characteristic Curves
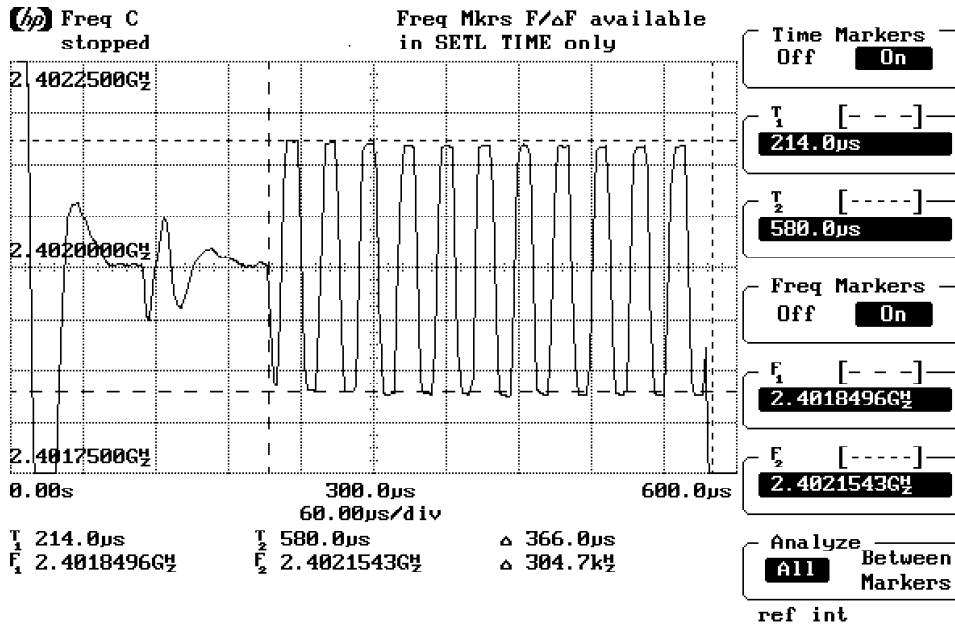
Figure 12. VCO Settling Time and Transmit Slot (16 Alternating 1s and 0s)

Characteristic Curves (continued)
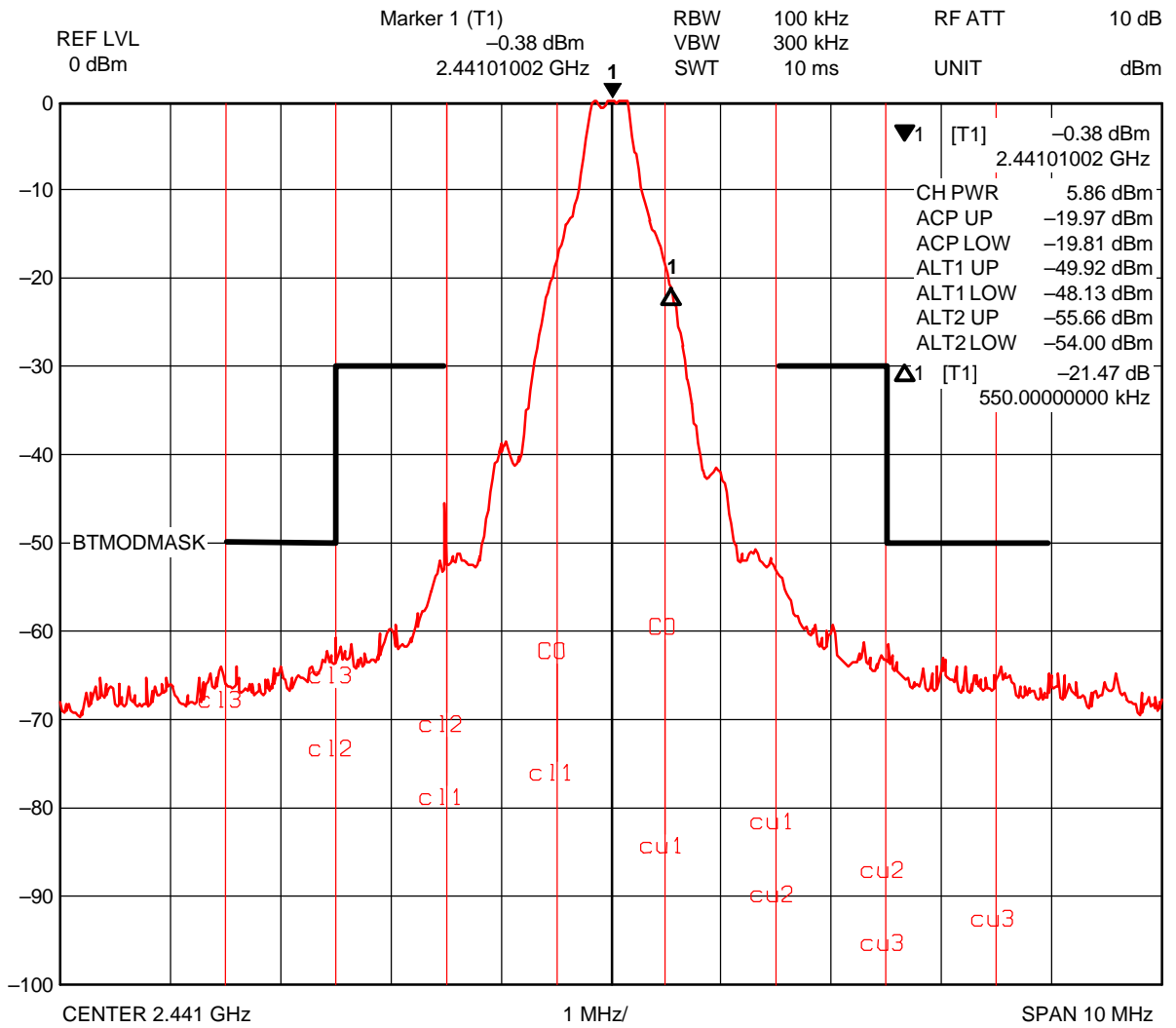
Figure 13. GFSK Transmit Modulation Mask

Characteristic Curves (continued)

	Marker 1 (T1)		RBW	10 kHz	RF ATT	10 dB
REF LVL	−1.81 dBm		VBW	30 kHz		
0 dBm	2.44100501 GHz		SWT	1 s	UNIT	dBm

▼1 [T1]   −1.81 dBm
2.44100501 GHz

△1 [T1]   −20.75 dB
−340.68136273 kHz

△2 [T1]   −20.72 dB
380.60120241 kHz

CENTER 2.441 GHz   500 kHz/   SPAN 5 MHz
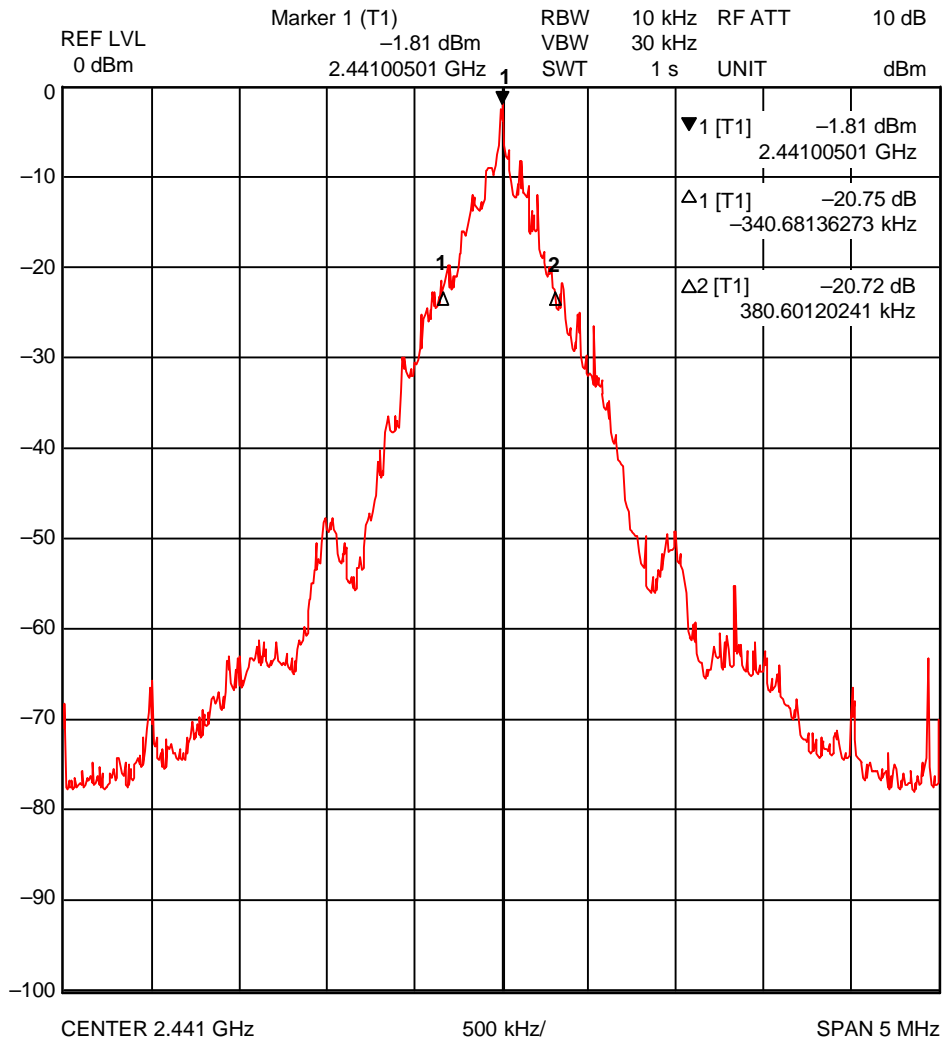
Figure 14. Transmit Modulation Spectrum (−20 dB Bandwidth)

Note: The displayed 20 dB bandwidth = 721 kHz.

Characteristic Curves (continued)
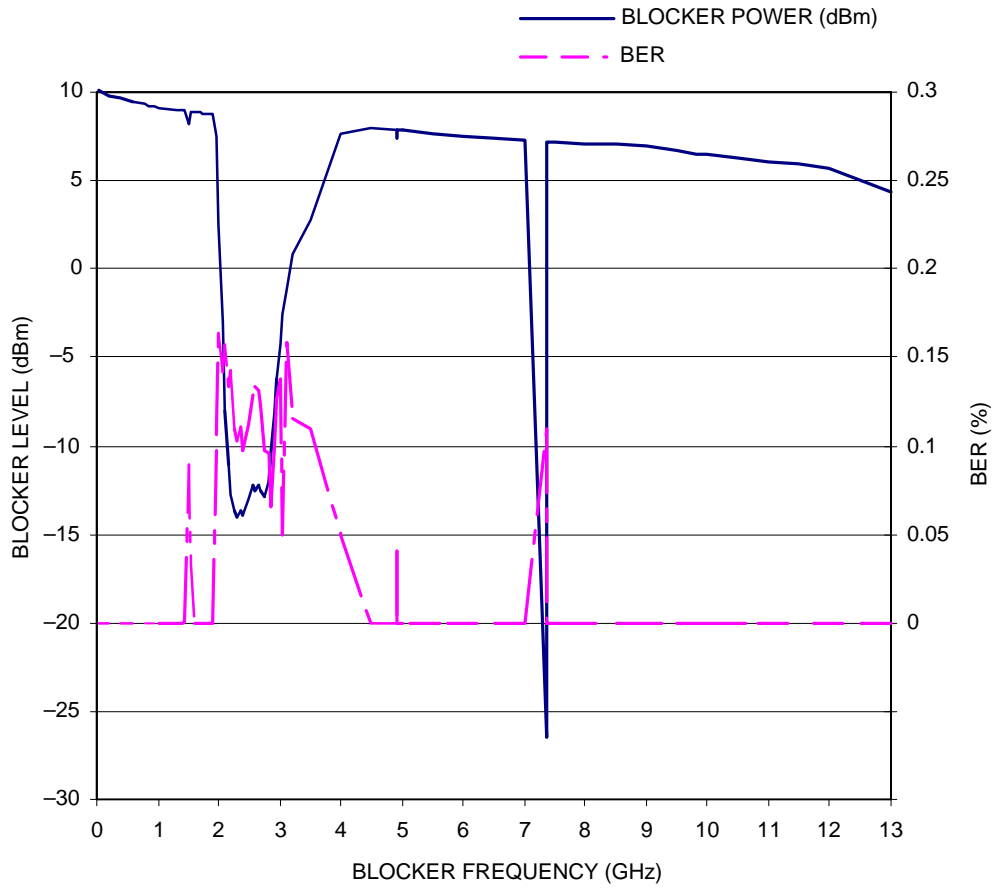
Figure 15. Receiver Out-of-Band Blocking

Note: Bit error rate (BER) less than 0.1% indicates limitations of blocker-signal power level.

Characteristic Curves (continued)
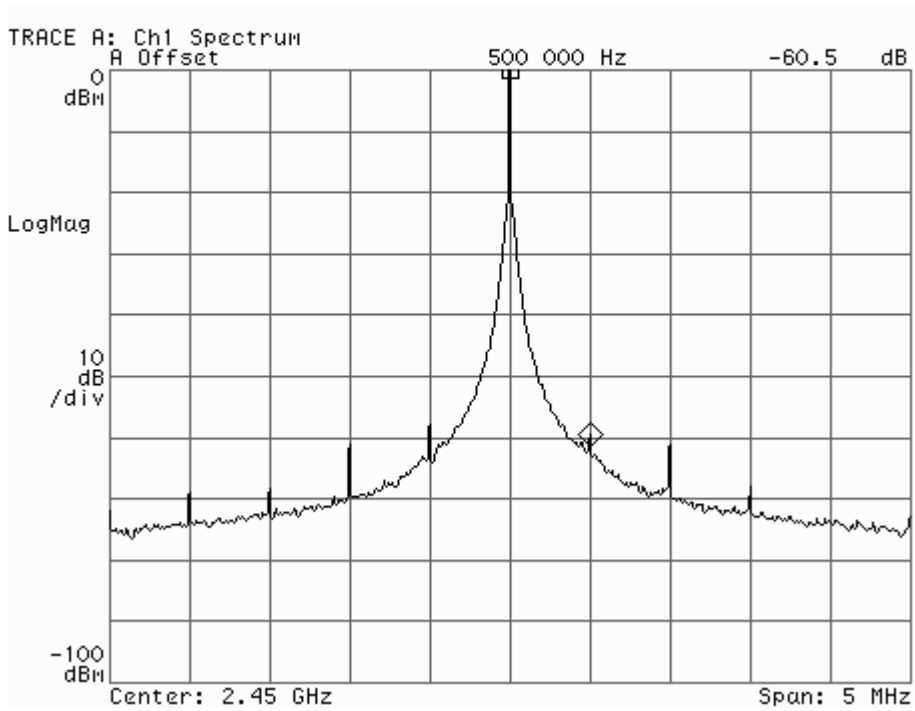
Figure 16. VCO/PLL Synthesizer

Characteristic Curves (continued)
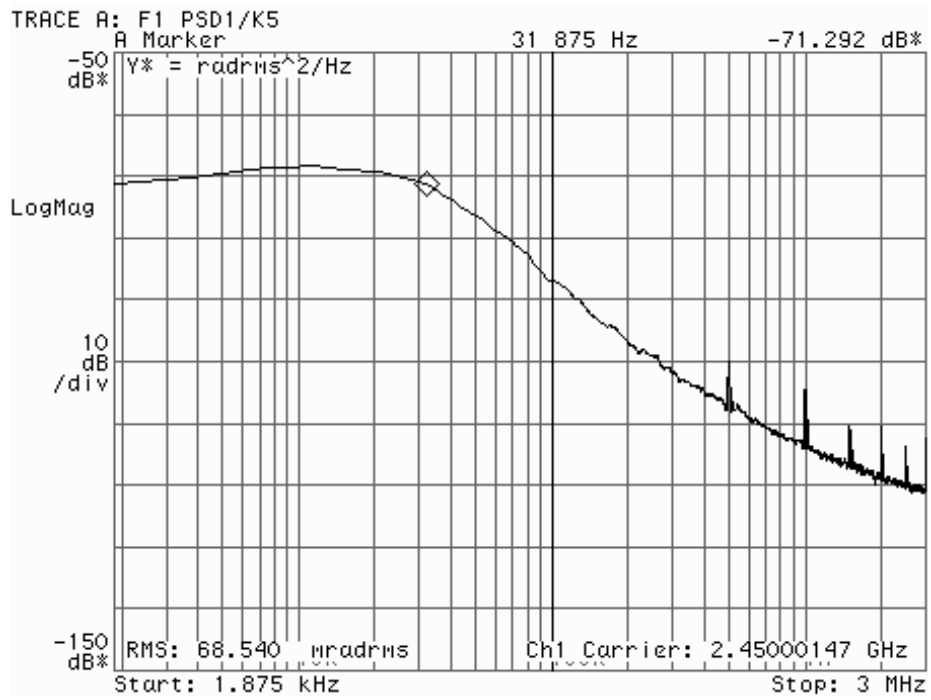
Figure 17. VCO/PLL Synthesizer SSB Phase Noise

Soldering Profile

To prevent damage to the components from crack, etc., the following soldering steps should be followed:

1. Carefully perform preheating so that the temperature difference ΔT between the solder and the component surface is in the range shown in Figure 18.

2. When the components are immersed in solvent after mounting, maintain the temperature difference within 100 °C.

3. Use rosin type flux or weakly active flux with chlorine content of 0.2% weight or less.

4. Use eutectic crystal solder.

Soldering Method	Temperature
Reflow	$\Delta T \leq 130\ ^{\circ}C$
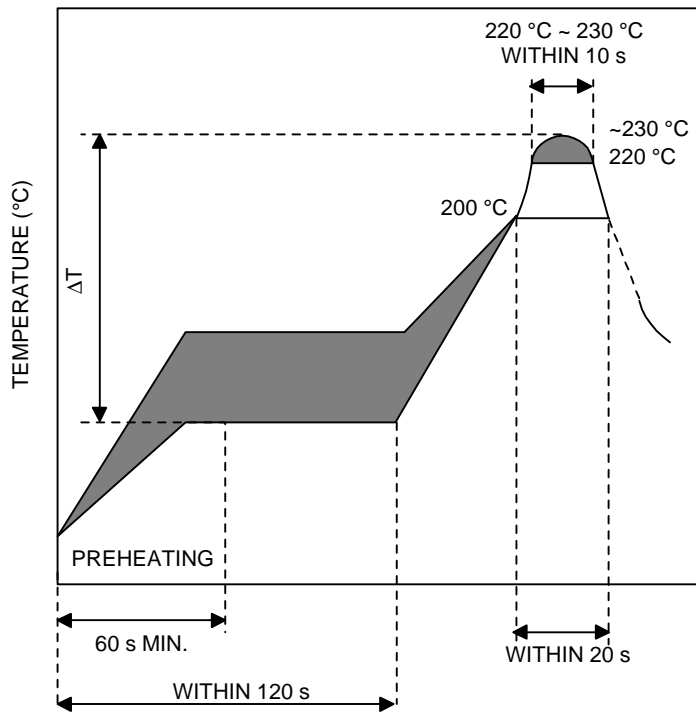
Figure 18. Solder Timing Diagram

Outline Diagram

34-pin MCLGA

Dimensions are in millimeters.
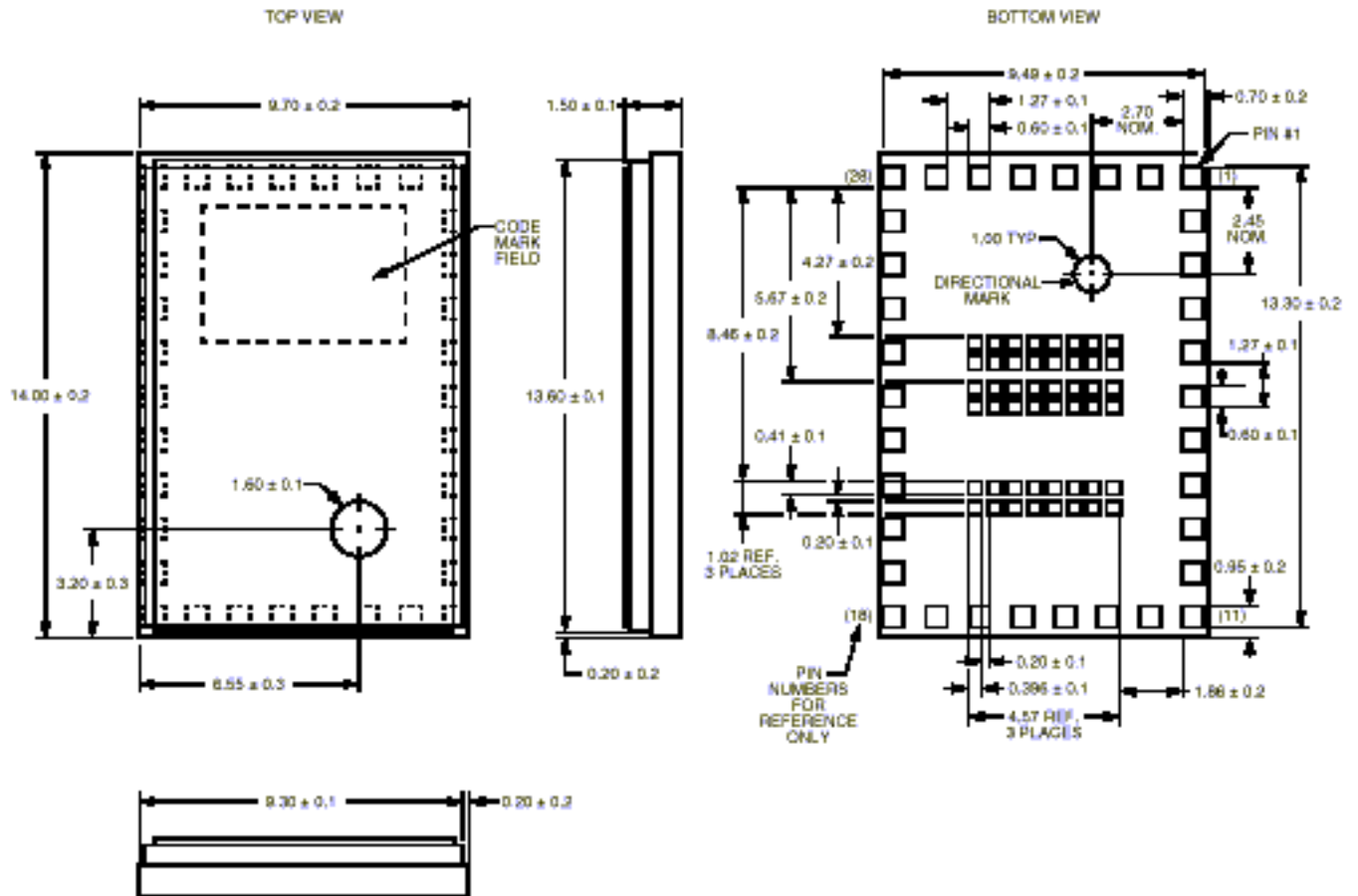
Note: Positions and dimensions of holes in the shield may vary.

Manufacturing Information

This device may be assembled in any of the following locations: J, S, and TW.

Ordering Information

The following devices are available:

- *Bluetooth* Radio Module

- *Bluetooth* Radio Module, Tape and Reel

- *Bluetooth* Radio Module, Bakeable Tray

- *Bluetooth* Radio Module, Dry Pack Tape and Reel

- W7020 Evaluation Board, including Solder-Attached W7020 Bluetooth Radio Module (LUCW7020)

- W7020 *Bluetooth* Radio Module Evaluation Kit, including EVB7020, USB Transceiver Interface Board, and PC Control Software

Contact your Lucent Technologies Microelectronics Group Account Manager for comcode information and minimum order requirements.

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