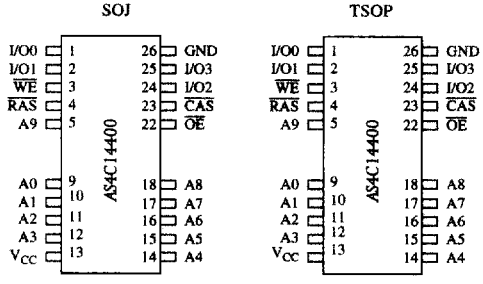
Preliminary information

Features

- Organization: 1,048,576 words × 4 bits
- High speed
  - 50/60 ns $\overline{RAS}$ access time
  - 25/30 ns column address access time
  - 13/15 ns $\overline{CAS}$ access time
- Low power consumption
  - Active: 385 mW max (-60)
  - Standby: 5.5 mW max, CMOS I/O
- Fast page mode
- 1024 refresh cycles, 16 ms refresh interval
  - $\overline{RAS}$-only or $\overline{CAS}$-before-$\overline{RAS}$ refresh
- Read-modify-write
- TTL-compatible, three-state I/O
- JEDEC standard packages
  - 300 mil, 20/26-pin SOJ
  - 300 mil, 20/26-pin TSOP
- Single 5V power supply
- ESD protection ≥ 2000V
- Latch-up current ≥ 200 mA

Pin arrangement



Pin designation

Pin(s)	Description
A0 to A9	Address inputs
$\overline{RAS}$	Row address strobe
I/O0 to I/O3	Input/output
$\overline{OE}$	Output enable
$\overline{CAS}$	Column address strobe
$\overline{WE}$	Read/write control
V_{CC}	Power (5.0 ± 0.5V)
GND	Ground

DRAM

Selection guide

	Symbol	4C14400-50	4C14400-60	Unit
Maximum $\overline{RAS}$ access time	t_{RAC}	50	60	ns
Maximum column address access time	t_{CAA}	25	30	ns
Maximum $\overline{CAS}$ access time	t_{CAC}	13	15	ns
Maximum output enable ($\overline{OE}$) access time	t_{OEA}	13	15	ns
Minimum read or write cycle time	t_{RC}	90	110	ns
Minimum fast page mode cycle time	t_{PC}	35	40	ns
Maximum operating current	I_{CC1}	80	70	mA
Maximum CMOS standby current	I_{CC5}	1.0	1.0	mA

DID 11-30005-A.

Functional description

The AS4C14400 is a high performance CMOS Dynamic Random Access Memory organized as 1,048,576 words × 4 bits. The AS4C14400 is fabricated with advanced CMOS technology and designed with innovative design techniques resulting in high speed, extremely low power and wide operating margins at component and system levels.

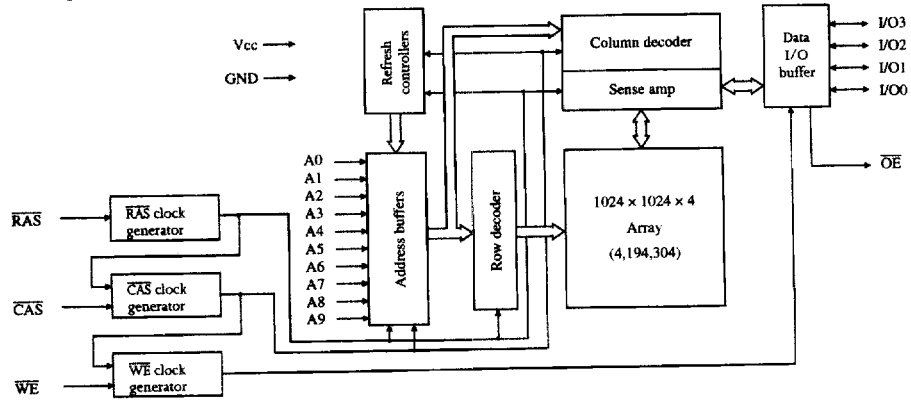
The AS4C14400 features a high speed page mode operation in which high speed read, write and read-write are performed on any of the 1024 × 4 bits defined by the column address. The asynchronous column address uses an extremely short row address capture time to ease the system level timing constraints associated with multiplexed addressing. Output is tri-stated by a column address strobe ($\overline{CAS}$) which acts as an output enable independent of $\overline{RAS}$. Very fast $\overline{CAS}$ to output access time eases system design.

Refresh on the 1024 address combinations of A0 to A9 during a 16 ms period is accomplished by performing any of the following:

- $\overline{RAS}$-only refresh cycles
- Hidden refresh cycles
- $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles
- Normal read or write cycles

The AS4C14400 is available in JEDEC standard 20/26-pin plastic SOJ and 20/26-pin plastic TSOP packages. System level features include single power supply of 5.0 ± 0.5V tolerance and direct interface with TTL logic families.

Logic block diagram



Recommended operating conditions

Parameter	Symbol	Minimum	Nominal	Maximum	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
	GND	0.0	0.0	0.0	V
Input voltage	V_{IH}	2.4	–	V_{CC} + 1	V
	V_{IL}	−1.0	–	0.8	V
Operating temperature	TA	0		70	°C

Recommended operating conditions apply to all specifications unless otherwise noted.

Absolute maximum ratings

Parameter	Symbol	Minimum	Maximum	Unit
Input voltage	V_{in}	-1.0	+7.0	V
Output voltage	V_{out}	-1.0	+7.0	V
Power supply voltage	V_{CC}	-1.0	+7.0	V
Storage temperature (plastic)	T_{STG}	-55	+150	°C
Soldering temperature × time	T_{SOLDER}	–	260 × 10	°C × sec
Power dissipation	P_D	–	1	W
DC output current	I_{out}	–	50	mA

NOTE: Stresses greater than those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions outside those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC electrical characteristics

			-50		-60			
Parameter	Symbol	Test conditions	Min	Max	Min	Max	Unit	Notes
Input leakage current	I_I	$0V \le V_{in} \le +5.5V$ Pins not under test = 0V	-2	+2	-2	+2	µA	
Output leakage current	I_{OZ}	Outputs disabled, $0V \le V_{out} \le +5.5V$	-10	+10	-10	+10	µA	
Operating power supply current	I_{CC1}	$\overline{RAS}$, $\overline{CAS}$, Address cycling: t_{RC}=min	–	80	–	70	mA	1,2
TTL standby power supply current	I_{CC2}	$\overline{RAS} = \overline{CAS} = V_{IH}$	–	2.0	–	2.0	mA	
Average power supply current, $\overline{RAS}$ refresh mode	I_{CC3}	$\overline{RAS}$ cycling, $\overline{CAS}$ = VIH, t_{RC} = min	–	80	–	70	mA	1
Fast page mode average power supply current	I_{CC4}	$\overline{RAS} = V_{IL}$, $\overline{CAS}$ cycling, Address cycling: t_{PC} = min	–	70	–	60	mA	1,2
CMOS standby power supply current	I_{CC5}	$\overline{RAS} = \overline{CAS} = V_{CC}$ - 0.2V	–	1.0	–	1.0	mA	
$\overline{CAS}$-before-$\overline{RAS}$ refresh power supply current	I_{CC6}	$\overline{RAS}$, $\overline{CAS}$ cycling: t_{RC} = min	–	80	–	70	mA	1
Output voltage	V_{OH}	I_{OUT} = -5.0 mA	2.4	–	2.4	–	V	
	V_{OL}	I_{OUT} = 4.2 mA	–	0.4	–	0.4	V	

DRAM

AC parameters common to all waveforms

Symbol	Parameter	-50 Min	-50 Max	-60 Min	-60 Max	Unit	Notes
t_{RC}	Random read or write cycle time	90	–	110	–	ns	
t_{RP}	$\overline{RAS}$ precharge time	30	–	40	–	ns	
t_{RAS}	$\overline{RAS}$ pulse width	50	10K	60	10K	ns	
t_{CAS}	$\overline{CAS}$ pulse width	13	–	15	–	ns	
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ delay time	20	37	20	45	ns	6
t_{RAD}	$\overline{RAS}$ to column address delay time	15	25	15	30	ns	7
$t_{RSH(R)}$	$\overline{CAS}$ to $\overline{RAS}$ hold time (read)	13	–	15	–	ns	
t_{CSH}	$\overline{RAS}$ to $\overline{CAS}$ hold time	50	–	60	–	ns	
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ precharge time	0	–	0	–	ns	
t_{ASR}	Row address setup time	0	–	0	–	ns	
t_{RAH}	Row address hold time	10	–	10	–	ns	
t_T	Transition time (rise and fall)	2	50	2	50	ns	4,5
t_{REF}	Refresh period	–	16	–	16	ms	3
t_{CLZ}	$\overline{CAS}$ to output in Low Z	0	–	0	–	ns	8

Read cycle

Symbol	Parameter	-50 Min	-50 Max	-60 Min	-60 Max	Unit	Notes
t_{RAC}	Access time from $\overline{RAS}$	–	50	–	60	ns	6
t_{CAC}	Access time from $\overline{CAS}$	–	13	–	15	ns	6,13
t_{AA}	Access time from address	–	25	–	30	ns	7,13
$t_{AR(R)}$	Column add hold from $\overline{RAS}$	40	–	45	–	ns	
t_{RCS}	Read command setup time	0	–	0	–	ns	
t_{RCH}	Read command hold time to $\overline{CAS}$	0	–	0	–	ns	9
t_{RRH}	Read command hold time to $\overline{RAS}$	0	–	0	–	ns	9
t_{RAL}	Column address to $\overline{RAS}$ lead time	25	–	30	–	ns	
t_{CPN}	$\overline{CAS}$ precharge time	10	–	10	–	ns	
t_{ODS}	Output disable setup time	0	–	0	–	ns	
t_{OFF}	Output buffer turn-off time	0	13	0	15	ns	8,10

Shaded areas contain advance information.

Write cycle

Symbol	Parameter	-50 Min	-50 Max	-60 Min	-60 Max	Unit	Notes
t_{ASC}	Column address setup time	0	–	0	–	ns	
t_{CAH}	Column address hold time	10	–	10	–	ns	
t_{AWR}	Column address hold time to $\overline{RAS}$	40	–	45	–	ns	
t_{WCS}	Write command setup time	0	–	0	–	ns	11
t_{WCH}	Write command hold time	10	–	10	–	ns	11
t_{WCR}	Write command hold time to $\overline{RAS}$	40	–	45	–	ns	
t_{WP}	Write command pulse width	10	–	10	–	ns	
t_{RWL}	Write command to $\overline{RAS}$ lead time	13	–	15	–	ns	
t_{CWL}	Write command to $\overline{CAS}$ lead time	13	–	15	–	ns	
t_{DS}	Data-In setup time	0	–	0	–	ns	12
t_{DH}	Data-In hold time	10	–	10	–	ns	12
t_{DHR}	Data-In hold time to $\overline{RAS}$	40	–	45	–	ns	

Read-modify-write cycle

Symbol	Parameter	-50 Min	-50 Max	-60 Min	-60 Max	Unit	Notes
t_{RWC}	Read-write cycle time	131	–	155	–	ns	
t_{RWD}	$\overline{RAS}$ to $\overline{WE}$ delay time	73	–	85	–	ns	11
t_{CWD}	$\overline{CAS}$ to $\overline{WE}$ delay time	36	–	40	–	ns	11
t_{AWD}	Column address to $\overline{WE}$ delay time	48	–	55	–	ns	11
$t_{RSH(W)}$	$\overline{CAS}$ to $\overline{RAS}$ hold time (write)	13	–	15	–	ns	
$t_{CAS(W)}$	$\overline{CAS}$ pulse width (write)	13	–	15	–	ns	

Fast page mode cycle

Symbol	Parameter	-50 Min	-50 Max	-60 Min	-60 Max	Unit	Notes
t_{PC}	Read-write cycle time (fast page)	35	–	40	–	ns	14
t_{CAP}	Access time from $\overline{CAS}$ precharge	–	30	–	35	ns	13
t_{CP}	$\overline{CAS}$ precharge time (fast page)	10	–	10	–	ns	
t_{PCM}	Fast page mode RMW cycle	76	–	85	–	ns	
t_{CRW}	Page mode $\overline{CAS}$ pulse width (RMW)	54	–	60	–	ns	
t_{RASP}	$\overline{RAS}$ pulse width	50	100K	60	100K	ns	

Refresh cycle

Symbol	Parameter	-50 Min	-50 Max	-60 Min	-60 Max	Unit	Notes
t_{CSR}	$\overline{CAS}$ setup time ($\overline{CAS}$-before-$\overline{RAS}$)	10	–	10	–	ns	3
t_{CHR}	$\overline{CAS}$ hold time ($\overline{CAS}$-before-$\overline{RAS}$)	10	–	15	–	ns	3
t_{RPC}	$\overline{RAS}$ precharge to $\overline{CAS}$ hold time	0	–	0	–	ns	
t_{CPT}	$\overline{CAS}$ precharge time ($\overline{CAS}$-before-$\overline{RAS}$ counter test)	10	–	10	–	ns	

Output enable

Std Symbol	Parameter	-50 Min	-50 Max	-60 Min	-60 Max	Unit	Notes
t_{ROH}	$\overline{RAS}$ hold time referenced to $\overline{OE}$	10	–	10	–	ns	
t_{OEA}	$\overline{OE}$ access time	–	13	–	15	ns	
t_{OED}	$\overline{OE}$ to data delay	13	–	15	–	ns	
t_{OEZ}	Output buffer turnoff delay from $\overline{OE}$	–	13	–	15	ns	8, 10
t_{OEH}	$\overline{OE}$ command hold time	13	–	15	–	ns	

Notes

1 I_{CC1}, I_{CC3}, I_{CC4}, and I_{CC6} depend on cycle rate.

2 I_{CC1} and I_{CC4} depend on output loading. Specified values are obtained with the output open.

3 An initial pause of 200 µs is required after power-up followed by any 8 $\overline{RAS}$ cycles before proper device operation is achieved. In the case of an internal refresh counter, a minimum of 8 $\overline{CAS}$-before-$\overline{RAS}$ initialization cycles instead of 8 $\overline{RAS}$ cycles are required. 8 initialization cycles are required after extended periods of bias without clocks (greater than 16 ms).

4 AC Characteristics assume t_T = 5 ns. All AC parameters are measured with a load equivalent to two TTL loads and 100 pF, V_{IL} (min) ≥ GND and V_{IH} (max) ≤ V_{CC}. See AC test conditions for more information.

5 V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.

6 Operation within the t_{RCD} (max) limit ensures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.

7 Operation within the t_{RAD} (max) limit ensures that t_{RAC} (max) can be met. t_{RAD} (max) is specified as a reference point only. If t_{RAD} is greater than the specified t_{RAD} (max) limit, then access time is controlled exclusively by t_{AA}.

8 Assumes three state test load (5 pF and a 380 Ω Thevenin equivalent).

9 Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.

10 t_{OFF} (max) defines the time at which the output achieves the open circuit condition; it is not referenced to output voltage levels.

11 t_{WCS}, t_{WCH}, t_{RWD}, t_{CWD} and t_{AWD} are not restrictive operating parameters. They are included in the datasheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$ (min) and $t_{WCH} \geq t_{WCH}$ (min), the cycle is an early write cycle and data out pins will remain open circuit, high impedance, throughout the cycle. If $t_{RWD} \geq t_{RWD}$ (min), $t_{CWD} \geq t_{CWD}$ (min) and $t_{AWD} \geq t_{AWD}$ (min), the cycle is a read-write cycle and the data out will contain data read from the selected cell. If neither of the above conditions is satisfied, the condition of the data out at access time is indeterminate.

12 These parameters are referenced to $\overline{CAS}$ leading edge in early write cycles and to $\overline{WE}$ leading edge in read-write cycles.

13 Access time is determined by the longest of t_{CAA} or t_{CAC} or t_{CAP}.

14 $t_{ASC} \geq t_{CP}$ to achieve t_{PC} (min) and t_{CAP} (max) values.

15 These parameters are sampled and not 100% tested.

AC test conditions

- Access times are measured with output reference levels of V_{OH} = 2V and V_{OL} = 0.8 V
- Input rise and fall times: 5 ns

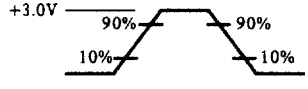


Figure A: Input waveform

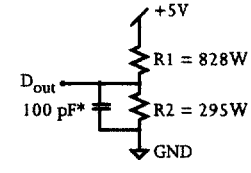


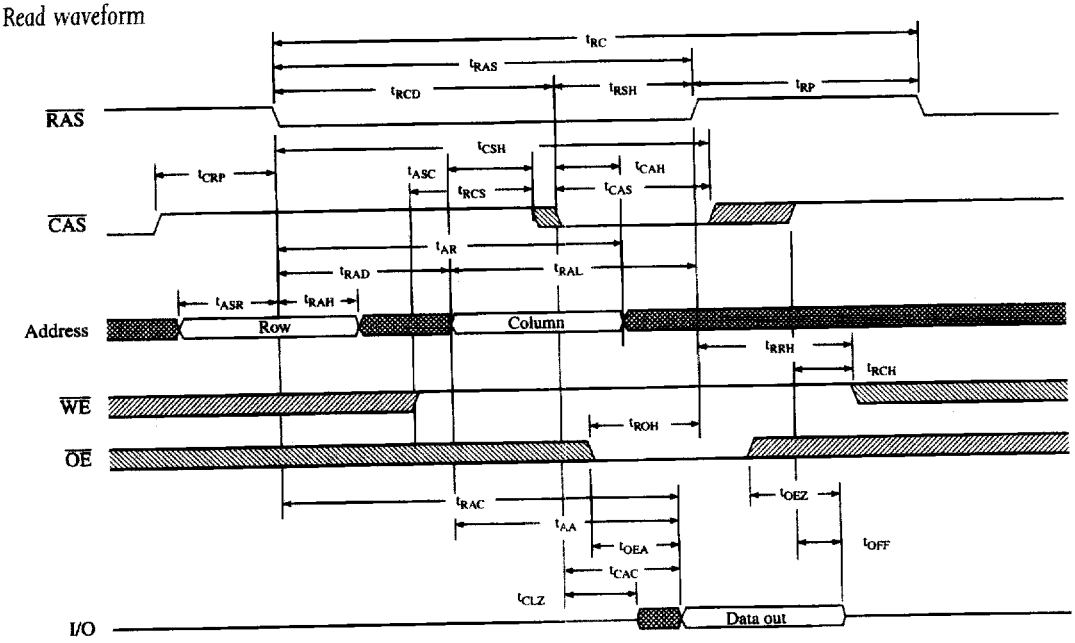
Figure B: Equivalent output load

Key to switching waveforms

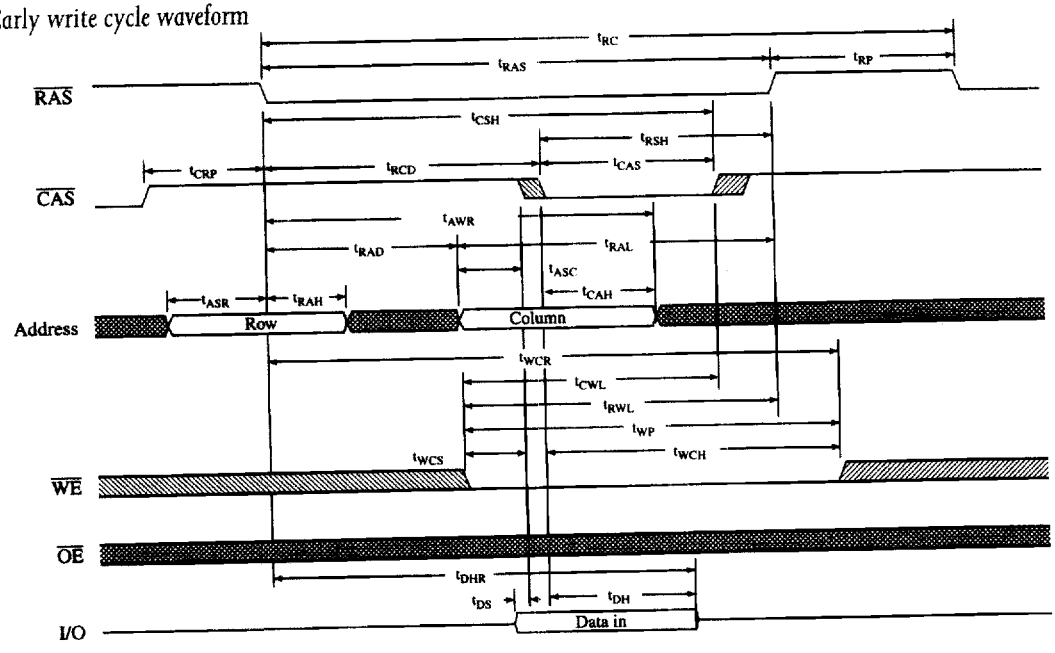
Rising input Falling input Undefined output/don't care

DRAM

Read waveform

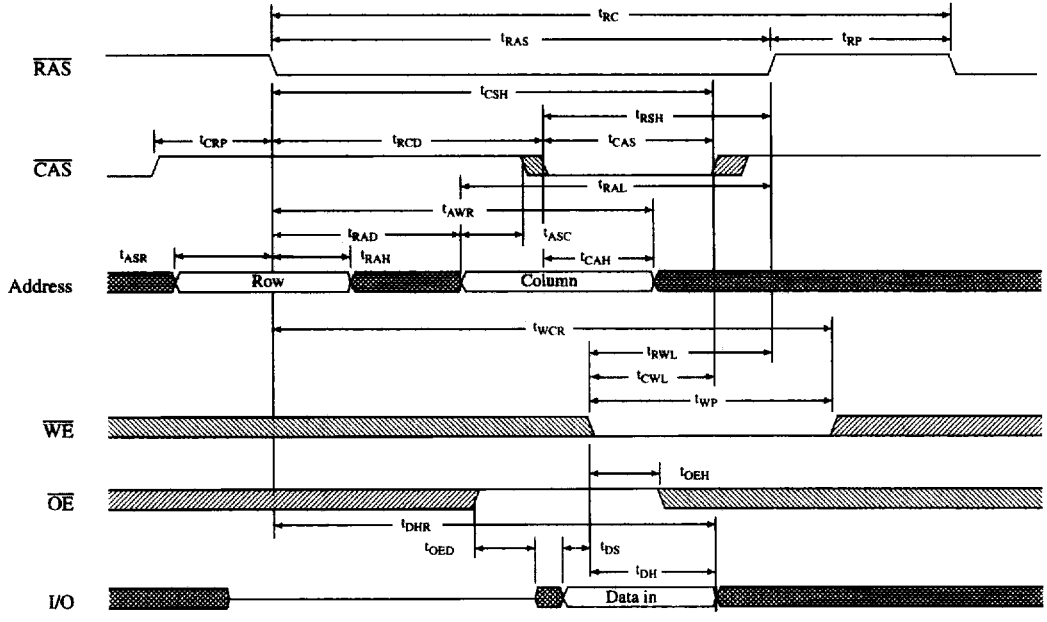


Early write cycle waveform

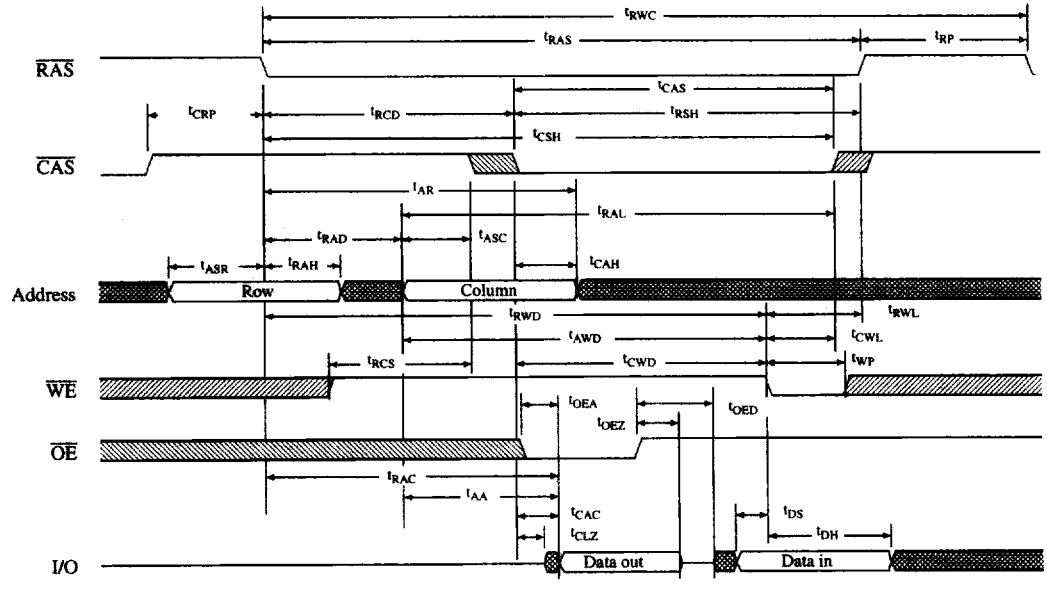


Write waveform

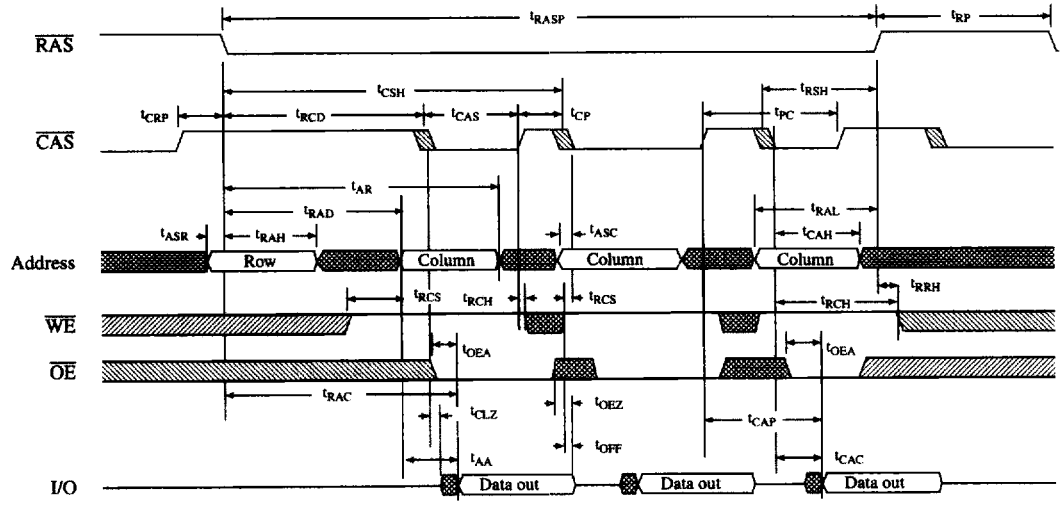
($\overline{OE}$ controlled)



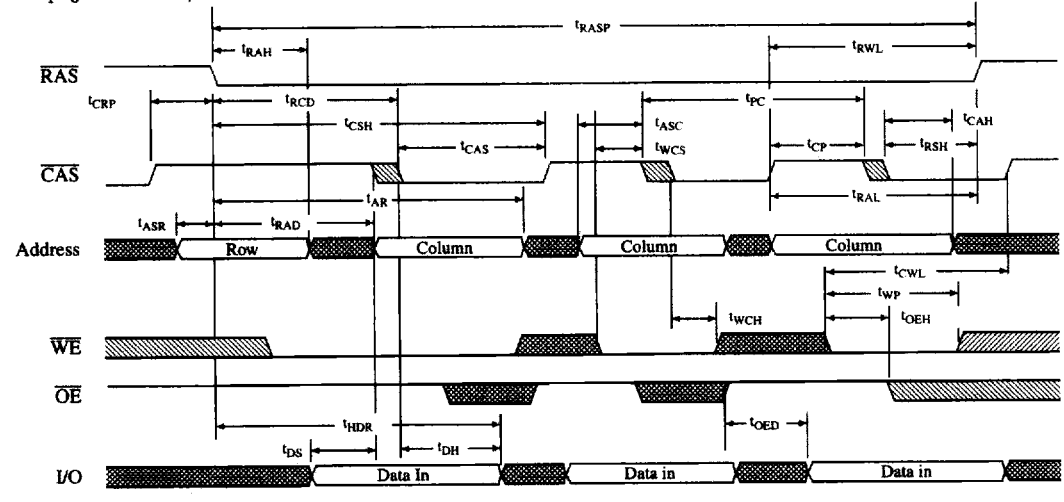
Read-write waveform



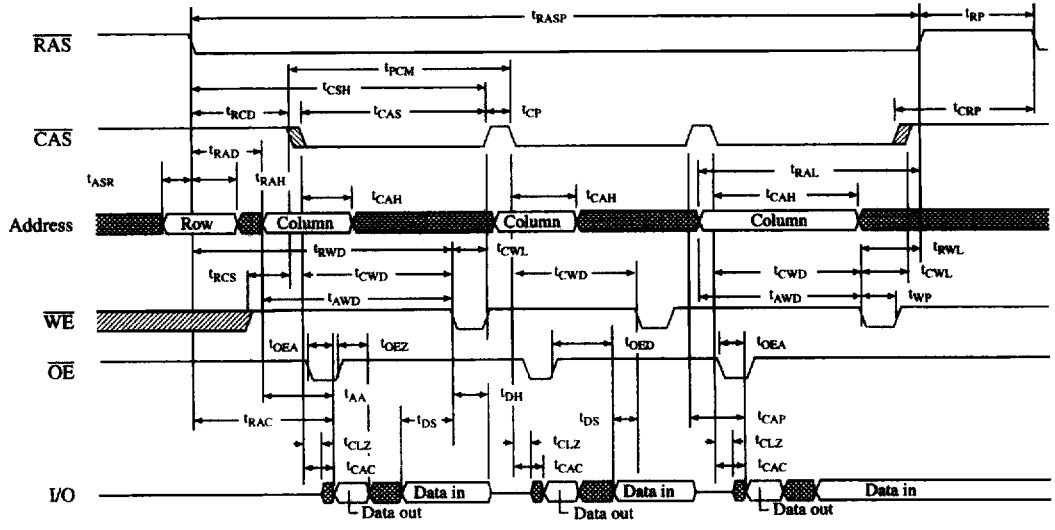
Fast page mode read waveform



Fast page mode early write waveform

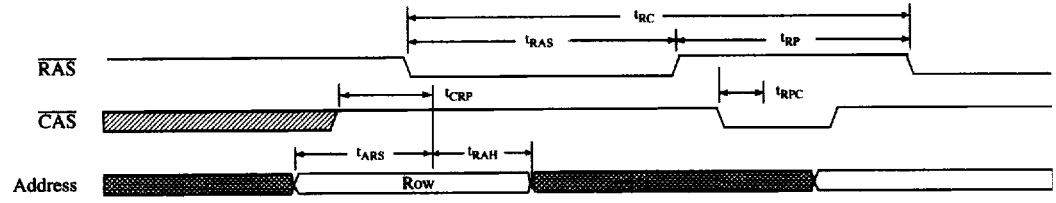


Fast page mode read-write waveform



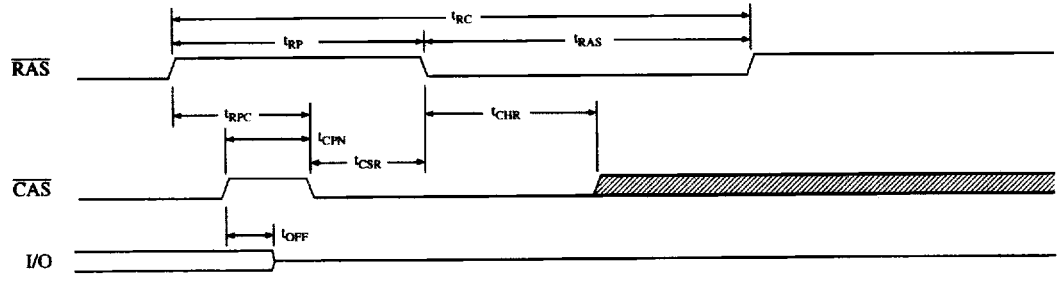
RAS only refresh waveform

($\overline{WE}$ = $\overline{OE}$ = V_{IH} or V_{IL})

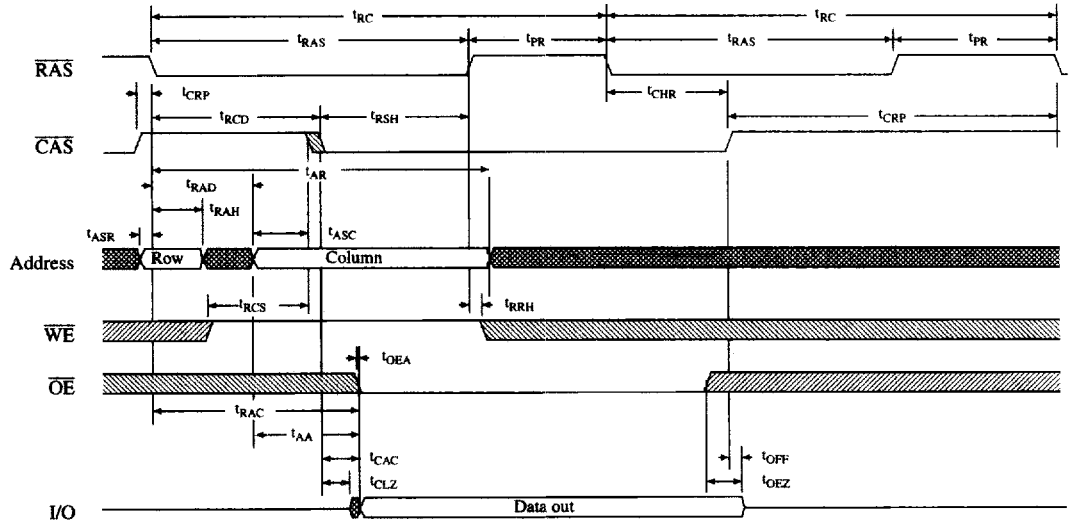


CAS-before-RAS refresh waveform

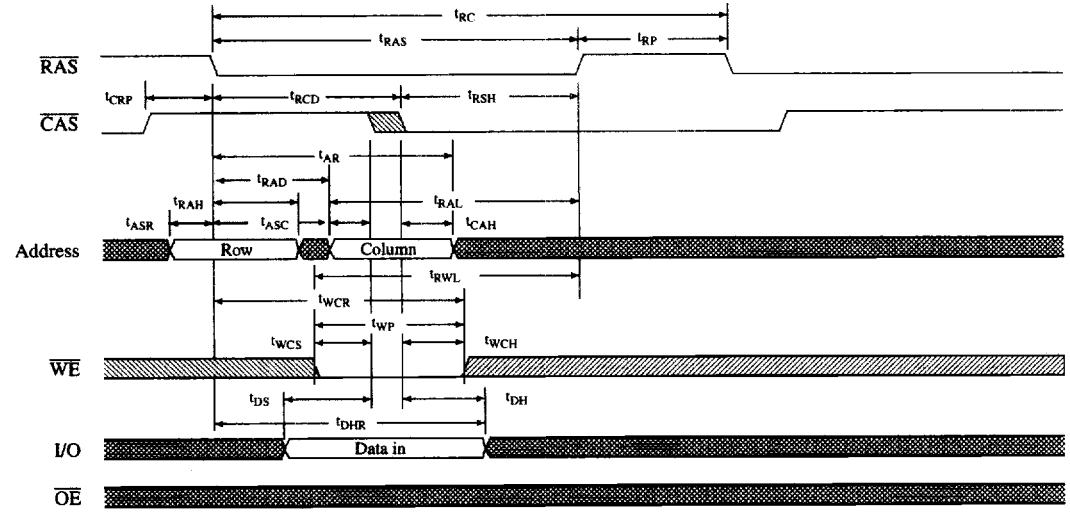
($\overline{WE}$ = $\overline{OE}$ = V_{IH} or V_{IL})



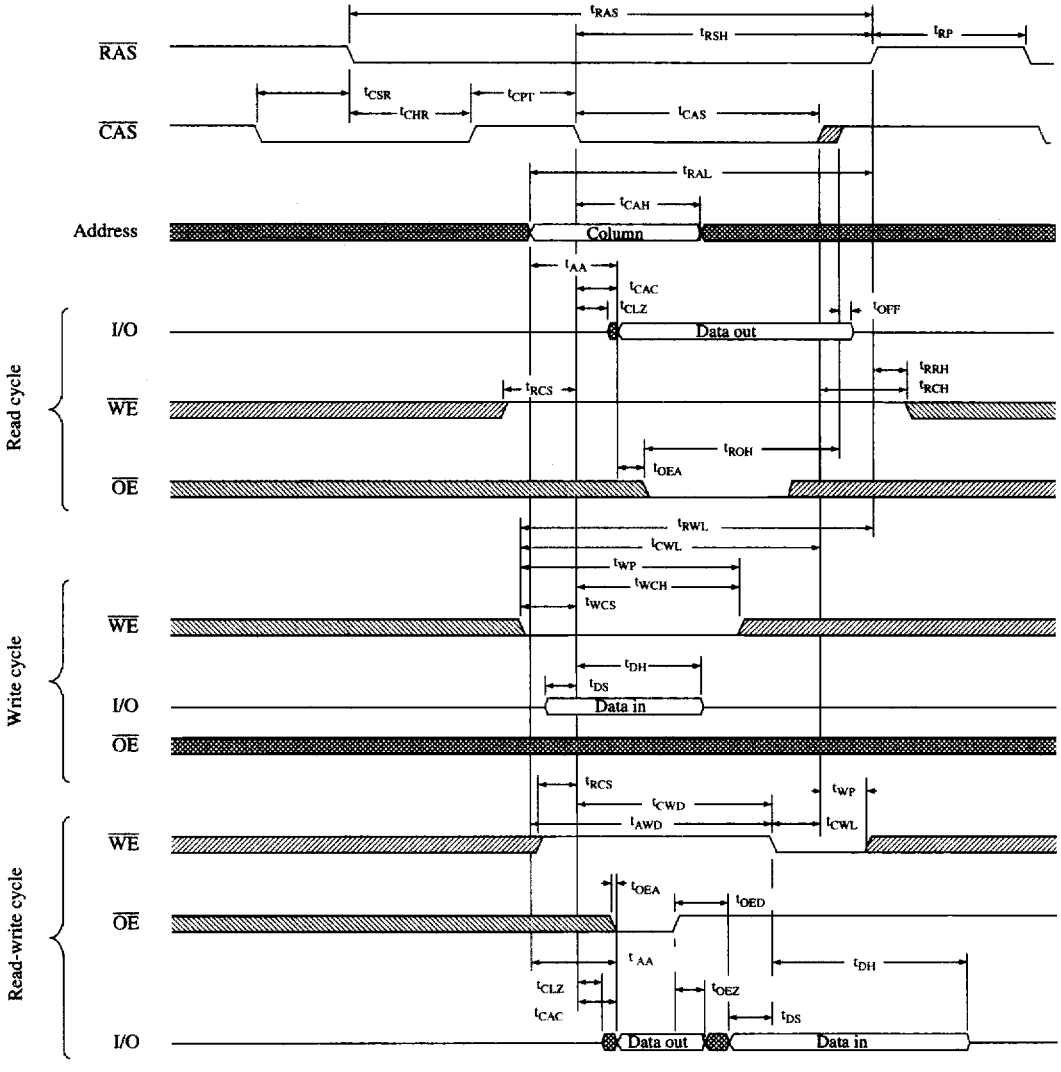
Hidden refresh waveform (read)



Hidden refresh waveform (write)

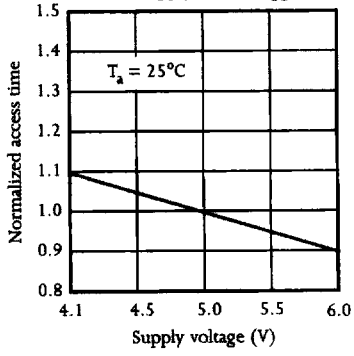


$\overline{CAS}$ before $\overline{RAS}$ refresh counter test waveform

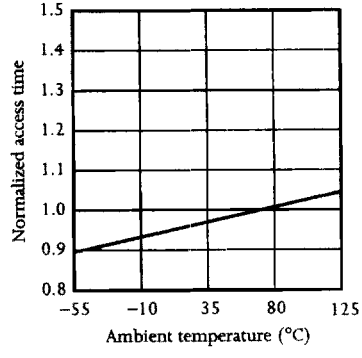


Typical DC and AC characteristics

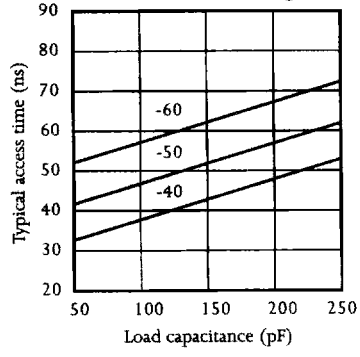
Normalized access time t_{RAC} vs. supply voltage V_{CC}



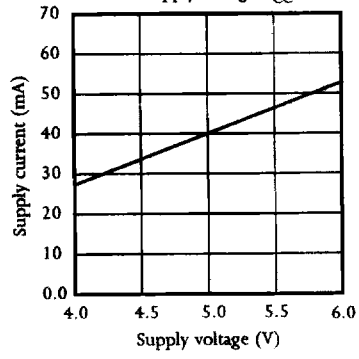
Normalized access time t_{RAC} vs. ambient temperature T_a



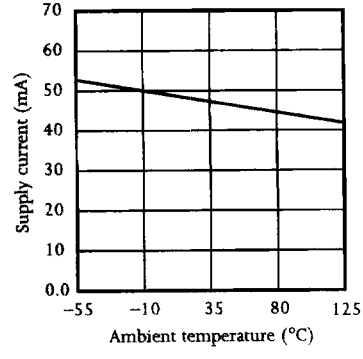
Typical access time t_{RAC} vs. load capacitance C_L



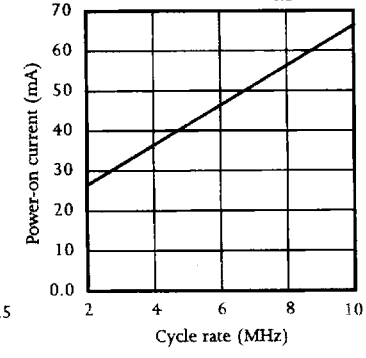
Typical supply current I_{CC} vs. supply voltage V_{CC}



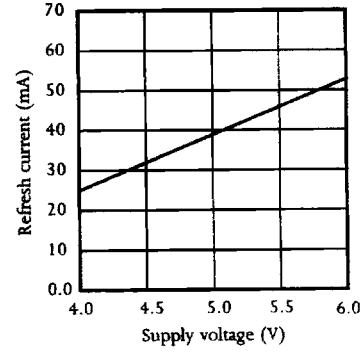
Typical supply current I_{CC} vs. ambient temperature T_a



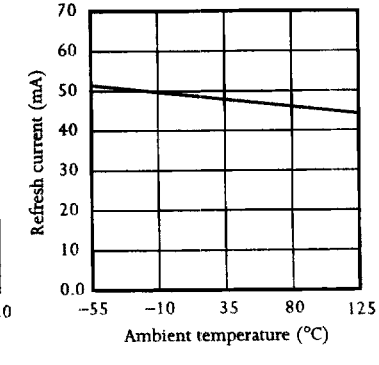
Typical power-on current I_{PO} vs. cycle rate $1/t_{RC}$



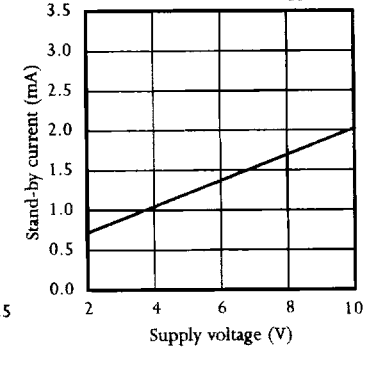
Typical refresh current I_{CC3} vs. supply voltage V_{CC}



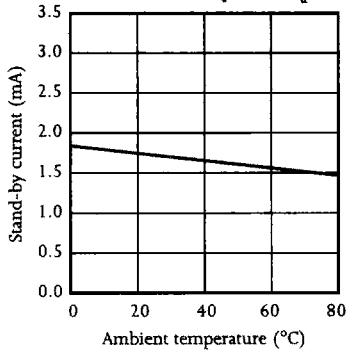
Typical refresh current I_{CC3} vs. ambient temperature T_a



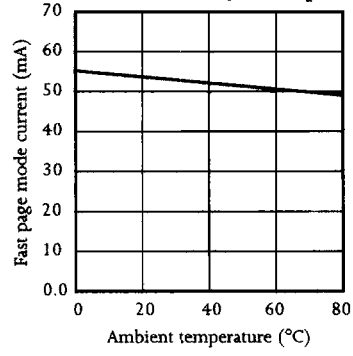
Typical TTL stand-by current I_{CC2} vs. supply voltage V_{CC}



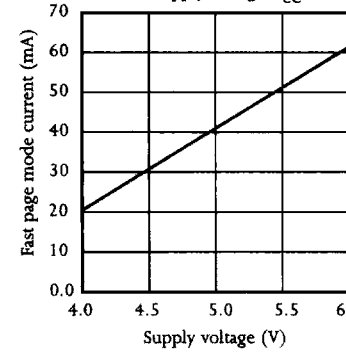
Typical TTL stand-by current I_{CC2} vs. ambient temperature T_a



Typical fast page mode current I_{CC4} vs. ambient temperature T_a



Typical fast page mode current I_{CC4} vs. supply voltage V_{CC}



Capacitance

($f = 1$ MHz, T_a = Room temperature)

Parameter	Symbol	Signals	Test conditions	Max	Unit
Input capacitance	C_{IN1}	A0 to A8	$V_{in} = 0V$	5	pF
	C_{IN2}	$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{OE}$	$V_{in} = 0V$	7	pF
I/O capacitance	$C_{I/O}$	I/O0 to I/O3	$V_{in} = V_{out} = 0V$	7	pF

AS4C14400 ordering codes

Package \ RAS access time	50 ns	60 ns
Plastic SOJ, 300 mil, 20/26-pin	AS4C14400-50JC	AS4C14400-60JC
Plastic TSOP, 300 mil, 20/26-pin	AS4C14400-50TC	AS4C14400-60TC

AS4C14400 part numbering system

AS4C	14400	-XX	X	C
DRAM Prefix	Device number	$\overline{RAS}$ access time	Package: J = SOJ 300 mil, T = TSOP 300 mil	Commercial temperature range, 0°C to 70 °C

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