SONY

CXD2027Q/R

DBS Audio Signal Processor

Description

The CXD2027Q/R are audio signal processors designed for DBS applications. These LSIs perform all digital processing from QPSK demodulation to analog audio output on a single chip.

Features

QPSK and PCM demodulators and DAC output are configured on a single chip.

Descrambler interface according to the COATEC system and SkyPort system .

Functions

QPSK demodulator
- Carrier, clock and data regeneration
- ALC and VCXO adjustment-free

PCM demodulator
- Frame sync protection by correlation detection
- De-interleaving and descrambling
- BCH error correction, range bit error correction
- Audio data range control
  - Expansion from 10 to 14 bits in A mode
  - Upper bit majority correction in B mode
- Control sign integration correction, chargeable flag integration correction by master frame synchronization
- Interface output for external DAC
- Digital interface output

1-bit DAC output
- Quadruple oversampling filter
- Digital de-emphasis circuit
- 1-bit stereo DAC with 2nd-order $\Delta\Sigma$ format noise shaper
  - S/N ratio : 90dB (Typ.)
  - Distortion : 0.011% (Typ.)

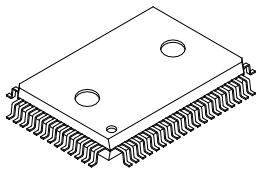
CPU interface
- I^2C bus

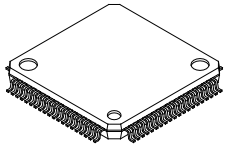
Descrambler interface
- COATEC system, SkyPort system

Mute functions
- Error occurrence frequency detection mute
- Audio chargeable flag detection mute
- Control sign (B7) detection mute

CXD2027Q
64 pin QFP (Plastic)

CXD2027R
80 pin LQFP (Plastic)





Structure

Silicon gate CMOS IC

Applications

TVs, VCRs with built-in BS tuners

Absolute Maximum Ratings (Ta = 25°C, Vss = 0V)

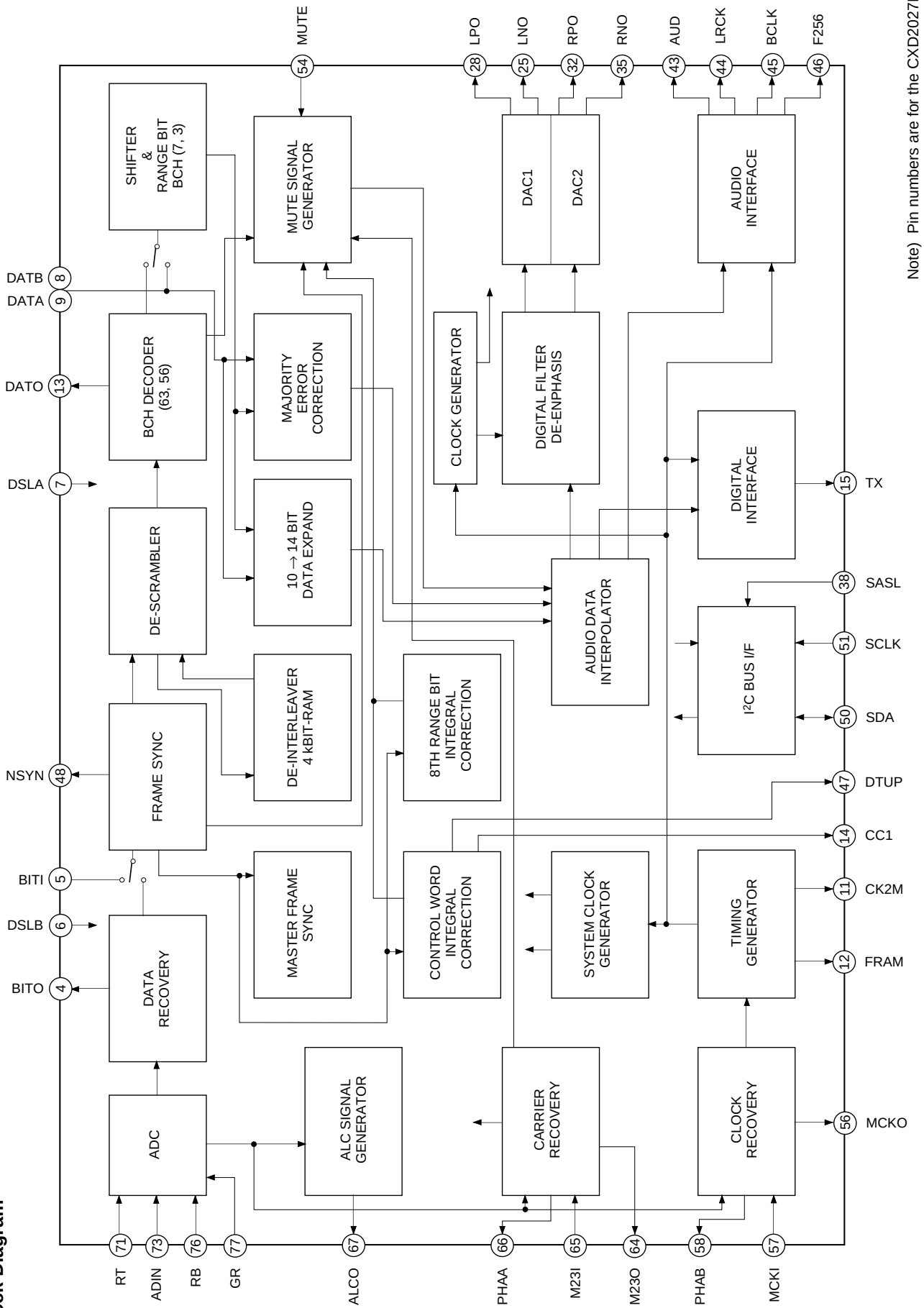
• Supply voltage	V_{DD}	Vss – 0.5 to +7.0	V
• Input voltage	V_I	Vss – 0.5 to V_{DD} + 0.5	V
• Output voltage	V_O	Vss – 0.5 to V_{DD} + 0.5	V
• Storage temperature	Tstg	–55 to +150	°C

Operating Conditions

• Supply voltage	V_{DD}	4.75 to 5.25	V
• Operating temperature	Topr	–20 to +75	°C

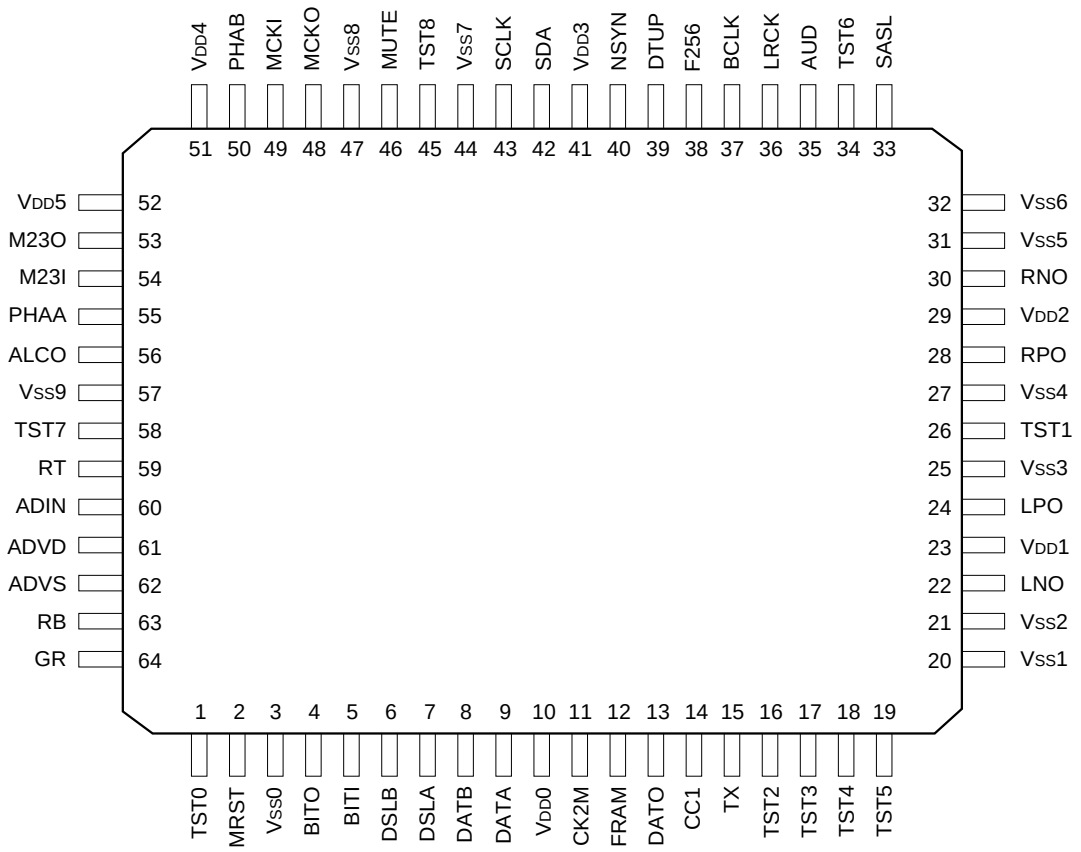
E94808-ST

Block Diagram

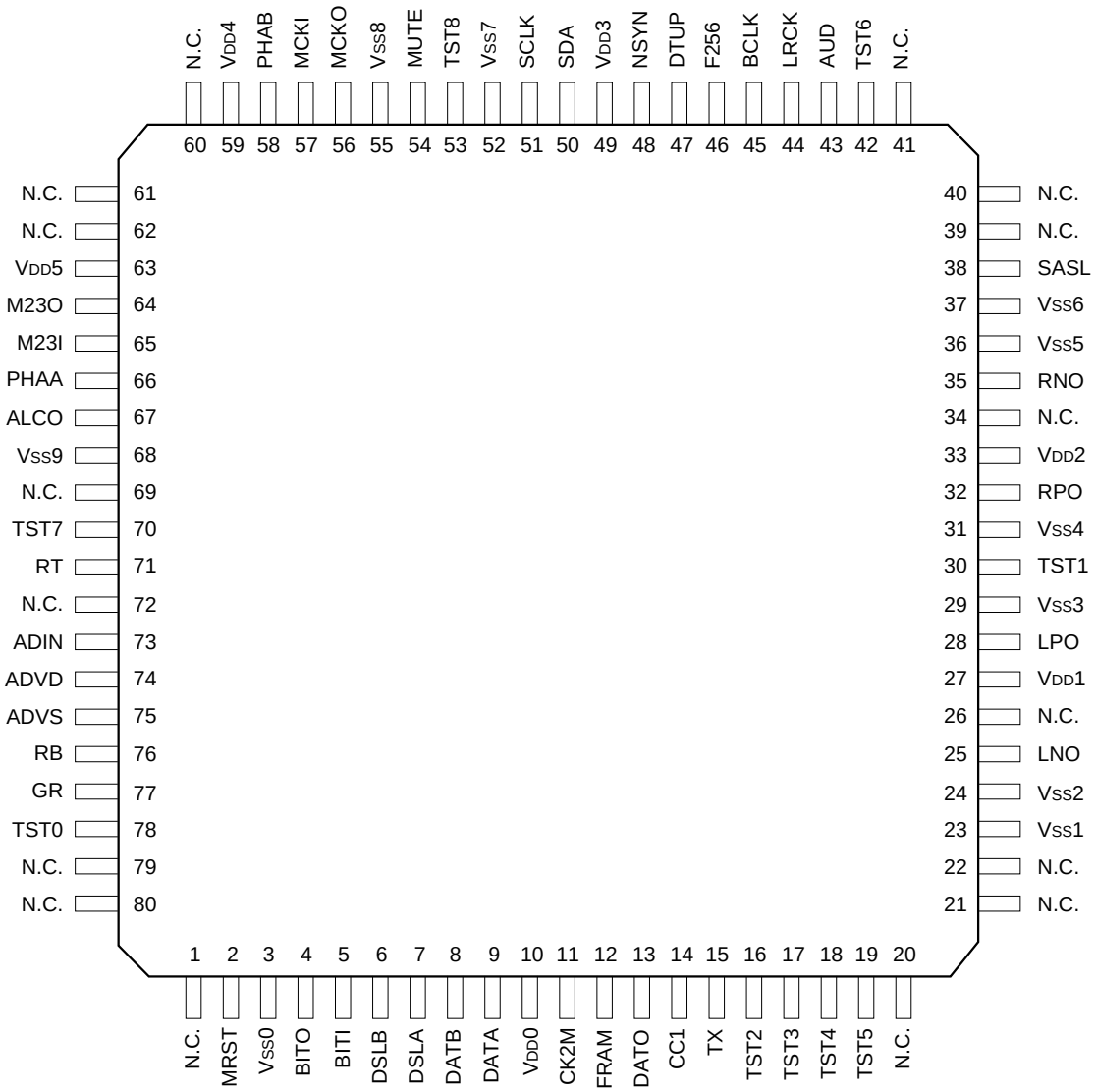


Note) Pin numbers are for the CXD2027R.

Pin Configuration 1
CXD2027Q



Pin Configuration 2
CXD2027R



Pin Description 1

CXD2027Q (64pin QFP)

Pin No.	Symbol	I/O	Pin Description	Remarks
1	TST0	I	Test pin; normally low	Internal pull down
2	MRST	I	Master reset; H: normal operation; L: reset	Internal pull up
3	V_{SS} Digital	—	Digital ground	
4	BITO	O	Bit stream output after PSK demodulation	
5	BITI	I	Bit stream input after PSK demodulation	TTL input
6	DSLB	I	External descrambler pin	TTL input
7	DSLA	I	External descrambler pin	TTL input
8	DATB	I	Data input 2 after BCH correction (for COATEC)	TTL input
9	DATA	I	Data input 1 after BCH correction (for SkyPort)	TTL input
10	V_{DD} Digital	—	Digital +5V power supply	
11	CK2M	O	2.048MHz clock output	
12	FRAM	O	Frame start bit flag	
13	DATO	O	Data output after BCH correction	
14	CC1	O	Control sign first bit output	
15	TX	O	Digital format audio output	
16	TST2	I	Test pin; normally low	Internal pull down
17	TST3	I	Test pin; normally low	Internal pull down
18	TST4	I	Test pin; normally low	Internal pull down
19	TST5	I	Test pin; normally high	
20	V_{SS} Digital	—	Digital ground	
21	V_{SS} D/A	—	Analog ground	
22	LNO	O	Lch D/A converter output	
23	V_{DD} D/A	—	Analog +5V power supply	
24	LPO	O	Lch D/A converter output	
25	V_{SS} D/A	—	Analog ground	
26	TST1	I	Test pin; normally low	Internal pull down
27	V_{SS} D/A	—	Analog ground	
28	RPO	O	Rch D/A converter output	
29	V_{DD} D/A	—	Analog +5V power supply	
30	RNO	O	Rch D/A converter output	
31	V_{SS} D/A	—	Analog ground	
32	V_{SS} Digital	—	Digital ground	
33	SASL	I	I^2C bus slave address select (L: D4, H: D6)	Internal pull down
34	TST6	I	Test pin; normally low	Internal pull down

Pin No.	Symbol	I/O	Pin Description	Remarks
35	AUD	O	Audio data output for external DF/DAC	
36	LRCK	O	LR clock output for external DF/DAC	
37	BCLK	O	Bit clock output for external DF/DAC	
38	F256	O	Clock output for external DF/DAC	
39	DTUP	O	CCUP: control sign update flag / DED: BCH 2 error detection	Switched by I^2C bus
40	NSYN	O	Asynchronous flag (H: asynchronous; L: synchronous)	
41	V_{DD} Digital	—	Digital +5V power supply	
42	SDA	I	SDA (I^2C bus)	I^2C bus compatible
43	SCLK	I	SCL (I^2C bus)	I^2C bus compatible
44	V_{SS} Digital	—	Digital ground	
45	TST8	I	Test pin; normally low	
46	MUTE	I	External forced muting input	TTL input
47	V_{SS} Digital	—	Digital ground	
48	MCKO	O	MCKI inversion output	
49	MCKI	I	24.576MHz clock input	
50	PHAB	O	Clock regeneration phase error data output	
51	V_{DD} Digital	—	Digital +5V power supply	
52	V_{DD} Digital	—	Digital +5V power supply	
53	M23O	O	M23I inversion output	
54	M23I	I	22.909088MHz clock input	
55	PHAA	O	Carrier regeneration phase error data output	
56	ALCO	O	ALC A/D control output	
57	V_{SS} Digital	—	Digital ground	
58	TST7	I	Test pin; normally low	
59	RT	I	A/D converter VRT input	
60	ADIN	I	Analog data input	
61	V_{DD} A/D	—	Analog +5V power supply	
62	V_{SS} A/D	—	Analog ground	
63	RB	I	A/D converter VRB input; connect to analog ground	
64	GR	I	A/D converter VGR input; connect to analog ground	

Pin Description 2

CXD2027R (80pin LQFP)

Pin No.	Symbol	I/O	Pin Description	Remarks
1	N.C.	—	Non-connection	
2	MRST	I	Master reset; H: normal operation; L: reset	Internal pull up
3	V_{SS} Digital	—	Digital ground	
4	BITO	O	Bit stream output after PSK demodulation	
5	BITI	I	Bit stream input after PSK demodulation	TTL input
6	DSLB	I	External descrambler pin	TTL input
7	DSLA	I	External descrambler pin	TTL input
8	DATB	I	Data input 2 after BCH correction (for COATEC)	TTL input
9	DATA	I	Data input 1 after BCH correction (for SkyPort)	TTL input
10	V_{DD} Digital	—	Digital +5V power supply	
11	CK2M	O	2.048MHz clock output	
12	FRAM	O	Frame start bit flag	
13	DATO	O	Data output after BCH correction	
14	CC1	O	Control sign first bit output	
15	TX	O	Digital format audio output	
16	TST2	I	Test pin; normally low	Internal pull down
17	TST3	I	Test pin; normally low	Internal pull down
18	TST4	I	Test pin; normally low	Internal pull down
19	TST5	I	Test pin; normally high	
20	N.C.	—	Non-connection	
21	N.C.	—	Non-connection	
22	N.C.	—	Non-connection	
23	V_{SS} Digital	—	Digital ground	
24	V_{SS} D/A	—	Analog ground	
25	LNO	O	Lch DAC output	
26	N.C.	—	Non-connection	
27	V_{DD} D/A	—	Analog +5V power supply	
28	LPO	O	Lch DAC output	
29	V_{SS} D/A	—	Analog ground	
30	TST1	I	Test pin; normally low	Internal pull down
31	V_{SS} D/A	—	Analog ground	
32	RPO	O	Rch DAC output	
33	V_{DD} D/A	—	Analog +5V power supply	
34	N.C.	—	Non-connection	

Pin No.	Symbol	I/O	Pin Description	Remarks
35	RNO	O	Rch D/A converter output	
36	$V_{SS\ D/A}$	—	Analog ground	
37	$V_{SS\ Digital}$	—	Digital ground	
38	SASL	I	I^2C bus slave address select (L: D4, H: D6)	Internal pull down
39	N.C.	—	Non-connection	
40	N.C.	—	Non-connection	
41	N.C.	—	Non-connection	
42	TST6	I	Test pin; normally low	Internal pull down
43	AUD	O	Audio data output for external DF/DAC	
44	LRCK	O	LR clock output for external DF/DAC	
45	BCLK	O	Bit clock output for external DF/DAC	
46	F256	O	Clock output for external DF/DAC	
47	DTUP	O	CCUP: control sign update flag/DED: BCH 2 error detection	Switched by I^2C bus
48	NSYN	O	Asynchronous flag (H: asynchronous; L: synchronous)	
49	$V_{DD\ Digital}$	—	Digital +5V power supply	
50	SDA	I	SDA (I^2C bus)	I^2C bus compatible
51	SCLK	I	SCL (I^2C bus)	I^2C bus compatible
52	$V_{SS\ Digital}$	—	Digital ground	
53	TST8	I	Test pin; normally low	
54	MUTE	I	External forced muting input	TTL input
55	$V_{SS\ Digital}$	—	Digital ground	
56	MCKO	O	MCKI inversion output	
57	MCKI	I	24.576MHz clock input	
58	PHAB	O	Clock regeneration phase error data output	
59	$V_{DD\ Digital}$	—	Digital +5V power supply	
60	N.C.	—	Non-connection	
61	N.C.	—	Non-connection	
62	N.C.	—	Non-connection	
63	$V_{DD\ Digital}$	—	Digital +5V power supply	
64	M23O	O	M23I inversion output	
65	M23I	I	22.909088MHz clock input	
66	PHAA	O	Carrier regeneration phase error data output	
67	ALCO	O	ALC A/D control output	
68	$V_{SS\ Digital}$	—	Digital ground	
69	N.C.	—	Non-connection	
70	TST7	I	Test pin; normally low	

Pin No.	Symbol	I/O	Description	Remarks
71	RT	I	A/D converter VRT input	
72	N.C.	—	Non-connection	
73	ADIN	I	Analog data input	
74	$V_{DD\ A/D}$	—	Analog +5V power supply	
75	$V_{SS\ A/D}$	—	Analog ground	
76	RB	I	A/D converter VRB input; connect to analog ground	
77	GR	I	A/D converter VGR input; connect to analog ground	
78	TST0	I	A/D test pin; normally low	Internal pull down
79	N.C.	—	Non-connection	
80	N.C.	—	Non-connection	

Absolute Maximum Ratings (Ta = 25°C, Vss = 0V)

Item	Symbol	Ratings	Unit
Supply voltage	V_{DD}	Vss – 0.5 to +7.0	V
Input voltage	V_I	Vss – 0.5 to V_{DD} + 0.5	V
Output voltage	V_O	Vss – 0.5 to V_{DD} + 0.5	V
Operating temperature	Topr	–20 to +75	°C
Storage temperature	Tstg	–55 to +150	°C

I/O Pin Capacitance (V_{DD} = V_I = 0V, f = 1MHz)

Item	Symbol	Min.	Typ.	Max.	Unit	Corresponding pins
Input pin capacitance	C_{IN}			9	pF	*1
				10		*2
				11		*3
Output pin capacitance	C_{OUT}			11		*4
Input/output pin capacitance	$C_{I/O}$			10		*5

*1 Input pins other than *2 and *3

*2 SCLK

*3 BITI, DSLB, DSLA, DATB, DATA, TST5

*4 All output pins

*5 SDA

Electrical Characteristics

[DC characteristics] (V_{DD} = 5V ± 0.25V, Vss = 0V, Ta = –20 to +75°C)

Item		Symbol	Measurement conditions	Min.	Typ.	Max.	Unit	Corresponding pins
Power consumption		P_D	V_{DD} = 4.75 to 5.25V	180	280	350	mW	
Input/output voltage		V_I, V_O		Vss		V_{DD}	V	*1
Input voltage	CMOS input	V_{IH}		0.7V_{DD}			V	*2
		V_{IL}				0.3V_{DD}		
	TTL input	V_{IH}		2.2				*3
		V_{IL}				0.8		
	High level	V_{t+}		0.7V_{DD}				*4
	Low level	V_{t-}				0.3V_{DD}		
	Hysteresis voltage	$V_{t+} - V_{t-}$			0.5			
Input rise/fall time		tr, tf		0		500	ns	*5
Output voltage		V_{OH}	I_{OH} = –2mA	V_{DD} – 0.8			V	*6
		V_{OL}	I_{OL} = 4mA			0.4		
		V_{OH}	I_{OH} = –4mA	V_{DD} – 0.8				*7
		V_{OL}	I_{OL} = 4mA			0.4		
		V_{OH}	I_{OH} = –4mA	V_{DD} – 0.8				*8
		V_{OL}	I_{OL} = 8mA			0.4		
		V_{OL}	I_{OL} = 3mA	0		0.4		*9
		V_{OL}	I_{OL} = 6mA	0		0.6		

*1 All pins

*2 Input pins other than *3 and *4

*3 BITI, DSLB, DSLA, DATB, DATA, MUTE

*4 SDA, SCLK

*5 All input pins

*6 Output pins other than *7, *8 and *9

*7 LNO, LPO, RPO, RNO

*8 BITO, CK2M, FRAM, DATO, CCI, TX

*9 SDA, SCLK

Item		Symbol	Measurement conditions	Min.	Typ.	Max.	Unit	Corresponding pins
Input leak current	Normal input pin	II	V_{IN} = V_{SS} or V_{DD}	–10		10	µA	*1
	With pull-up resistor	IIL	V_{IN} = V_{SS}	–40	–100	–240	µA	*2
	With pull-down resistor	IIH	V_{IN} = V_{DD}	40	100	240	µA	*3
	Bidirectional pin (during input state)	II	V_{IN} = V_{SS} or V_{DD}	–40		40	µA	*4
Output leak current (I^2C bus)		IOZ	V_{IN} = V_{SS}	–10		–10	µA	*5

*1 Input pins other than *2, *3 and *4

*2 MRST

*3 TST0, TST1, TST2, TST3, TST4, SASL, TST6

*4 BITI, DSLB, DSLA, DATB, DATA, TST5

*5 SDA, SCLK

[Oscillation cell electrical characteristics] (V_{DD} = 5V ± 0.25V, Ta = –20 to +75°C)

Item	Symbol	Measurement conditions	Min.	Typ.	Max.	Unit	Corresponding pins
Logic threshold value	LVth			V_{DD}/2		V	
Input voltage	V_{IH}		0.7V_{DD}			V	*6
	V_{IL}				0.3V_{DD}	V	
Feedback resistance	R_{FB}	V_{IN} = V_{SS} or V_{DD}	250k	1M	2.5M	Ω	*7
Output voltage	V_{OH}	I_{OH} = –12mA	V_{DD}/2			V	*8
	V_{OL}	I_{OL} = 12mA			V_{DD}/2		

*6 MCKI, M23I

*7 MCKI, MCKO, M23I, M23O

*8 MCKO, M23O

[Internal A/D converter characteristics]

Absolute Maximum Ratings (Ta = 25°C)

Item	Symbol	Ratings	Unit
Supply voltage	AV_D	+7.0	V
Input voltage (analog)	AIN	AV_D to AV_S	V
Input voltage (digital)		V_{DD} to V_{SS}	V
Reference voltage	RB, RT	AV_D to AV_S	V

Operating Conditions

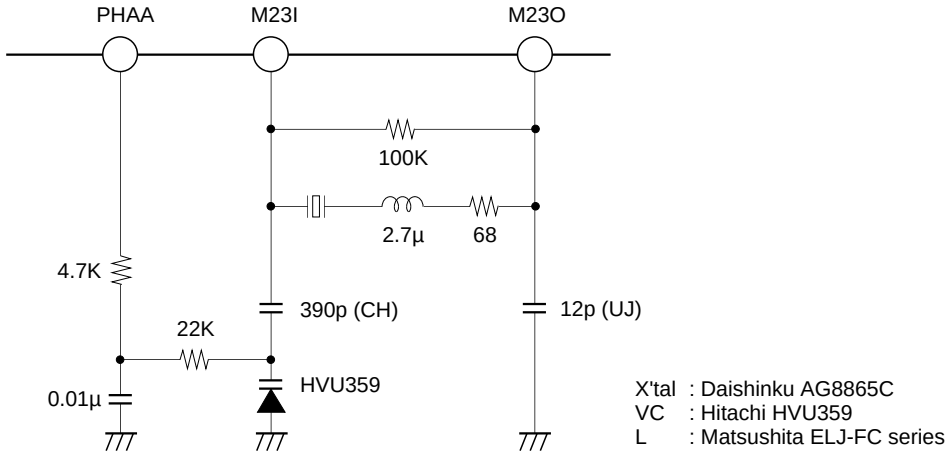
Item	Symbol		Ratings	Unit
Supply voltage	AV_D, AV_S		4.75 to 5.25	V
	l DV_S – AV_S l		0 to 100	mV
Reference input voltage	RB		0 to	V
	RT		to 3.75	
Analog input	AIN	Amplitude	100 to 300 (typ. 200)	mV_{p-p}
		DC level	typ.1.25	V
Operating ambient temperature	Topr		–20 to +75	°C

[AC characteristics] (V_{DD} = 5.0V ± 0.25V, Ta = 25°C)

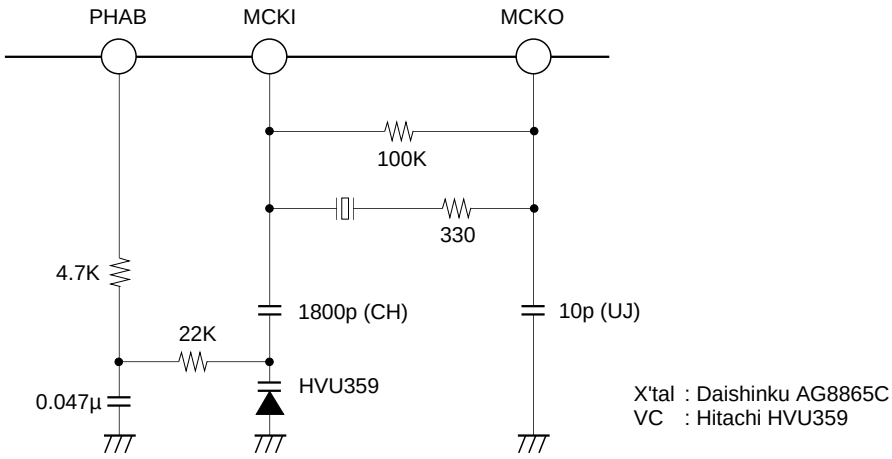
Item	Conditions		Min.	Typ.	Max.	Unit
ALC characteristics	Deviation from standard input level 200mVp-p				±50	%
Carrier regeneration PLL pull-in range	Pull-in frequency* relative to 5.7272MHz. Includes temperature characteristics (–20 to +75°C) and supply voltage fluctuation (±5%) of VCXO.	Upper	+750			Hz
		Lower	–450			
Clock regeneration PLL pull-in range	Pull-in frequency* relative to 2.048MHz. Includes temperature characteristics (–20 to +75°C) and supply voltage fluctuation (±5%) of VCXO.	Upper	+300			Hz
		Lower	–100			

* Performance guaranteed only when using constants of the recommended oscillation circuit.

22.909088MHz (for carrier regeneration PLL) VCXO circuit



24.576MHz (for clock regeneration PLL) VCXO circuit

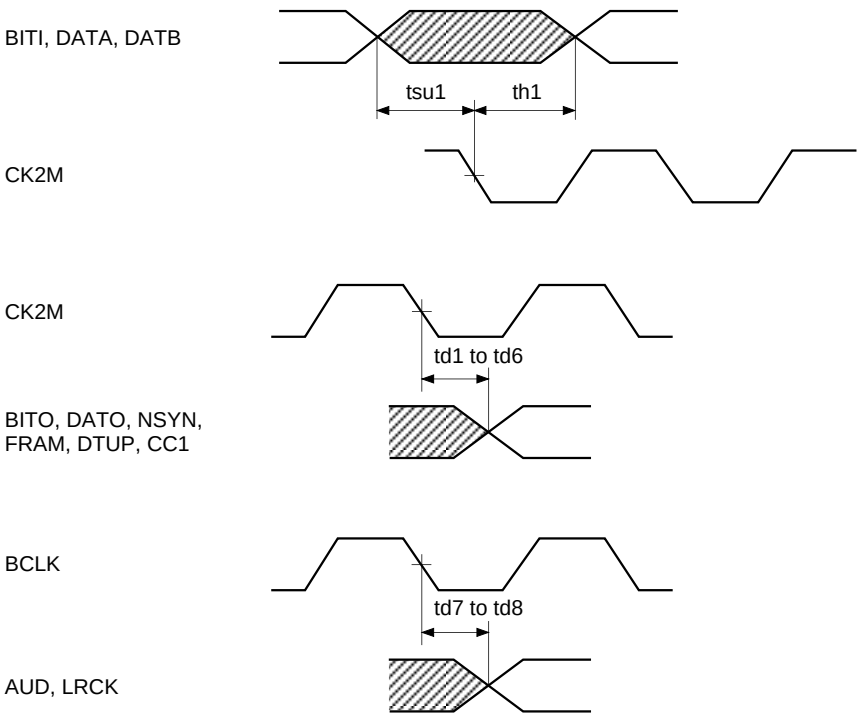


(V_{DD} = 5.0V ± 0.25V, Ta = –20 to +75°C, C_L = 60pF)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
BITI set-up time	tsu1	Value relative to CK2M fall	32			ns
DATA set-up time						
DATB set-up time						
BITI hold time	th1	Value relative to CK2M fall	0			ns
DATA hold time						
DATB hold time						

(V_{DD} = 5.0V ± 0.25V, Ta = –20 to +75°C, C_L = 60pF)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
BITO delay time	td1	Value relative to CK2M fall			17	ns
DATO delay time	td2				24	ns
NSYN delay time	td3				37	ns
FRAM delay time	td4				23	ns
DTUP delay time	td5				38	ns
CC1 delay time	td6				21	ns
AUD delay time	td7	Value relative to BCLK fall			28	ns
LRCK delay time	td8				26	ns



Internal 1-bit DAC analog characteristics

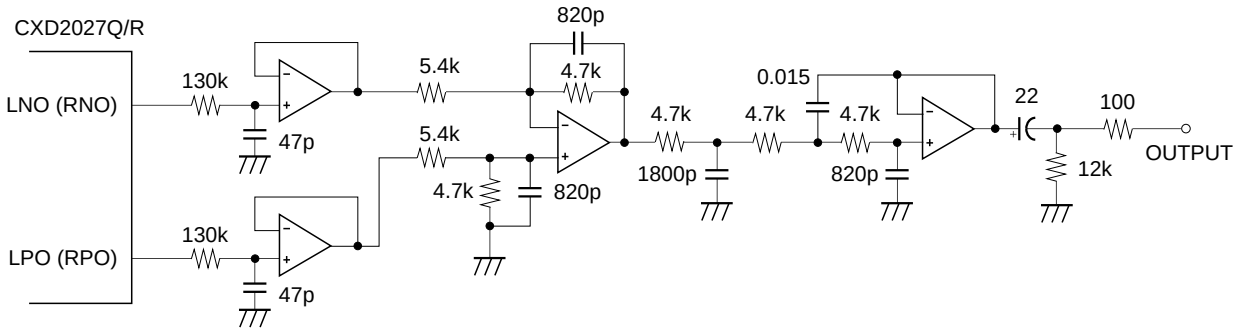
(fs = 48kHz, V_{DD} = 5.0V, Ta = 25°C, signal frequency = 1kHz, measurement band = 4Hz to 20kHz, B mode)

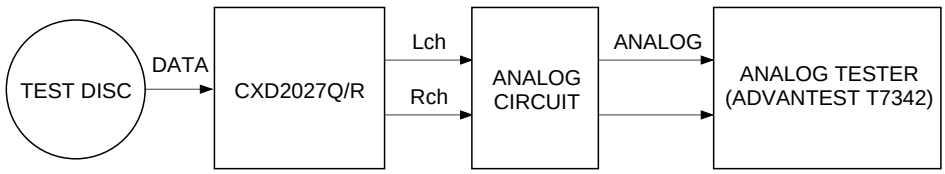
Item	Min.	Typ.	Max.	Unit	Remarks
S/N		90		dB	(EIAJ) *1
THD + N		0.011		%	(EIAJ)
Output level		1.95		V(rms)	*2

*1 "A" characteristic weighting filter used

*2 When master clock is 256fs

The following circuit is used for analog characteristics measurement.





Description of Functions

- **ALC**

  This detects the fluctuation of the input QPSK modulated signal level and absorbs the fluctuation by controlling A/D VRT. With this function, a signal is output from ALCO after PWM modulation, and should be fed back to the RT pin after integration.

- **Carrier regeneration**

  A 5.727272MHz carrier is regenerated.

  The input QPSK modulated signal is A/D converted at a sample rate of 22.909088MHz (5.727272MHz × 4), and control voltage is generated using that sampling position as phase error data. The control voltage is output from the PHAA pin after PWM modulation, and controls VCXO, which consists of an internal oscillation cell and external crystal.

- **Clock regeneration**

  This is a PLL circuit with 24.576MHz clock. It is 512 × fs, for use with the DAC.

  Phase comparison is carried out using the regenerated I and Q signals and VCXO divided output, and control voltage is generated. After PWM modulation, the control voltage is output from the PHAB pin, and controls VCXO, which consists of an internal oscillation cell and external crystal.

- **Data regeneration**

  A 2.048MHz bit stream is regenerated from the regenerated I and Q signals.

- **Frame sync and master frame sync**

  Correlated detection and competitive counter format is used for sync protection. The number of rear protection is set at three times, and that of front protection is set at 3, 5, 7, or 9 times.

  Also, synchronizing to the master frame can be done when the master frame signal is being sent to the control sign 14th bit. In this case, the number of rear protection is set to 2 times, and that of front protection is set at 7, 9 or 11 times.

- **Descramble**

  A superimposed PN signal is removed for BS.

  Also, there is a built-in interface for an external descrambler unit.

- **De-interleave**

  The data interleaved by the built-in 4kbit SRAM is returned to the correct data array.

- **(63, 56) BCH sign error correction**

  This performs (63, 56) BCH sign error correction. Error capability is 1 error correction, 2 errors detection.

- **Range bit BCH sign error correction**

  This performs (7, 3) BCH sign error correction. Error capability is 1 error correction, 2 errors detection.

  When there are 2 errors, the previous value is held.

• **Control sign integration detection and 8th range bit integration detection**

Integration detection is carried out in units of 15 frames. When a match of 12/15 or more is obtained, a defined control sign is detected. However, updating is every 18 frames.

When a match of 12/15 or more is not obtained, the previous value is held.

Further, synchronizing to the master frame can be done when the master frame signal is being sent to the control sign 14th bit.

After integration detection, the control sign and range bit can be read by the I^2C bus.

• **10 → 14 bit data expansion**

During A mode, the instantaneously compressed 10 bits of audio data are expanded to 14 bits according to the range expansion rule. The lower bits of data are fixed at a set value during expansion, and the data is treated as 16 bits.

• **Upper bit majority detection**

During B mode, this carries out upper bit majority detection and protects the upper bits.

• **Mute signal generation**

This performs muting by the external MUTE signal and internal logic, and also generates a mute signal according to the mute setting from the I^2C bus.

• **Audio data interpolation**

This receives the bit error detection signal and interpolation indication signal from majority detection, and then carries out the average value interpolation or the previous value hold.

• **Clock generation for D/A converter**

This generates the clock for the DAC.

• **Digital filter (DF) and de-emphasis**

A 2ch 1-bit DAC with 2nd-order $\Delta\Sigma$ format noise shaper of quadruple oversampling filter is built in.

The output format is differential.

De-emphasis function corresponding to the mode is also built in.

• **Audio interface**

One of the following three output formats can be selected.

1) SONY: bit clock 32 fs/ MSB first/ 16 bits (for built-in D/A converter)
2) IIS: SONY format 1 BCLK delay
3) Bit clock 64fs / MSB first / 16 bits rearward truncation

• **Digital interface**

Conforms to the following digital audio interface format: type II form I (for consumer digital audio equipment)

• **I^2C bus interface**

Control by microcomputer is carried out by the I^2C bus I/F.

The slave address can be switched by controlling SASL; for low: D4, for high: D6.

• Output channel selection

The output channels provided are analog output for built-in D/A converter Lch/Rch, one output system for external D/A audio output and one for digital audio output. Channel selection can be done easily through the I^2C bus.

Unused channels can be suppressed using the I^2C bus.

• Audio output selection

Mode selection can be carried out via the I^2C bus.

• Zero cross muting

The I^2C bus can be used for zero cross muting.

When a mute signal is input, muting is not carried out until zero cross conditions are satisfied for 1 frame.

If these conditions are not met for 1 frame, muting is forced at the next frame.

Zero cross mute cancel is performed in frame units.

The conditions for zero cross are a change in audio data MSB, or when audio data value is between 00ffh and ff00h.

• Description of mute function

A signal is treated as a mute signal in the following cases:

1) when asynchronous
2) control sign 7th bit (non-broadcast flag) or 16th bit (audio suppression flag) is high
3) 8th range bit (audio chargeable flag) is high (however, only channel for high)
4) number of double error flags goes over a certain TH level (error frequency detection mute)
5) audio carrier (5.7272MHz) can not be detected
6) an I^2C bus mute flag is up
7) for other than audio

1. Asynchronous flag mute

   Muting is applied when an asynchronous state exists. Also, the number of front sync protection can be changed among 3, 5, 7 or 9 times by the I^2C bus, so the conditions for asynchronous flag muting can be changed.

2. Muting by control sign 7th and 16th bits

   The control sign 7th bit is a flag indicating broadcast or non-broadcast. If this bit is high, muting is applied. Also, the I^2C bus can be used so that this bit does not apply muting.

   The control sign 16th bit audio suppression flag is used when broadcast channels are switched and when transmission modes are switched. Both use the value after integration detection.

3. Chargeable flag detection mute

   The 8th range bit indicates if audio data is for a chargeable broadcast or not. For a chargeable broadcast, a flag ("H") goes up in that bit's position. When this bit is high, the broadcast is detected as chargeable and muting is applied. Further, the I^2C bus can be used for each channel so that this bit does not apply muting. The value after every 18 frames of integration detection is used.

4. Error frequency detection mute
   Muting is applied after BCH (63, 56) sign error correction is executed for every 64 data, when the number of double error detection flags goes over a certain TH (threshold value) level during a certain number of frames. Also, the I²C bus can be used so that muting is not applied. The setting values are indicated below.
   Number of frames: 128, 256, 512, 1024
   Up to 32 double errors can be detected in one frame, so 1/16, 1/8, 1/4 and 1/2 of the maximum detections for each frame number are set as the TH levels.
   Therefore, there are 16 possible combinations, and the value is set by the I²C bus.
   The TH level for muting cancel is half of the TH value when muting is applied; in other words, 1/32, 1/16, 1/8 and 1/4, respectively.

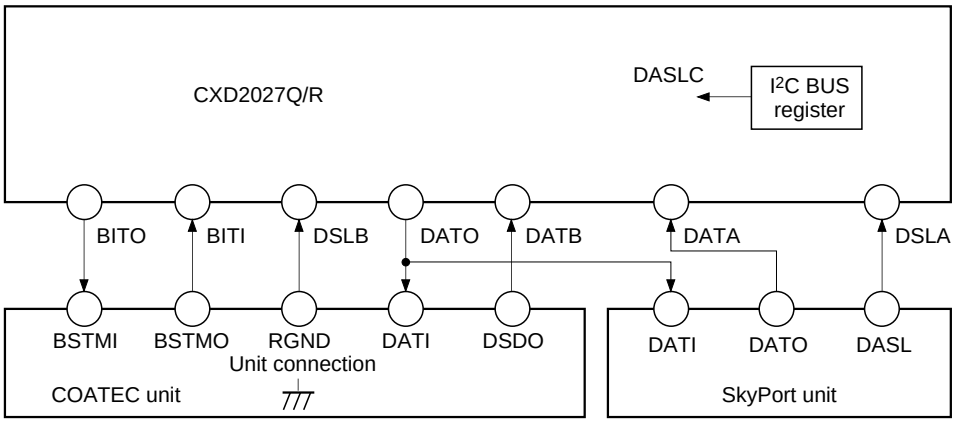
5. Carrier detection mute
   When the BS broadcast audio carrier frequency of 5.7272MHz can not be detected by the PSK demodulator unit, muting is applied. Also, the I²C bus can be used so that muting is not applied.

6. I²C bus muting
   The I²C bus can apply forced muting to analog and AUD outputs. TX output is locked to analog output.

7. Muting other than audio
   Muting is done for other than audio mode when the control sign 2nd and 3rd, or 4th and 5th bits are "H, H".

External descramble I/F circuit example

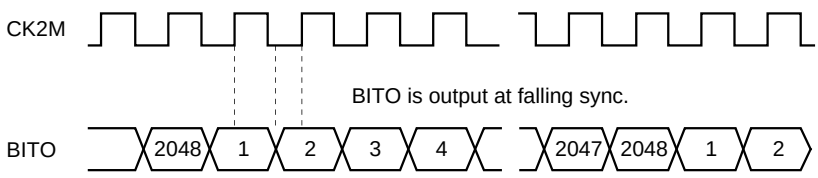
COATEC and SkyPort units can be connected simultaneously.



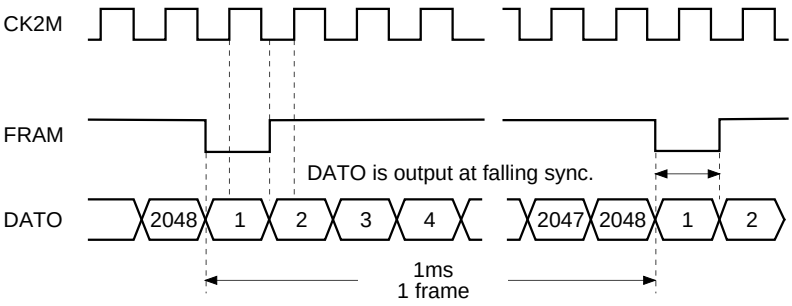
DSLA	DSLB	Descramble format
0	0	COATEC, SkyPort *
0	1	SkyPort
1	0	COATEC
1	1	Internal

* The COATEC unit and SkyPort unit can be connected simultaneously.
However, use the I²C bus to set DASLC at high when turning off the COATEC unit power supply.

Bit stream signal interface



Data interface after BCH error correction

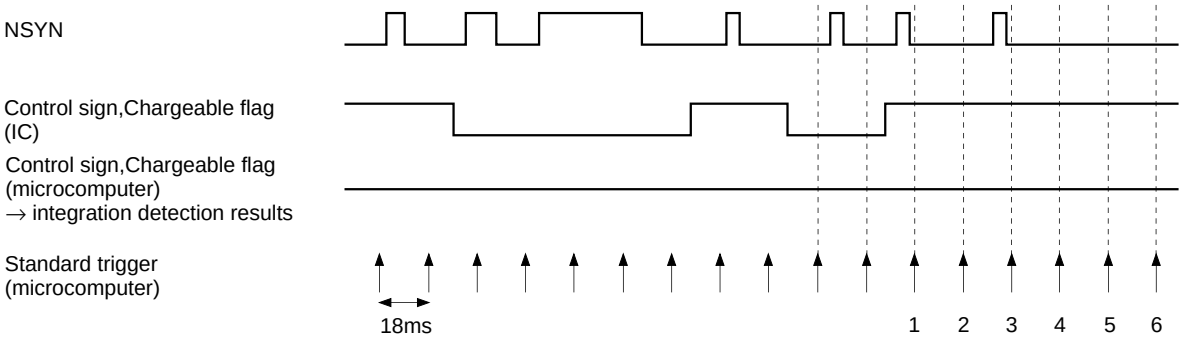


Examples of error detection countermeasures for low C/N control sign and chargeable flag integration detection

When C/N is low, NSYN frequently goes high level (asynchronous state).

In this case, problems such as wrong display or wrong detection of control sign 7th bit "broadcast/non-broadcast" flag may occur due to incorrect integration detection. This can be improved using the microcomputer software shown below.

Integration detection result can be updated only when NSYN is low level. Detection results of this IC are read by the standard trigger of the microcomputer, and if the result values match for 5 to 6 times continuously, the detection result is taken as an update for the system. It is also possible to update the integration detection result by the continuous matching of 7 times or more. However, standard trigger cycle of the microcomputer must be set about 18ms.



Description of I²C bus

The I²C bus is a bidirectional serial bus system developed by Philips. It can transmit and receive data between multiple devices using two lines, SCLK (Serial Clock) and SDA (Serial Data).

This LSI has a built-in I²C bus interface circuit and is compatible with slave RECEIVER and slave TRANSMITTER operation modes.

For the transfer configuration, both RECEIVER mode and TRANSMITTER mode have sub-addresses.

RECEIVER mode

The first byte is the slave address, the second byte is the sub-address, and data is read at the third byte and after. Continuous data reading is also possible. After transmission of the first byte, the sub-address is made (+1) automatically.

TRANSMITTER mode

The first byte is the slave address, and data is sent at the second byte and after. Continuous data output is also possible. After transmission of the first byte, the sub-address is made (+1) automatically.
When there is no verification answer from the master, the SDA line is released.

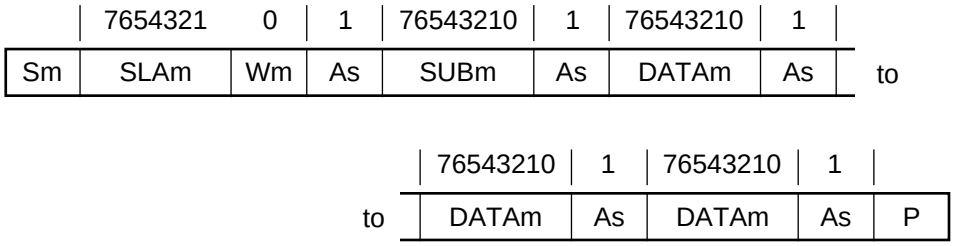
To read data, the sub-address for the data to be read is written in RECEIVER mode, then the data is read in TRANSMITTER mode.

The SDA line is released for initial reset, so the bus is not occupied. Also, even if the IC supply voltage falls to 0V, the bus is not occupied. Nonetheless, please keep within the absolute maximum ratings.

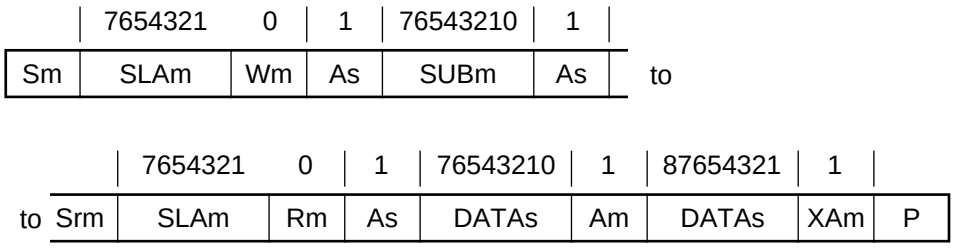
This bus is compatible not only with standard mode (maximum 100kbit/s) but with high speed mode (maximum 400kbit/s) as well.

• **Specifications**

Data write (RECEIVER mode)



Data read (RECEIVER mode & TRANSMITTER mode)



Symbol	Description
*m	from master to slave
*s	from slave to master
S	Start Condition
Sr	Start Condition
P	Stop Condition
SLA	Slave Address
SUB	Sub Address
DATA	Data
W	0 : Write Master → Slave
R	1 : Read Slave → Master
A	Clock pulse for Acknowledgement (SDA: L)
XA	Acknowledgement none (SDA:H)

I²C bus control table

SASL	L	H
Slave address	D4	D6

R/W	Sub-address	MSB			Data				LSB
		bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
WR	00'H	A1S1	A1S2	A1S3		A2S1	A2S2	A2S3	
	01'H					DOS1	DOS2	DOS3	
	02'H	BUSMT1	BUSMT2	AMUTE	SIG	MTOF0	MTOF1	MTOF2	MTOF3
	03'H	OTSTP1	OTSTP2	OTSTP3	OTSTP4	NF1	NF2	TH1	TH2
	04'H	DASLC	C1SL	LRSL	IIS	BLFS	FPCC	FPCB	(TEST1)
	05'H					C2	C10	XPRT	DOMU
	06'H	(TSB0)	(TSB1)	XEOFF	XINH	PI1	PI2	NR	
	07'H	RGOF1	RGOF2	RGOF3	RGOF4	OTSL	MFRAM	(TEST2)	(TEST3)
RD	00'H	CC1	CC2	CC3	CC4	CC5	CC6	CC7	CC8
	01'H	CC9	CC10	CC11	CC12	CC13	CC14	CC15	CC16
	02'H	(L)	(L)	(L)	(L)	RG81	RG82	RG83	RG84

Blanks : Data not related to internal logic.
( ) : Data for testing. Fix to the default value.
(L) : Low is output.
MSB, LSB : Data is transmitted with MSB first.

Default data (default value of internal register after master reset)

W	Sub-address	MSB			Data				LSB
		bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
WR	00'H	0	1	0	—	0	1	0	—
	01'H	—	—	—	—	0	1	0	—
	02'H	0	0	1	0	1	1	1	1
	03'H	0	0	0	0	0	1	0	1
	04'H	0	0	0	0	1	0	1	(0)
	05'H	—	—	—	—	1	1	0	0
	06'H	(0)	(0)	1	0	0	0	0	—
	07'H	1	1	1	1	0	0	(0)	(0)

( ) : Always fix to the default value.

• **BUS setting values for audio output selection**

Sub-address 00'H 00000000'B

BIT No.	Name	Description
bit7	A1S1	Audio output mode selection when using built-in DF/DAC
bit6	A1S2	
bit5	A1S3	
bit3	A2S1	Audio output mode selection when using external DF/DAC
bit2	A2S2	
bit1	A2S3	

Applications				A1S1	A1S2	A1S3
				A2S1	A2S2	A2S3
				DOS1	DOS2	DOS3
stereo	A mode		TV	0	X	X
			independent	1	X	X
	B mode			X	X	X
2ch mono	A mode	TV	main + sub	0	1	X
			main	0	0	0
			sub	0	0	1
		independent	main + sub	1	1	X
			main	1	0	0
			sub	1	0	1
	B mode		main + sub	X	1	X
			main	X	0	0
			sub	X	0	1
1ch mono	A mode	TV	main	0	X	X
		independent	main	1	X	X
	B mode		main	X	X	X

Sub-address 01'H 00000001'B

BIT No.	Name	Description
bit3	DOS1	Output mode selection when using digital interface
bit2	DOS2	
bit1	DOS3	

Same setting method as for A1S1, A1S2 and A1S3

• **Muting-related BUS setting values**

Sub-address 02'H 00000010'B

BIT No.	Name	Description	H	L
bit7	BUSMT1	Audio data mute when using built-in DF/DAC	ON	OFF
bit6	BUSMT2	Audio data mute when using external DF/DAC	ON	OFF
bit3	MTOF0	Carrier detection mute	ON	OFF
bit2	MTOF1	Non-broadcast flag mute	ON	OFF
bit1	MTOF2	Error occurrence frequency mute	ON	OFF
bit0	MTOF3	External mute (EXMU)	ON	OFF

Sub-address 03'H 00000011'B

BIT No.	Name	Description	H	L
bit7	OTSTP1	Signal suppression for external DF/DAC (AUD, LRCK, BCLK)	Non-operation	Operation
bit6	OTSTP2	Signal suppression for external descramble (CK2M, FRAM, DATO)	Non-operation	Operation
bit5	OTSTP3	Control sign output suppression (NSYN, CCUP, CC1)	Non-operation	Operation
bit4	OTSTP4	Built-in DF/DAC operation / non-operation selection	Non-operation	Operation
bit3	NF1	Error occurrence frequency mute setting (number of frames)		
bit2	NF2			
bit1	TH1	Error occurrence frequency mute setting (threshold value)		
bit0	TH2			

bit3	bit2	Number of frames
NF1	NF2	
0	0	128
0	1	256
1	0	512
1	1	1024

bit1	bit0	Threshold value	
TH1	TH2	MUTE*1	Cancel*2
0	0	1/2	1/4
0	1	1/4	1/8
1	0	1/8	1/16
1	1	1/16	1/32

*1 MUTE when over this value

*2 MUTE cancel when below this value

• BUS setting values for chargeable flag mute

Sub-address 07'H 00000111'B

BIT No.	Name	Description	H	L
bit7	RGOF1	Audio 1ch mute	ON	OFF
bit6	RGOF2	Audio 2ch mute	ON	OFF
bit5	RGOF3	Audio 3ch mute	ON	OFF
bit4	RGOF4	Audio 4ch mute	ON	OFF
bit2	MFRAM	Master frame sync processing	OFF	ON
bit1	TEST2	For testing (fix to low)		
bit0	TEST3	For testing (fix to low)		

• BUS setting values for external I/F, etc.

Sub-address 02'H 00000010'B

BIT No.	Name	Description	H	L
bit4	SIG	Signal polarity selection for external descramble I/F	Inverted	Positive

Corresponding input pins : BITI, DATA, DATB

Corresponding output pins : CK2M, DATO, FRAM

Sub-address 04'H 00000100'B

BIT No.	Name	Description	H	L
bit7	DASLC	External descramble I/F control	Refer to page 20.	
bit6	C1SL	CC1 (control sign 1st bit) output polarity inversion	Inverted	Positive
bit5	LRSL	LRCK polarity inversion	Inverted	Positive
bit4	IIS	Audio output format switching		
bit3	BLFS			
bit2	FPCC	Selection of the number of front protection for frame sync protection and master frame syncprotection selection		
bit1	FPCB			
bit0	TEST1	For testing (fix to low)		

bit4	bit3	Format
IIS	BLFS	
1	1	Prohibited
1	0	2) IIS
0	1	3) 64fs
0	0	1) SONY

bit2	bit1	The number of frame sync front protection	The number of master frame sync front protection
FPCC	FPCB		
1	1	3	7
1	0	5	9
0	1	7	11
0	0	9	11

Sub-address 07'H 00000111'B

BIT No.	Name	Description	H	L
bit3	OTSL	DTUP pin output signal switching	DED	CCUP

• Digital I/F BUS setting values

Sub-address 05'H 00000101'B

BIT No.	Name	Description	H	L
bit3	C2	Digital copy allowed/prohibited selection	Allowed	Prohibited
bit2	C10	Channel status 10th bit	General	BS
bit1	XPRT	Parity inversion selection for digital interface	Transmission error	Normal
bit0	DOMU	Mute for digital interface (TX is DC low)	ON	OFF

• DF and D/A converter-related BUS setting values

Write register
Sub-address 06'H 00000110'B

BIT No.	Name	Description	H	L
bit7	TSB0	For testing (normally set to low regardless of input data)		
bit6	TSB1			
bit5	XEOFF	Digital de-emphasis selection	ON	OFF
bit4	XINH	DC dither selection	ON	OFF
bit3	PI1	DC dither phase control Rch	Inverted	Positive
bit2	PI2	DC dither phase control Lch	Inverted	Positive
bit1	NR	Modulation NR	ON	OFF

• Control sign bit reading after integration correction

Sub-address 00'H 00010000'B

BIT No.	Name	Description	
bit7	CC1	Control sign 1st bit	Mode selection
bit6	CC2	Control sign 2nd bit	TV audio
bit5	CC3	Control sign 3rd bit	
bit4	CC4	Control sign 4th bit	Additional audio
bit3	CC5	Control sign 5th bit	
bit2	CC6	Control sign 6th bit	Suppression backup
bit1	CC7	Control sign 7th bit	Broadcast identification
bit0	CC8	Control sign 8th bit	Expansion bit

Sub-address 01'H 00010001'B

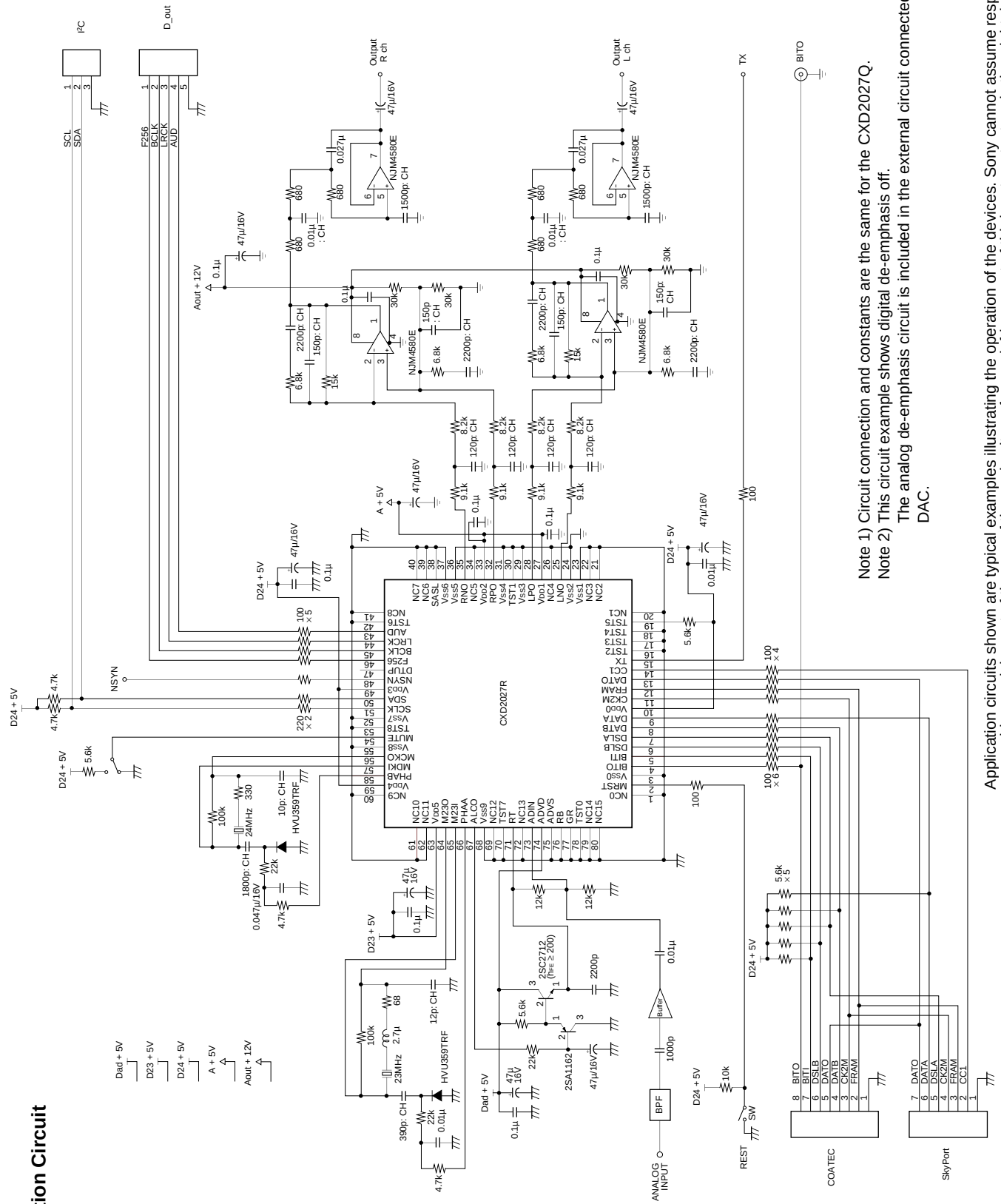
BIT No.	Name	Description	
bit7	CC9	Control sign 9th bit	Expansion bits
bit6	CC10	Control sign 10th bit	
bit5	CC11	Control sign 11th bit	
bit4	CC12	Control sign 12th bit	Video scramble existent/non-existent
bit3	CC13	Control sign 13th bit	—
bit2	CC14	Control sign 14th bit	Master frame sync flag H: asynchronous, L: synchronous
bit1	CC15	Control sign 15th bit	Data suppression
bit0	CC16	Control sign 16th bit	Audio output suppression

• **Range 8th bit read after integration correction**

Sub-address 02'H 00010010'B

BIT No.	Name	Description
bit7	—	Low level fixed output
bit6	—	
bit5	—	
bit4	—	
bit3	RG81	Range 8th bit (chargeable flag) 1ch
bit2	RG82	Range 8th bit (chargeable flag) 2ch
bit1	RG83	Range 8th bit (chargeable flag) 3ch
bit0	RG84	Range 8th bit (chargeable flag) 4ch

Application Circuit



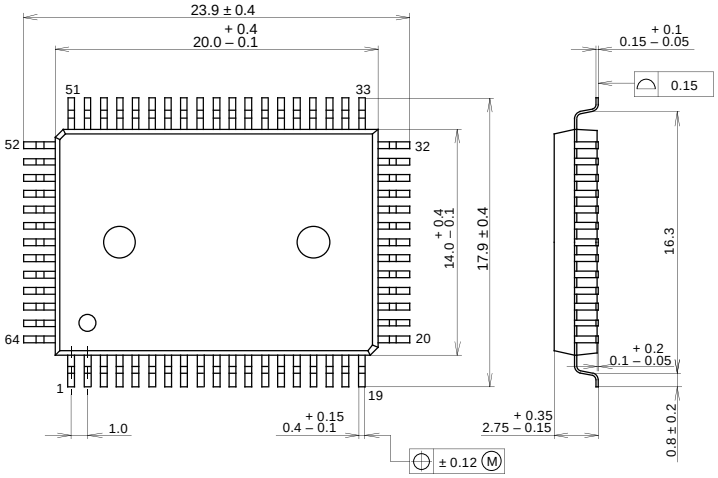
Note 1) Circuit connection and constants are the same for the CXD2027Q.
Note 2) This circuit example shows digital de-emphasis off.
The analog de-emphasis circuit is included in the external circuit connected to the built-in DAC.

Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to the same.

Package Outline Unit: mm

CXD2027Q

64PIN QFP(PLASTIC)



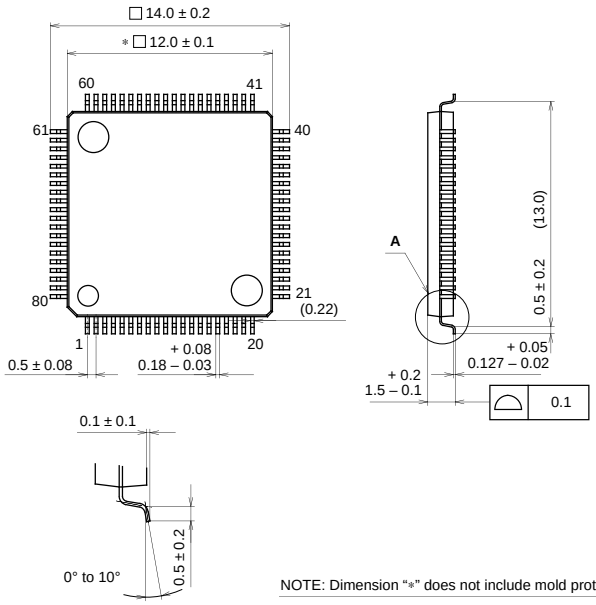
PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER/PALLADIUM PLATING
LEAD MATERIAL	COPPER /42 ALLOY
PACKAGE WEIGHT	1.5g

SONY CODE	QFP–64P–L01
EIAJ CODE	*QFP064–P–1420
JEDEC CODE	————

CXD2027R

80PIN LQFP (PLASTIC)



NOTE: Dimension "*" does not include mold protrusion.

DETAIL **A**

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY / PHENOL RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	42 ALLOY
PACKAGE WEIGHT	0.5g

SONY CODE	LQFP-80P-L01
EIAJ CODE	*QFP080-P-1212-A
JEDEC CODE	————