

**M52034SP/FP**

STANDARD PLL VIF/SIF

**DESCRIPTION**

The M52034SP/FP is a semiconductor integrated circuit consisting of IF signal processing for VCR and CTV tuners. The circuit realizes PLL detection system with same application as conventional quasi-synchronous VIF/SIF ICs. The circuit includes VIF amplifier, video detector, VCO, APC detector, AFT, SIF detector, IF/RF AGC, SIF limiter and FM detector.

The package is of 20-pin plastic molded shrink. Flat package is also available.

**FEATURES**

- Low power dissipation is realized by 5V PLL detector. ( $V_{cc}=5.0V$ ,  $I_{cc}=30mA$ )
- A full synchronous detector circuit using PLL as video detector provides excellent DG, DP, 920kHz beat and cross color characteristics.
- Dynamic AGC realizes high speed response with only single filter. 12V power supply can be used for RF AGC and AFT outputs.
- It is optimum for VCR and color TV sets with video output terminals due to the built-in equalizer amplifier.

**APPLICATION**

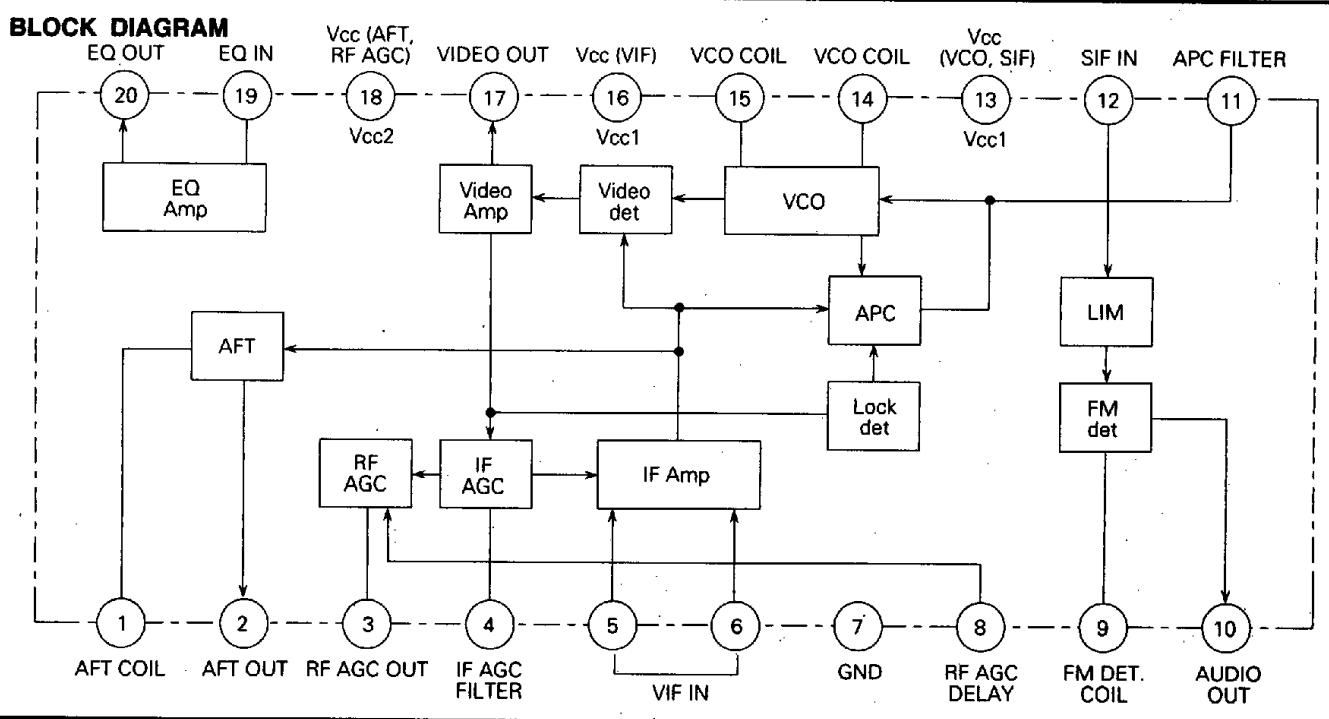
CTV, VCR

**RECOMMENDED OPERATING CONDITION**

Supply voltage range ..... 4.5~5.5V  
 Rated supply voltage ..... 5.0V

**PIN CONFIGURATION (TOP VIEW)**

AFT COIL	1	EQ OUT	20
AFT OUT	2	EQ IN	19
RF AGC OUT	3	Vcc (AFT, RF AGC)	18
IF AGC FILTER	4	VIDEO OUT	17
VIF IN	5	Vcc (VIF)	16
VIF IN	6	VCO COIL	15
GND	7	VCO COIL	14
RF AGC DELAY	8	Vcc (VCO,SIF)	13
FM DET. COIL	9	SIF IN	12
AUDIO OUT	10	APC FILTER	11

Outline 20P4B (SP)  
20P2N-A (FP)

## ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Ratings								Unit
Vcc1	Supply voltage 1	7								V
Vcc2	Supply voltage 2	14								V
Pd	Power dissipation	1000								mW
Topr	Operating temperature	-20~75								°C
Tstg	Storage temperature	-40~125								°C
Surge	Electrostatic discharge	±200								V

## ELECTRICAL CHARACTERISTICS (Ta=25°C, Vcc=5V, Vcc=12V, unless otherwise noted)

Symbol	Parameter	Test point	Test circuit	Input		Test conditions						Limits			Unit		
				VIF	SIF	1	2	3	4	5	6	V4	V8	Min.	Typ.	Max.	
Icc	Circuit current	A	1	-	-	2	1	1	1	1	1	-	-	25.0	36.0	47.0	mA
V17	Video detector output DC voltage 1	TP7	1	-	-	1	1	1	2	1	1	1	-	2.8	3.1	3.4	V
V20	Video detector output DC voltage 2	TP9	1	-	-	1	1	1	2	1	1	1	-	3.2	3.5	3.8	V
V0det1	Video detector output 1	TP7	1	SG 1	-	1	1	1	1	1	1	-	-	0.70	0.95	1.20	Vp-p
V0det2	Video detector output 2	TP9	1	SG 1	-	1	1	1	1	1	1	-	-	1.50	1.93	2.40	Vp-p
P/N	Video S/N	TP8	1	SG 2	-	1	1	1	1	1	1	-	-	48.0	54.0	-	dB
BW	Video frequency characteristics	TP7	1	SG 3	-	1	1	1	1	1	1	-	-	5.5	6.2	-	MHz
Vin (min)	Input sensitivity	TP7	1	SG 4	-	1	1	1	1	1	1	-	-	-	45	52	dB $\mu$
Vin (max)	Maximum allowable input	TP7	1	SG 5	-	1	1	1	1	1	1	-	-	102	108	-	dB $\mu$
GR	AGC control range	-	1	-	-	-	-	-	-	-	-	-	-	50	63	-	dB
V4H	IF AGC maximum voltage	TP3	1	-	-	1	1	1	1	1	1	-	-	3.5	4.6	-	V
V4	IF AGC voltage (80 dB $\mu$ )	TP3	1	SG 6	-	1	1	1	1	1	1	-	-	1.9	2.4	2.9	V
V4L	IF AGC minimum voltage (120 dB $\mu$ )	TP3	1	SG 7	-	1	1	1	1	1	1	-	-	-	0.0	0.2	V
V2	AFT output voltage	TP1	1	-	-	1	1	1	2	1	1	0	-	3.0	5.0	6.9	V
$\mu$	AFT detector sensitivity	TP1	1	SG10	-	1	1	1	1	1	1	-	-	40	56	78	mV/kHz
V2H	AFT maximum voltage	TP1	1	SG10	-	1	1	1	1	1	1	-	-	11.4	11.8	-	V
V2L	AFT minimum voltage	TP1	1	SG10	-	1	1	1	1	1	1	-	-	-	0.1	0.5	V
V3H	RF AGC maximum voltage	TP2	1	SG 2	-	1	1	1	1	1	1	-	2	10.8	11.6	-	V
V3L	RF AGC minimum voltage	TP2	1	SG 2	-	1	1	1	1	1	1	-	6	-	0.1	1.0	V
DG	DG	TP7	1	SG16	-	1	1	1	1	1	1	-	-	-	3	5	%
DP	DP	TP7	1	SG16	-	1	1	1	1	1	1	-	-	-	2	5	deg
CL-U	Capture range (U)	TP7	1	SG11	-	1	1	1	1	1	1	-	-	0.45	0.84	-	MHz
CL-L	Capture range (L)	TP7	1	SG11	-	1	1	1	1	1	1	-	-	1.70	2.78	-	MHz
CL-T	Capture range (T)	TP7	1	-	-	1	1	1	1	1	1	-	-	2.15	3.62	-	MHz
FC1	EQ frequency characteristics 1	TP7 TP9	1	SG12	-	1	1	1	1	1	1	-	-	3.5	6.0	8.5	dB
FC2	EQ frequency characteristics 2	TP7 TP9	1	SG13	-	1	1	1	1	1	1	-	-	6.6	9.0	11.5	dB
FC3	EQ frequency characteristics 3	TP7 TP9	1	SG14	-	1	1	1	1	1	1	-	-	8.7	11.0	13.3	dB
IM	Intermodulation	TP7	1	SG15	-	1	1	1	1	1	1	-	-	30	36	-	dB
Vsync	Pin 20 sync level	TP9	1	SG 2	-	1	1	1	1	1	1	-	-	1.0	1.3	1.6	V
Rin (V)	VIF input resistance		2	90dB $\mu$	-	-	-	-	-	-	-	-	-	-	1.2	-	KΩ
Cin (V)	VIF input capacitance		2	90dB $\mu$	-	-	-	-	-	-	-	-	-	-	2.3	-	PF
V10	AF output voltage	TP4	1	-	-	1	1	1	2	1	1	0	-	1.20	1.80	2.40	V

## ELECTRICAL CHARACTERISTICS (cont.)

Symbol	Parameter	Test point	Test circuit	Input		Test conditions							Limits			Unit	
				VIF	SIF	1	2	3	4	5	6	V4	V8	Min.	Typ.	Max.	
VoAF (Max)	Maximum AF output	TP4	1	—	SG17	1	1	1	2	1	1	0	—	141	202	263	mVrms
THD AF	AF output distortion	TP4	1	—	SG21	1	1	1	2	1	1	0	—	—	0.5	1.2	%
Vin (Lim)	Input limiting sensitivity	TP4	1	—	SG18	1	1	1	2	1	1	0	—	—	40	49	dBr
AMR	AMR	TP4	1	—	SG19	1	1	1	2	1	1	0	—	47	56	—	dB
S/N	AF S/N	TP4	1	—	SG20	1	1	1	2	1	1	0	—	54	68	—	dB

## ELECTRICAL CHARACTERISTICS TEST METHOD

## “P/N” : Video S/N

- Input SG2 in VIF IN.
- The noise appearing at pin 17 is determined by measuring the r.m.s. voltage at TP8 through low pass filter (-3dB at 5MHz).
- $P/N = 20 \log \left\{ \frac{V_{det} 1 (V_{p-p}) \times 0.7}{\text{Noise (V.r.m.s.)}} \right\}$

## “BW” : Video frequency characteristics

- Set SG3 as follows:  
 $f_1 = 58.75\text{MHz } V_i = 90\text{dB}\mu$  } Mixed Signal  
 $f_2 = 57.75\text{MHz } V_i = 70\text{dB}\mu$
- Measure the amplitude of 1MHz at TP7 and let it be V1.
- Decrease frequency f2 until the amplitude of (f1-f2) at TP7 reaches 3dB smaller than V1. Then, read frequency f2.  
 $BW = 58.75 - f_2(\text{MHz}) + 1\text{MHz}$

## “Vin (min)” : Input sensitivity

- Input SG4 in VIF IN.
- Decrease the SG4 level until the detector output level of pin 17 reaches 3dB smaller than Vdet1 and let the level be input sensitivity.

## “Vin (max)” : Maximum allowable input

- Set SG5 to 90dB $\mu$  and input it in VIF IN.
- Let the detector output of pin 17 be V2.
- Increase the SG5 voltage until the detector output level reaches 3dB smaller than V2 and let the voltage be maximum allowable input.

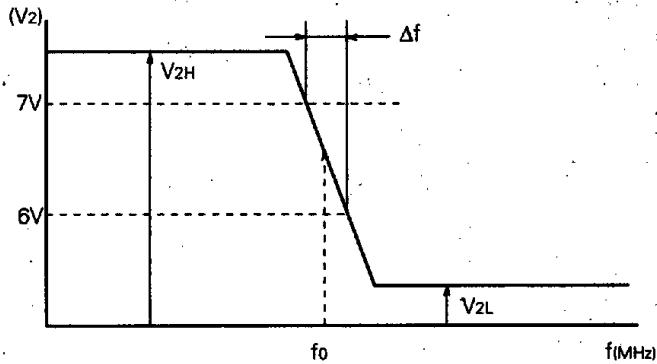
## “GR” : AGC control range

- AGC control range is defined as follows:  
 $GR = (\text{Maximum allowable input}) - (\text{Input sensitivity})$

“ $\mu$ ” : AFT detector sensitivity

- Input SG10 in VIF IN.
- Measure difference of frequency between 5V and 7V of DC voltage at TP1 and let it be  $\Delta f$ .
- AFT detector sensitivity is defined as follows:

$$\mu = \frac{2000(\text{mV})}{\Delta f(\text{kHz})} (\text{mV/kHz})$$



## “V2H” : AFT maximum voltage

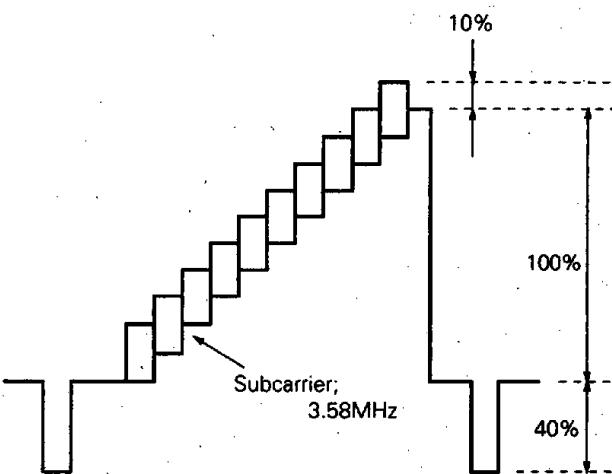
- Let maximum DC voltage in the above figure be V2H.

## “V2L” : AFT minimum voltage

- Let minimum DC voltage in the above figure be V2L.

## “DG, DP” : DG, DP

- Modulated waves of SG16 is generated by 87.5% video modulation of the 10-step waves shown in the figure below.
- At TP7, measure DG and DP with vectorscope.



**M52034SP/FP****STANDARD PLL VIF/SIF****"CL-u" : Capture range (u)**

- Input SG11 in VIF IN and increase the frequency until VCO lock is released.
- Decrease the frequency of SG11 and let the frequency at which VCO locks again be  $f_u$  (MHz).
- Capture range( $u$ )= $f_u - 58.75$  (MHz)

**"CL-L" : Capture range (L)**

- Input SG11 in VIF IN and decrease the frequency until VCO lock is released.
- Increase the frequency of SG11 and let the frequency at which VCO locks again be  $f_L$  (MHz).
- Capture range( $L$ )= $58.75 - f_L$  (MHz)

**"CL-T" : Capture range (T)**

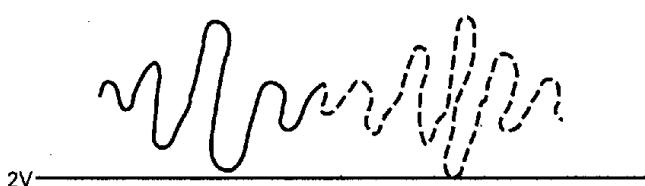
- "CL-T" = "CL-u" + "CL-L" (MHz)

**"FC1," "FC2," "FC3" : EQ frequency characteristics**

- Input SG12 in VIF IN.
- Measure the level of ( $f_1 - f_2$ ) at TP7 and let it be  $V_{EQ\ IN}$  (dB $\mu$ ).
- Measure the level of ( $f_1 - f_2$ ) at TP9 and let it be  $V_{EQ\ OUT}$  (dB $\mu$ ).
- EQ frequency characteristics are defined as follows:  
 $FC1 \sim 3 = V_{EQ\ OUT} - V_{EQ\ IN}$  (dB)

**"IM" : Intermodulation**

- Input SG15 in VIF IN.
- Observe TP7 with oscilloscope and adjust the voltage of  $V_4$  so that minimum level of detector output will come to 2V.
- Observe TP7 with spectrum analyzer and let the ratio of the 0.92MHz level to the 3.58MHz level be intermodulation.

**"Vin (lim)" : Input limiting sensitivity**

- Set SG18 to 80 dB $\mu$  and input it in SIF IN.
- Decrease the SG18 output level until the detector output of TP4 reaches 3dB smaller than  $V_{O\ AF\ MAX}$  and let the level be input limiting sensitivity.

**"AMR" : AMR**

- Input SG19 in SIF IN.
- Measure the output voltage at TP4 and let it be  $V_{AM}$ .
- AMR is defined as follows:

$$AMR = 20 \log \left\{ \frac{V_{O\ AF\ MAX}(mVr.m.s.)}{V_{AM}(mVr.m.s.)} \right\} (\text{dB})$$

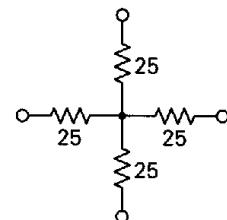
**"S/N" : AF S/N**

- Input SG20 in SIF IN.
- Measure the output voltage at TP4 and let it be  $V_N$ .
- AF S/N is defined as follows:

$$S/N = 20 \log \left\{ \frac{V_{O\ AF\ MAX}(mVr.m.s.)}{V_N(mVr.m.s.)} \right\} (\text{dB})$$

**Note :**

- Amplitude level of all AM modulated waves is the peak level of modulated waves.
- The following is used for the mixer.



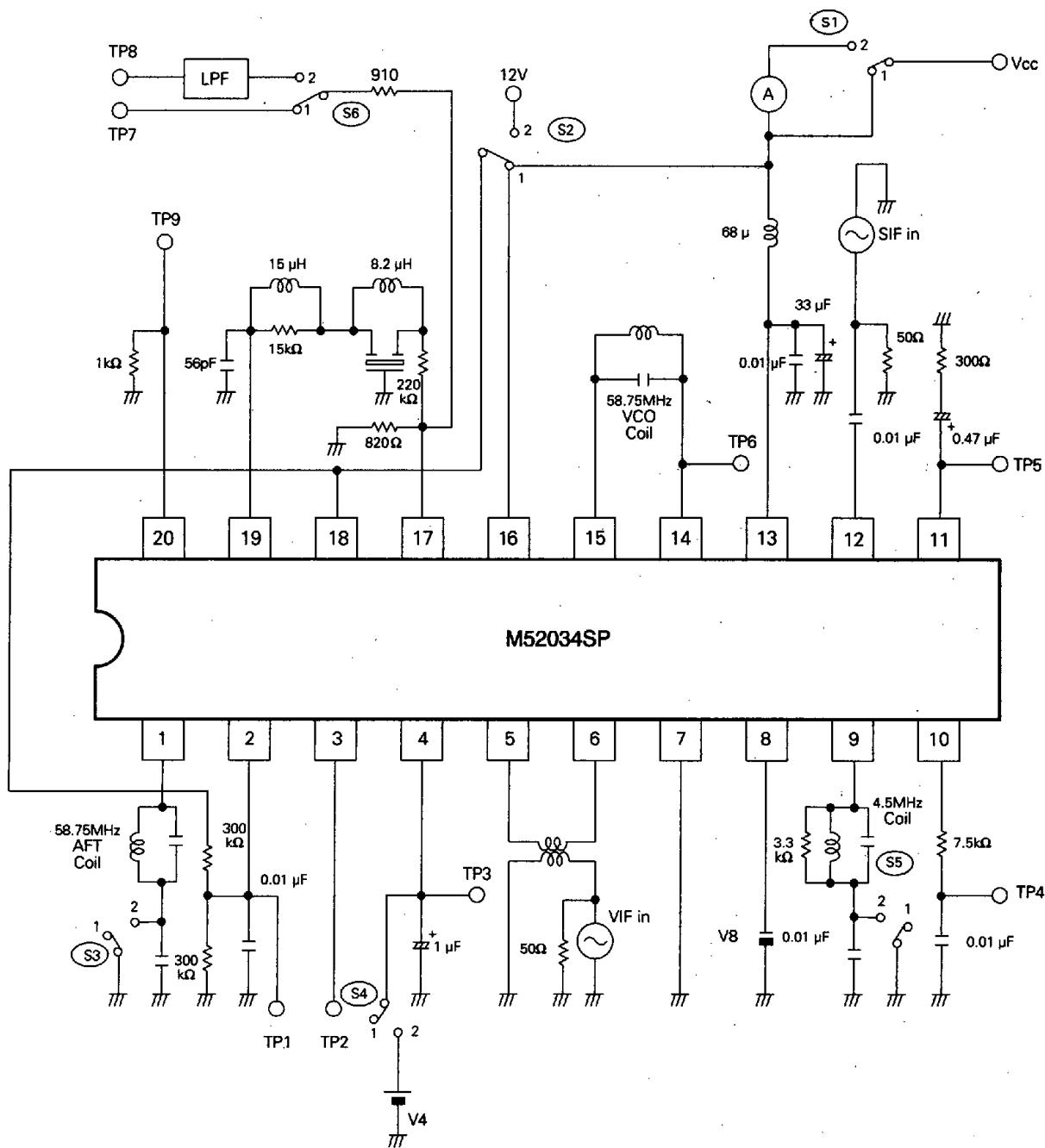
- With VCO coil, IF AGC 0V and non-input condition, adjust free run frequency to 58.75MHz.

**INPUT SIGNAL**

SG. No.	Signals (50Ω termination)	
SG 1	$f_0 = 58.75\text{MHz}$	$V_i = 90\text{dB}\mu$ 77.8% AM (87.5% Video modulation equivalent $fm = 20\text{kHz}$ )
SG 2	$f_0 = 58.75\text{MHz}$	$V_i = 90\text{dB}\mu$
SG 3	$f_1 = 58.75\text{MHz}$	$V_i = 90\text{dB}\mu$ $f_2 = 53 \pm 5\text{MHz}$
SG 4	$f_0 = 58.75\text{MHz}$	$V_i = \text{Variable}$ $fm = 20\text{kHz}$ 77.8% AM
SG 5	$f_0 = 58.75\text{MHz}$	$V_i = \text{Variable}$ $fm = 20\text{kHz}$ 16% AM
SG 6	$f_0 = 58.75\text{MHz}$	$V_i = 80\text{dB}\mu$
SG 7	$f_0 = 58.75\text{MHz}$	$V_i = 120\text{dB}\mu$
SG 8	$f_0 = 54.25\text{MHz}$	$V_i = 100\text{dB}\mu$
SG 9	$f_0 = 54.25\text{MHz}$	$V_i = 80\text{dB}\mu$
SG10	$f_0 = 58.75\text{MHz} \pm 5\text{MHz}$	$V_i = 90\text{dB}\mu$
SG11	$f_0 = 58.75\text{MHz} \pm 5\text{MHz}$	$V_i = 90\text{dB}\mu$ $fm = 20\text{kHz}$ 77.8% AM
SG12	$f_1 = 58.75\text{MHz}$	$V_i = 90\text{dB}\mu$ $f_2 = 58.25\text{MHz}$
SG13	$f_1 = 58.75\text{MHz}$	$V_i = 90\text{dB}\mu$ $f_2 = 55.75\text{MHz}$
SG14	$f_1 = 58.75\text{MHz}$	$V_i = 90\text{dB}\mu$ $f_2 = 53.75\text{MHz}$
SG15	$f_1 = 58.75\text{MHz}$	$V_i = 90\text{dB}\mu$ $f_2 = 55.17\text{MHz}$
SG16	$f_1 = 58.75\text{MHz}$	Standard 10-step wave modulation $m = 87.5\%$ Video modulation Sync chip level $V_i = 90\text{dB}\mu$
SG17	$f_0 = 4.5\text{MHz} \pm 25\text{kHz}$	$dev$ $V_i = 90\text{dB}\mu$ $fm = 400\text{Hz}$
SG18	$f_0 = 4.5\text{MHz} \pm 25\text{kHz}$	$dev$ $V_i = \text{Variable}$ $fm = 400\text{Hz}$
SG19	$f_0 = 4.5\text{MHz}$	$V_i = 90\text{dB}\mu$ 30% AM $fm = 400\text{Hz}$
SG20	$f_0 = 4.5\text{MHz}$	$V_i = 90\text{dB}\mu$
SG21	$f_0 = 4.5\text{MHz}$	$V_i = 90\text{dB}\mu$ $fm = 400\text{Hz} \pm 7.5\text{kHz}$ $dev$

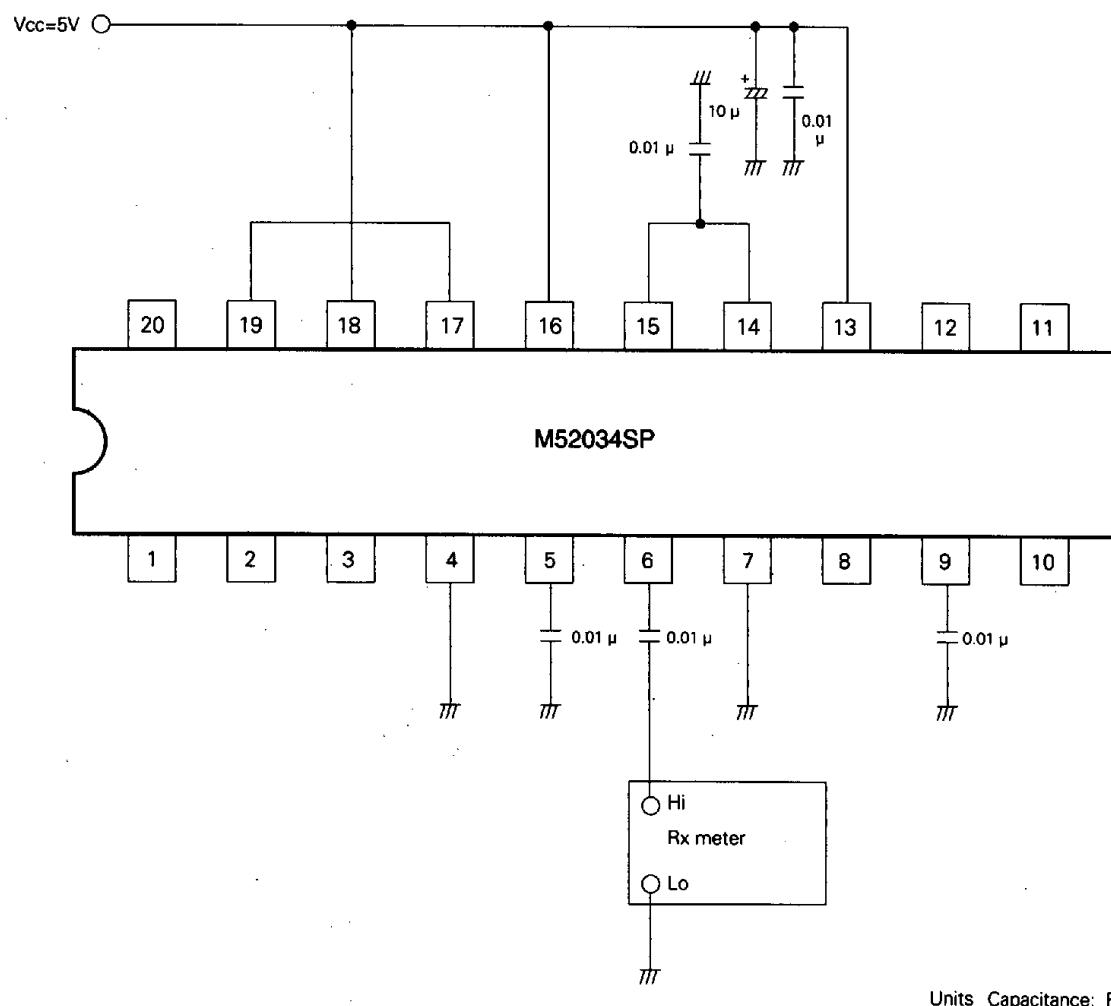
## STANDARD PLL VIF/SIF

## TEST CIRCUIT 1



## STANDARD PLL VIF/SIF

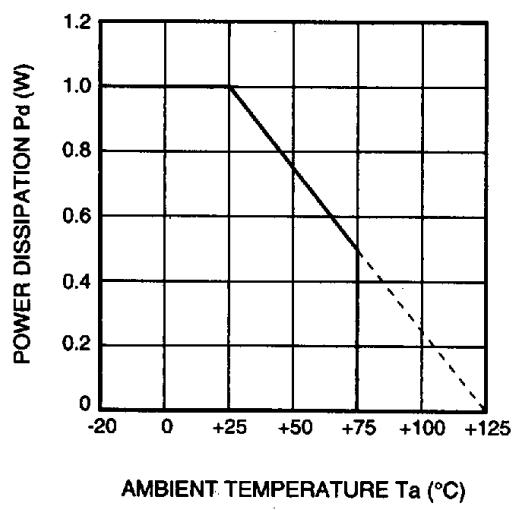
## TEST CIRCUIT 2



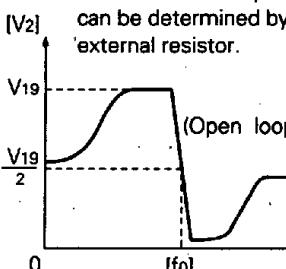
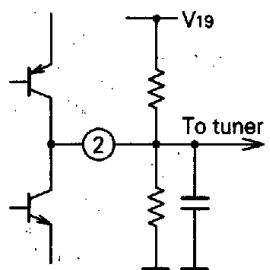
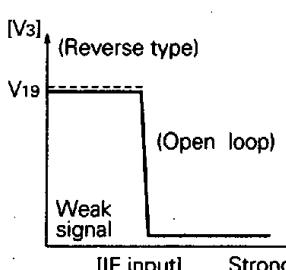
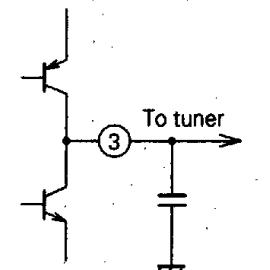
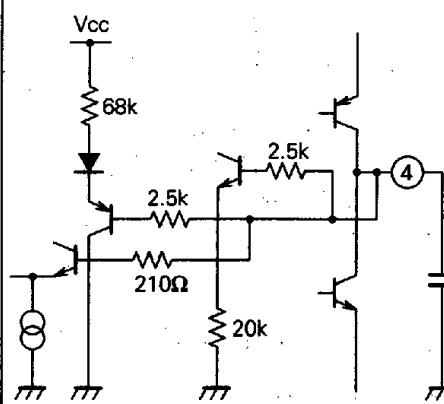
Units Capacitance: F

## TYPICAL CHARACTERISTICS

## THERMAL DERATING (MAXIMUM RATING)

AMBIENT TEMPERATURE  $T_a$  (°C)

## DESCRIPTION OF PIN

Pin No.	Name	Voltage and wave information	Peripheral circuit of pins
①	AFT coil	Mute function is provided and AFT muting is available by grounding this pin. 5V	
②	AFT out	Since AFT output has high impedance, detector sensitivity can be determined by external resistor.  [V2] V19 V19/2 0 [f0]	
③	RF AGC out	[V3] (Reverse type)  [V3] V19 Weak signal [IF input] Strong signal	
④	IF AGC Filter	[V4] 4.4V 0V Weak signal [IF input] Strong signal 2-pin filter characteristics can be obtained by only single filter due to the dynamic AGC circuit adopted.	

## DESCRIPTION OF PIN (cont.)

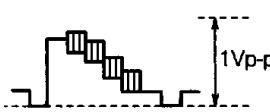
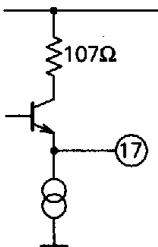
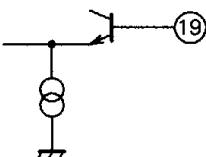
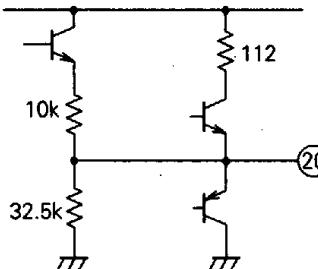
Pin No.	Name	Voltage and wave information	Peripheral circuit of pins
(5) (6)	VIF in	Since frequency ripple may be caused by improper matching with SAW filter, care should be taken in matching in designing. 2.9V	<p>The diagram shows a biasing network consisting of a 6k resistor from Vcc to pin 5, and two 1.2k resistors in series between pin 5 and ground. Pin 6 is connected to the midpoint of these resistors. A common collector stage is formed by a transistor with its collector connected to Vcc and its emitter connected to pin 5. The base of this transistor is connected to the midpoint of the 1.2k resistors. The output of this stage is connected to a SAW filter, represented by a circle labeled "SAW".</p>
(7)	GND	This is the only grounding pin in this IC. 0V	<p>The diagram shows a horizontal line representing the GND connection for pin 7.</p>
(8)	RF AGC Delay	RF AGC delay point can be varied by changing the voltage applied to this pin.	<p>The diagram shows a circuit for pin 8. It consists of a 230Ω resistor connected between pin 8 and Vcc. A capacitor is connected between pin 8 and ground. A switch is also connected between pin 8 and ground.</p>
(9)	FM Det coil	The quadrature detector circuit is used for FM detector. It is necessary to provide a capacitor which cuts off DC signal between pin 9 and GND in series with tank coil. It should be noted that ceramic discriminator does not provide good characteristics. Sound muting is available by grounding this pin. 3.0V	<p>The diagram shows a complex circuit for pin 9. It includes a 30.5k resistor from pin 9 to ground, a 10k resistor, and a 10k capacitor. There are several transistors and diodes forming a detector and muting logic. A "Bias" input is also connected to pin 9.</p>
(10)	Audio out	Audio output pin 2.25V	<p>The diagram shows a circuit for pin 10. It consists of a 11.5kΩ resistor from pin 10 to ground, and an 85Ω resistor connected between pin 10 and Vcc.</p>

## STANDARD PLL VIF/SIFF

## DESCRIPTION OF PIN (cont.)

Pin No.	Name	Voltage and wave information	Peripheral circuit of pins
⑪	APC Filter	<p>[11 pin output]</p> <p>Unlocked state</p> <p>Locked state</p> <p>FM modulation frequency</p> <p>100kHz</p> <p>Frequency response characteristics in locked state is around 100kHz of cut-off frequency, which is the bandwidth of carrier regenerated from IF signal. In unlocked state, cut-off frequency is higher and pull-in range is widened.</p> <p>[11 pin voltage]</p> <p>IF input frequency</p> <p>3.2V</p>	
⑫	SIF in	<p>Input impedance is approx. 1.5kΩ.</p> <p>2.7V</p>	
⑬	Vcc1	5.0V	
⑭ ⑮	VCO coil	<p>This pin oscillates by adding a coil and tuning capacitor. Set this oscillation frequency to <math>f_0</math> for use. Since oscillation level is as large as 112dB<math>\mu</math>, malfunction of VCO may be caused. To avoid this, care should be taken in designing of external pattern around this pin.</p> <p>2.9V</p>	

## DESCRIPTION OF PIN (cont.)

Pin No.	Name	Voltage and wave information	Peripheral circuit of pins
⑯	Vcc 1	5V	—
⑰	Video out	Positive output. Output is generated by 87.5% video modulation and has 1 Vp-p amplitude.  	
⑱	Vcc 2	AFT output and RF AGC output can be input to the tuner by setting this voltage to that of tuner.  5V~12V	—
⑲	EQ in	This is an open base input pin. Usually, 17 pin voltage is used as input voltage to this pin.	
⑳	EQ out	Push-and-pull feedback circuit is used. Output driving capacity is 3.9kΩ, but it can be improved to 600Ω by adding 1kΩ between 20 pin and GND.	

## STANDARD PLL VIF/SIFF

**PRECAUTIONS FOR APPLICATION****1. Adjustment of free run frequency**

## Example 1)

- With no input to IF and IF AGC voltage (pin 4) set to 0V, decrease IF AMP gain.
- Read the oscillation frequency leaked to video output (pin 17) and adjust the coil to the center frequency (ex. 58.75MHz).

## Example 2)

- Input sweep signal to IF. Add a large capacity capacitor ( $\sim 10\mu F$ ) to APC filter pin (pin 11) so that PLL does not follow the sweep frequency.
- Measure beat signal in the video output and adjust VCO coil so that the zero beat will come to 58.75MHz.

## Example 3)

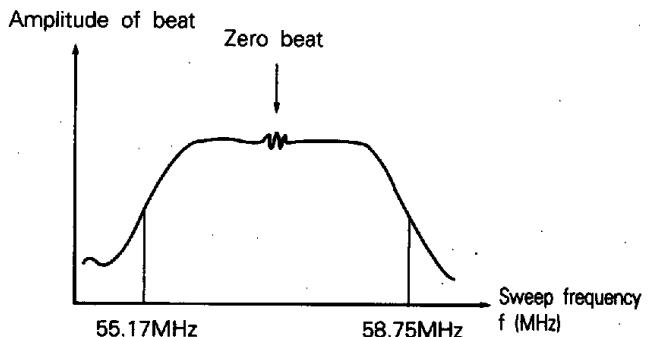
- With no input to IF, measure DC voltage at APC filter pin(pin 11) when VCO is oscillating in the free run state. At this time, set IF AGC voltage (pin 4) to 0V.
- With loop IF AGC, input 58.75 MHz in IF AMP and adjust VCO coil so that APC filter pin (pin 11) will come to the voltage measured in (a).

**2. Adjustment of IF response**

(This adjustment should be made after adjusting free run frequency.)

- Connect an external power supply to APC filter pin (pin 11) and adjust the applied voltage so that it oscillates at 58.75MHz( $V_{11} \sim 5.0V$ ).
- Input sweep signal in IF. Apply IF AGC voltage (pin 4) from outside and fix the voltage so that beat output to the video output pin (pin 17) does not distort. Envelope of beat at this time indicates general response for both IF and IC.

- To see characteristics around 58.75MHz, shift the free run frequency.



However, response is varied when the free run frequency is shifted from 58.75MHz. This is because frequency characteristics inside IC starts dropping at around 3MHz and accordingly, amplitude level of beat drops slightly as the beat frequency increases.

