

SWITCHING
N-CHANNEL POWER MOS FET
INDUSTRIAL USE**DESCRIPTION**

The 2SK3060 is N-Channel MOS Field Effect Transistor designed for high current switching applications.

FEATURES

- Low on-state resistance
 $R_{DS(on)1} = 13 \text{ m}\Omega \text{ MAX. (} V_{GS} = 10 \text{ V, } I_D = 35 \text{ A)}$
 $R_{DS(on)2} = 20 \text{ m}\Omega \text{ MAX. (} V_{GS} = 4.0 \text{ V, } I_D = 35 \text{ A)}$
- Low C_{iss} : $C_{iss} = 2400 \text{ pF TYP.}$
- Built-in gate protection diode

ORDERING INFORMATION

PART NUMBER	PACKAGE
2SK3060	TO-220AB
2SK3060-S	TO-262
2SK3060-ZJ	TO-263
★ 2SK3060-Z	TO-220SMD ^{Note}

Note This package is produced only in Japan.

ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C)

Drain to Source Voltage (V _{GS} = 0 V)	V _{DSS}	60	V
Gate to Source Voltage (V _{DS} = 0 V)	V _{GSS(AC)}	±20	V
Gate to Source Voltage (V _{DS} = 0 V)	V _{GSS(DC)}	+20, -10	V
Drain Current (DC)	I _{D(DC)}	±70	A
Drain Current (Pulse) ^{Note1}	I _{D(pulse)}	±210	A
Total Power Dissipation (T _c = 25°C)	P _T	70	W
Total Power Dissipation (T _A = 25°C)	P _T	1.5	W
Channel Temperature	T _{ch}	150	°C
Storage Temperature	T _{stg}	-55 to +150	°C
Single Avalanche Current ^{Note2}	I _{AS}	35	A
Single Avalanche Energy ^{Note2}	E _{AS}	122.5	mJ

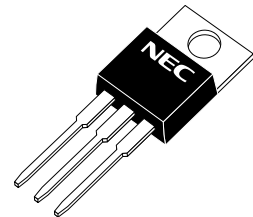
Notes 1. PW ≤ 10 μs, Duty cycle ≤ 1%

2. Starting T_{ch} = 25°C, R_G = 25 Ω, V_{GS} = 20 V → 0 V

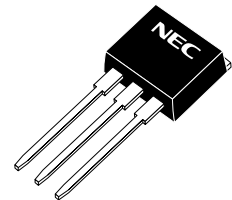
THERMAL RESISTANCE

Channel to Case	R _{th(ch-C)}	1.79	°C/W
Channel to Ambient	R _{th(ch-A)}	83.3	°C/W

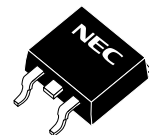
(TO-220AB)



(TO-262)



(TO-263, TO-220SMD)

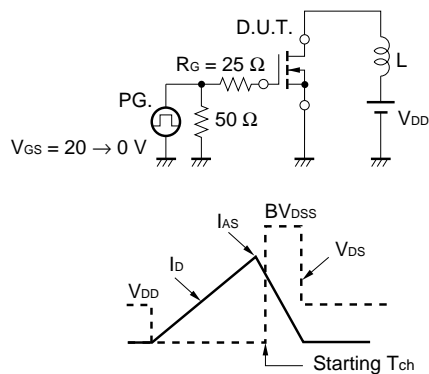


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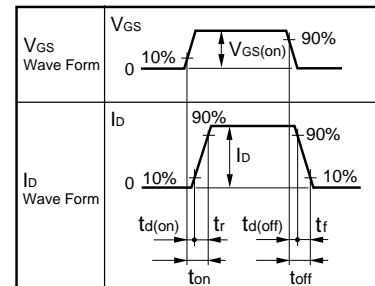
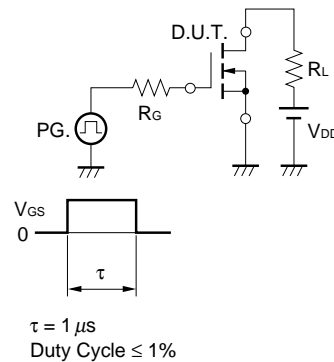
ELECTRICAL CHARACTERISTICS (T_A = 25°C)

CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Drain to Source On-state Resistance	R _{DS(on)1}	V _{GS} = 10 V, I _D = 35 A		11	13	mΩ
	R _{DS(on)2}	V _{GS} = 4.0 V, I _D = 35 A		16	20	mΩ
Gate to Source Cut-off Voltage	V _{GS(off)}	V _{DS} = 10 V, I _D = 1 mA	1.0	1.5	2.0	V
Forward Transfer Admittance	y _{fs}	V _{DS} = 10 V, I _D = 35 A	15	50		S
Drain Leakage Current	I _{DSS}	V _{DS} = 60 V, V _{GS} = 0 V			10	μA
Gate to Source Leakage Current	I _{GSS}	V _{GS} = ±20 V, V _{DS} = 0 V			±10	μA
Input Capacitance	C _{iss}	V _{DS} = 10 V		2400		pF
Output Capacitance	C _{oss}	V _{GS} = 0 V		700		pF
Reverse Transfer Capacitance	C _{rss}	f = 1 MHz		280		pF
Turn-on Delay Time	t _{d(on)}	I _D = 35 A		30		ns
Rise Time	t _r	V _{GS(on)} = 10 V		600		ns
Turn-off Delay Time	t _{d(off)}	V _{DD} = 30 V		140		ns
Fall Time	t _f	R _G = 10 Ω		450		ns
Total Gate Charge	Q _G	I _D = 70 A		50		nC
Gate to Source Charge	Q _{GS}	V _{DD} = 48 V		7.5		nC
Gate to Drain Charge	Q _{GD}	V _{GS} = 10 V		18		nC
Body Diode Forward Voltage	V _{F(S-D)}	I _F = 70 A, V _{GS} = 0 V		1.0		V
Reverse Recovery Time	t _{rr}	I _F = 70 A, V _{GS} = 0 V		55		ns
Reverse Recovery Charge	Q _{rr}	di/dt = 100 A/μs		75		nC

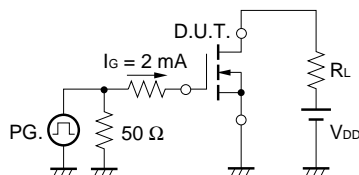
TEST CIRCUIT 1 AVALANCHE CAPABILITY



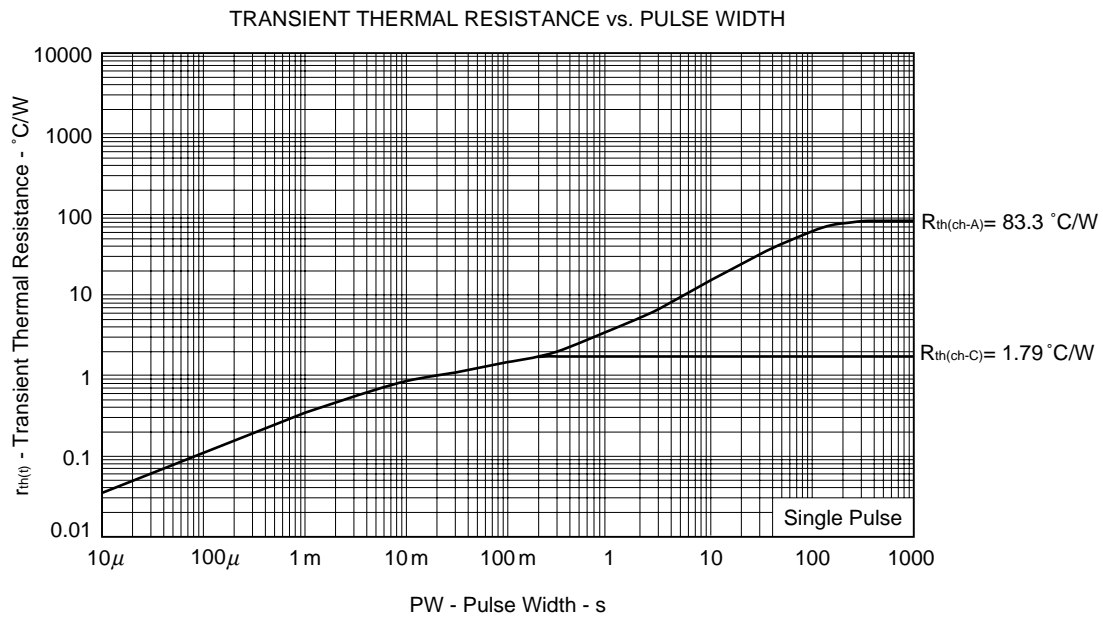
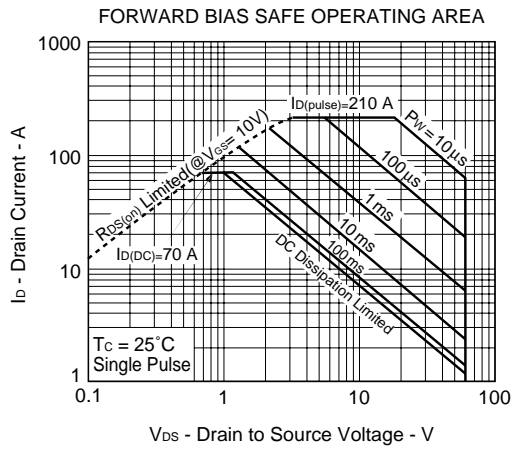
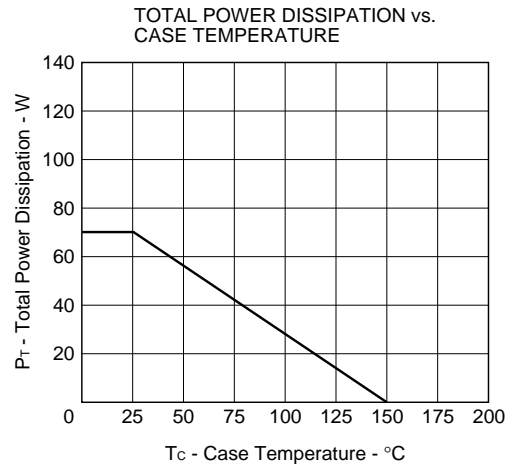
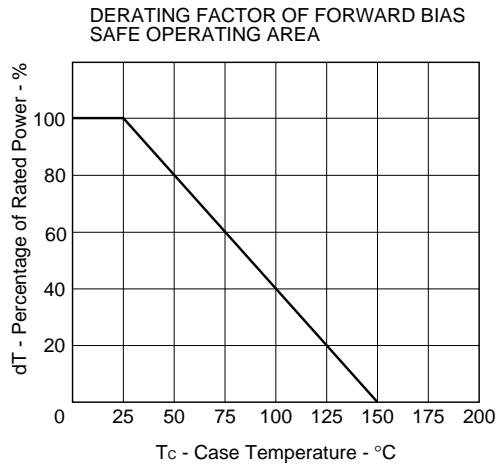
TEST CIRCUIT 2 SWITCHING TIME

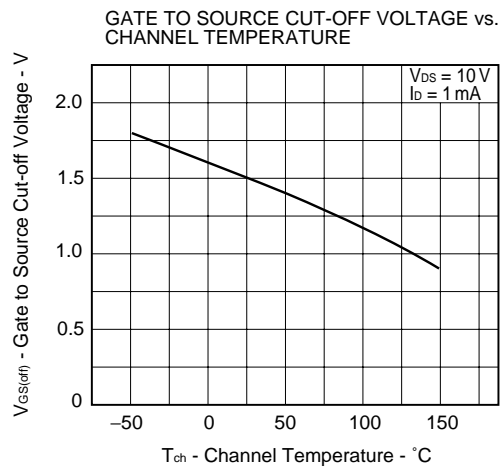
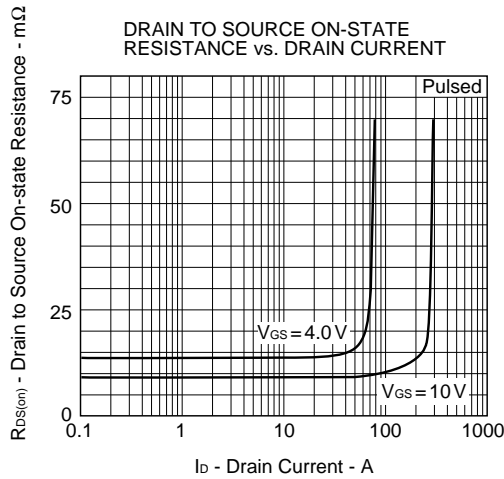
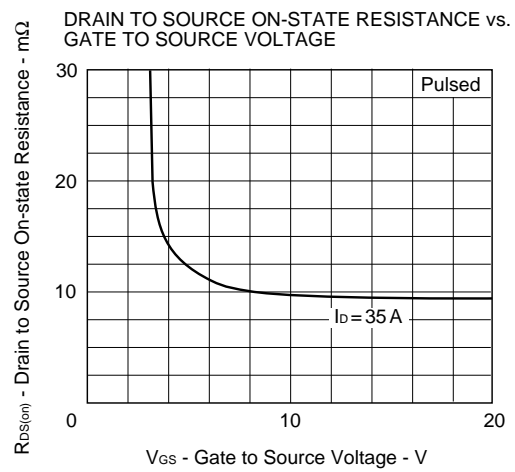
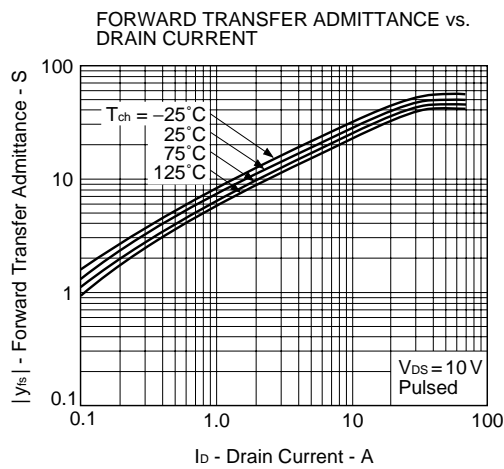
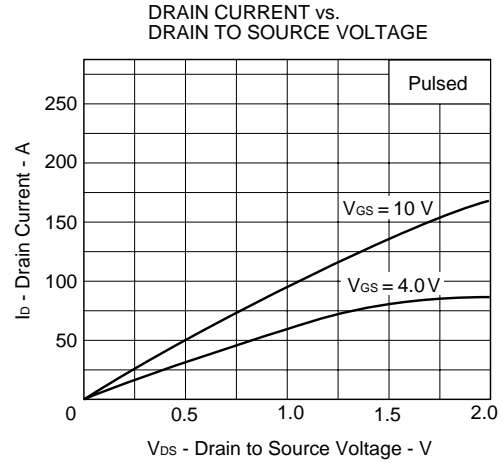
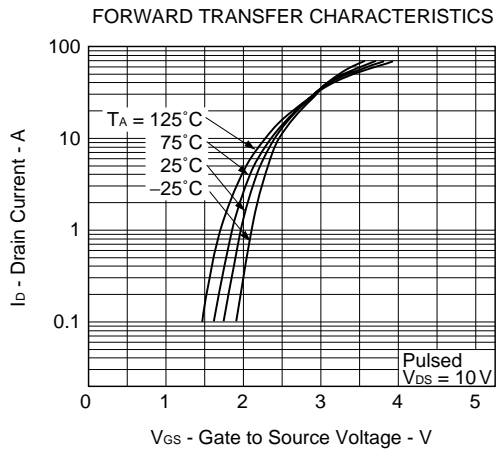


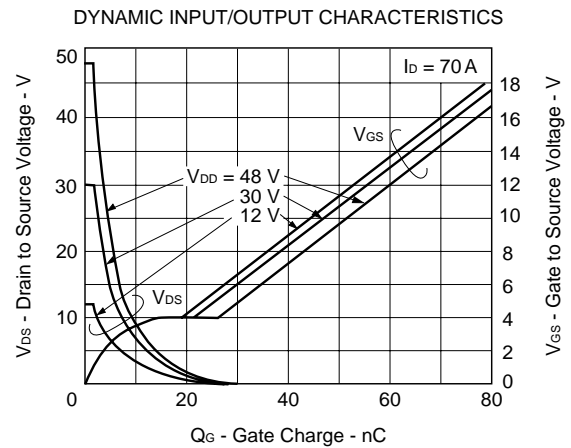
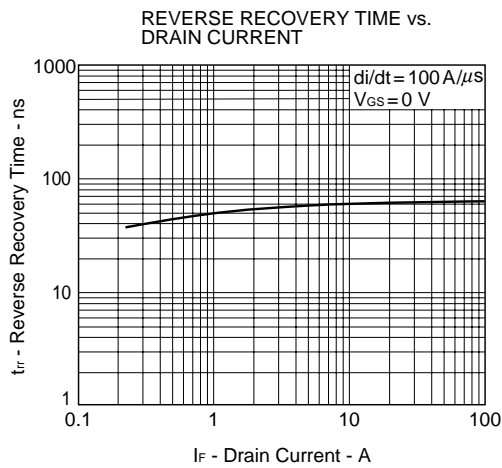
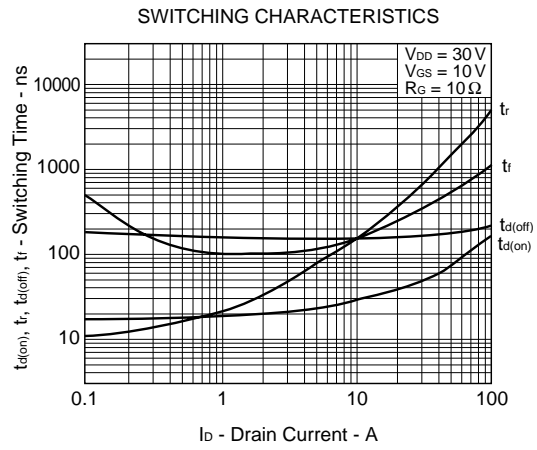
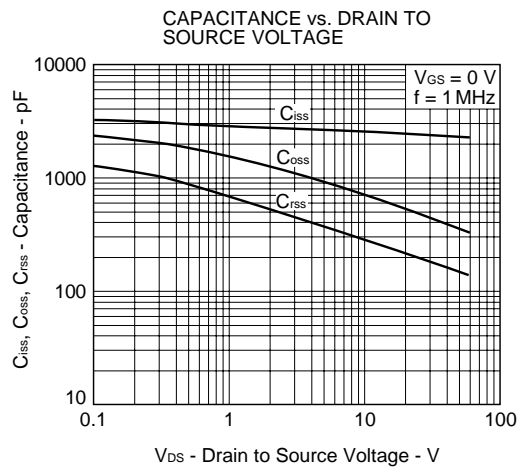
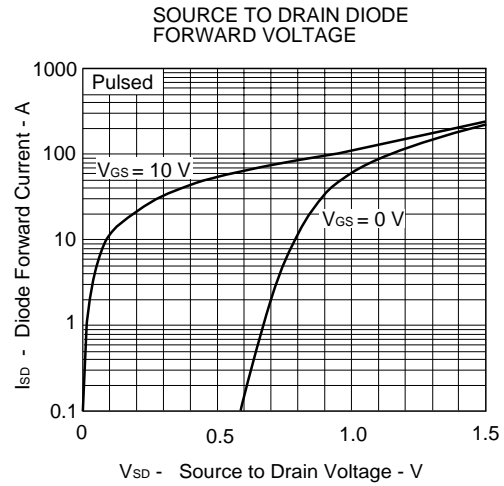
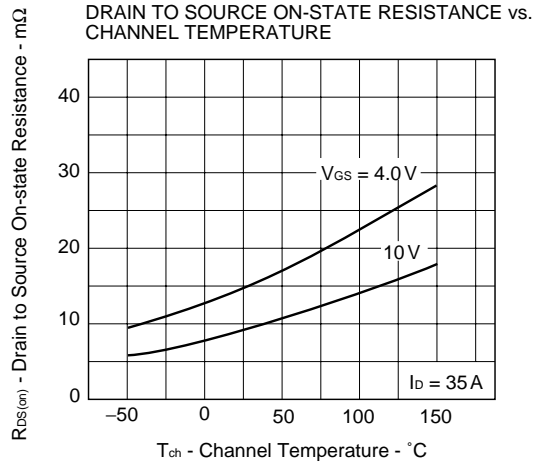
TEST CIRCUIT 3 GATE CHARGE

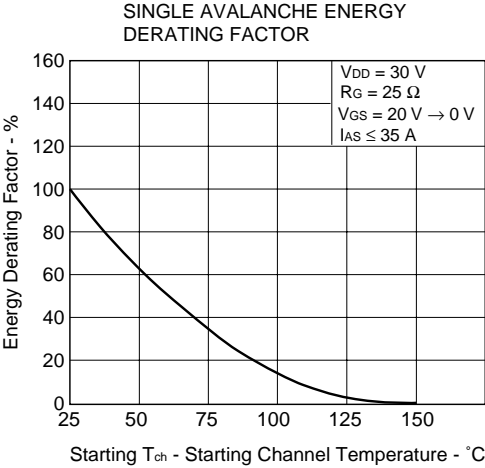
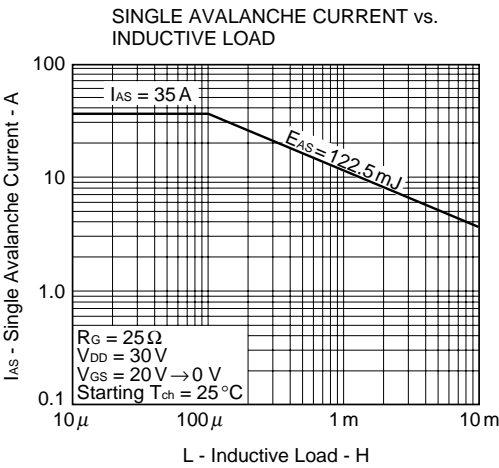


TYPICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$)



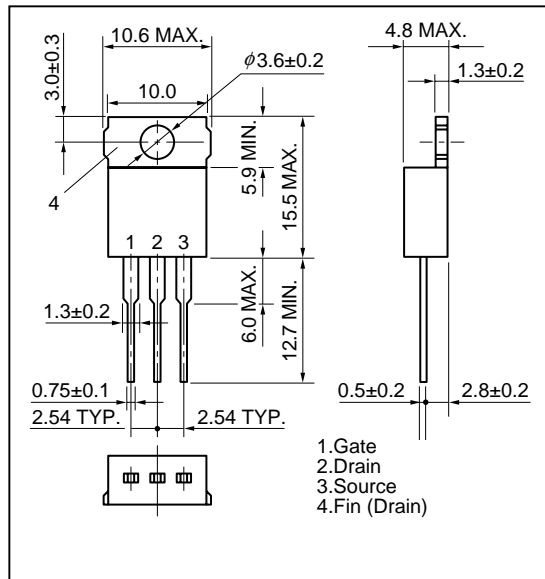




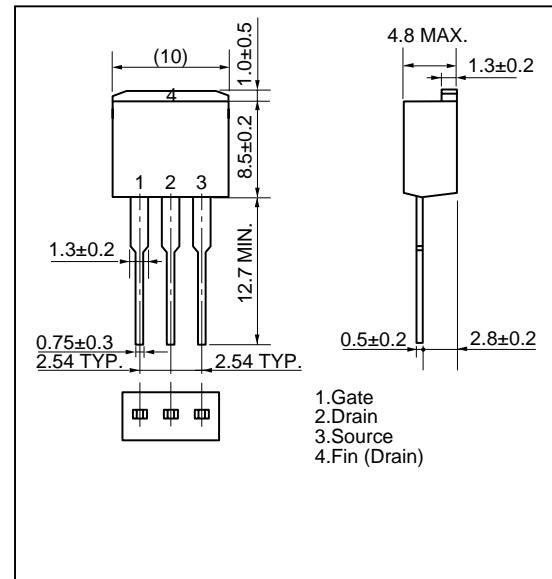


PACKAGE DRAWINGS (Unit : mm)

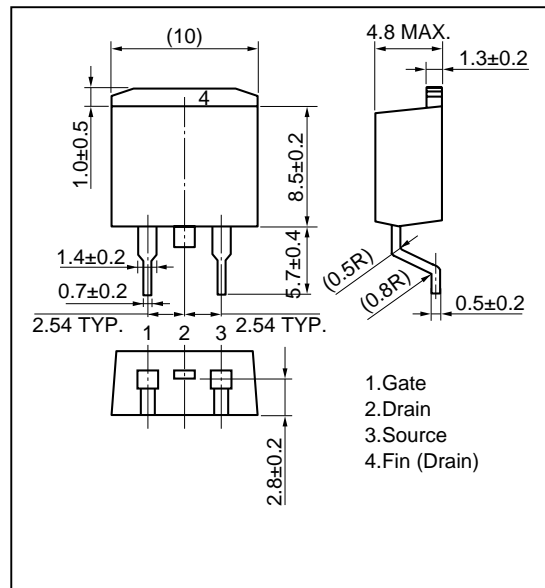
1)TO-220AB (MP-25)



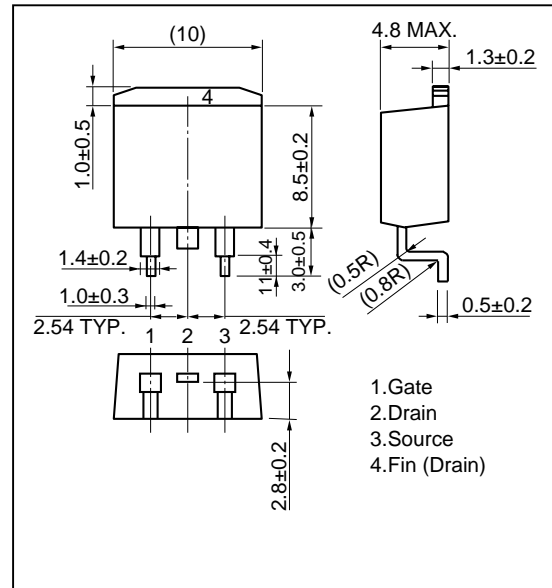
2)TO-262 (MP-25 Fin Cut)



3)TO-263 (MP-25ZJ)

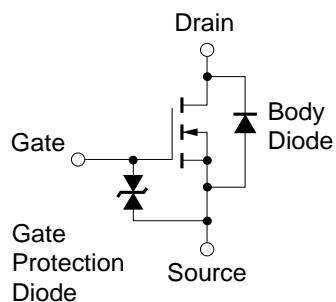


★ 4)TO-220SMD (MP-25Z) ^{Note}



Note This package is produced only in Japan.

EQUIVALENT CIRCUIT



Remark The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.

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