32-Channel Serial to Parallel Converter With High Voltage Push-Pull Outputs

Features

- HVCMOS® technology
- Operating output voltage up to +50/-40V
- Shift register speed 40MHz @ V_{DD} = 5V
- Data speed up to 160MHz @ V_{DD} = 5V
- 32 high voltage outputs
- CMOS/TTL compatible

Applications

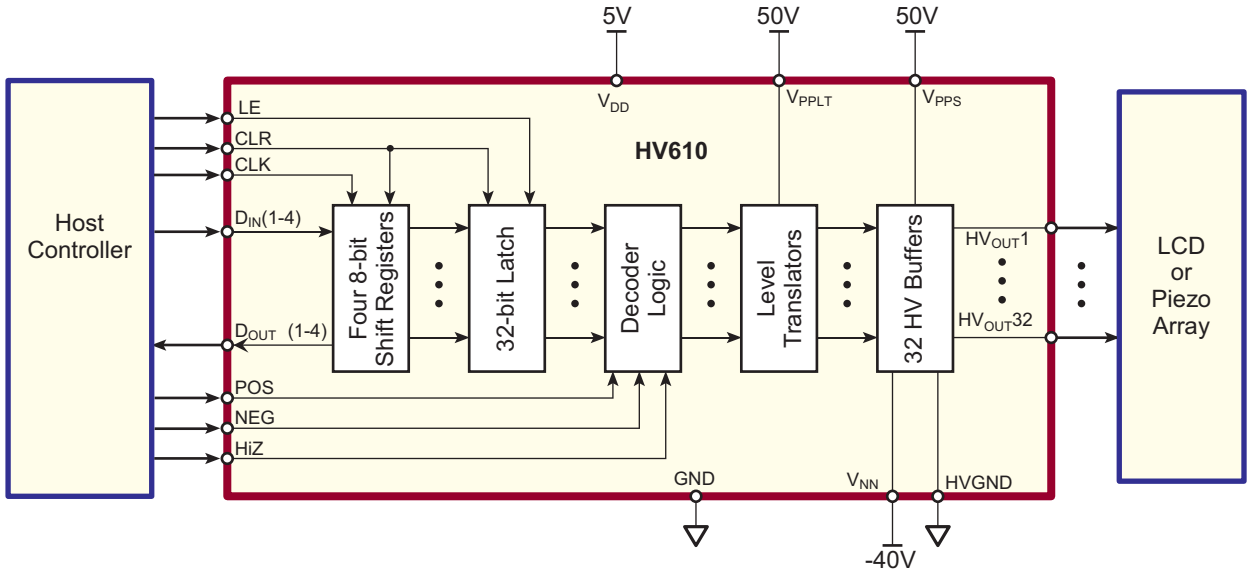
- High speed print head driver
- LCD driver

General Description

The HV610 is a 32-channel high voltage, medium current driver IC. The outputs can be either at V_{PPS}, V_{NN}, HiZ, or HVGND.

Data is shifted through four parallel 8-bit shift registers on the low to high transition of the clock. A data output buffer is provided for cascading devices. Data is transferred to a 32-bit latch when logic level high is applied to the LE input. The CLR signal will reset both the shift register and the latch. Output states are controlled by POS, and NEG input signals, and by data in the latch. All outputs are tri-stated upon a logic high on the HiZ input signal.

Typical Application Diagram

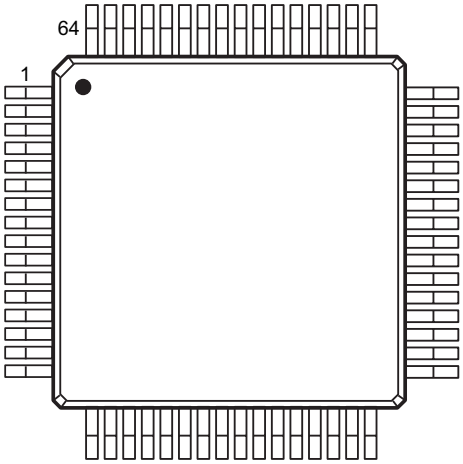


Ordering Information

Device	64-Lead TQFP *10x10x1.20mm body, 0.50mm pitch*
HV610	HV610FG-G

-G indicates package is RoHS compliant ('Green')

Pin Configuration



64-Lead TQFP
(top view)

Absolute Maximum Ratings

Parameter	Value
Supply voltage, V_{DD}	-0.5V to 6V
Supply voltage, V_{PP}	55V
Supply voltage, V_{NN}	-45V
Logic input levels	-0.5V to V_{DD}+0.5V
Operating junction temperature range	-40°C to +125°C
Storage temperature range	-65°C +150°C

All voltages referenced to GND.

Product Marking

Top Marking

Bottom Marking

YY = Year Sealed
WW = Week Sealed
L = Lot Number
C = Country of Origin*
A = Assembler ID*
_____ = "Green" Packaging

**May be part of top marking*

Operating Supply Voltages and Temperatures *(All voltages referenced to GND)*

Symbol	Parameter	Min	Typ	Max	Units	Conditions
V_{DD}	Logic supply voltage	4.5	5.0	5.5	V	---
V_{PPS}	Positive high voltage supply for HV_{OUTPUT} source	25	-	50	V	For f_{OUT} = 200kHz
V_{PPLT}	Positive high voltage supply for level translators	47.5	-	50	V	---
V_{NN}	Negative high voltage supply	-15	-	-40	V	For f_{OUT} = 200kHz
HVGND	High voltage ground	-5	-	+5	V	---
V_{IH}	High-level input voltage	2.0	-	V_{DD}	V	---
V_{IL}	Low-level input voltage	0		0.8	V	---
T_A	Operating ambient temperature	-40	-	+85	°C	---

DC Electrical Characteristics

Over operating supply voltages and temperature, unless otherwise noted.

Symbol	Parameter		Min	Typ	Max	Units	Conditions
I_{DD}	V_{DD} supply current		-	-	15	mA	f_{CLK} = 40MHz
I_{DDQ}	V_{DD} quiescent supply current		-	-	0.1	mA	All logic inputs = V_{DD} or 0V
			-	-	2.2		Per each input at TTL level
I_{PPS}	V_{PPS} supply current		-	-	412	mA	CL = 700pF, f_{OUT} = 200kHz, all channels switching per HV_{OUT} waveform
I_{PPSQ}	V_{PPS} quiescent supply current		-	-	100	µA	V_{PPS} = 50V, outputs static, V_{PPLT} = 50V
I_{PPLT}	V_{PPLT} supply current		-	-	17	mA	f_{OUT} = 200kHz
I_{PPLTQ}	V_{PPLTQ} quiescent supply current		-	-	100	µA	V_{PPS} = 50V, outputs static, V_{PPLT} = 50V
I_{NN}	V_{NN} supply current		-	-	433	mA	CL = 700pF, f_{OUT} = 200kHz, all channels switching per HV_{OUT} waveform
I_{NNQ}	V_{NN} quiescent supply current		-	-	100	µA	V_{NN} = -40V, outputs static
I_{IH}	Logic input high current		-	-	50	µA	V_{IH} = V_{DD}
			-	-	50	µA	V_{IH} = 2.0V
I_{IL}	Logic input low current		-	-	-50	µA	V_{IL} = 0V
			-	-	-50		V_{IL} = 0.8V
I_{OL}	D_{OUT} low level logic sink current		-	-	12	mA	D_{OUT} < 0.8V
I_{OH}	D_{OUT} high level logic source current		-	-	-12	mA	D_{OUT} > 2.0V
V_{OH}	High level output	HV_{OUT}	V_{PPS} -10	-	-	V	IHV_{OUT} = -35mA, V_{PPS} = +50V, V_{PPLT} = +50V, V_{NN} = -40V
		D_{OUT}	V_{DD} -1.0	-	-		ID_{OUT} = -15mA
V_{OL}	Low level output	HV_{OUT}	-	-	V_{NN} +10	V	IHV_{OUT} = 35mA, V_{PPS} = +50V, V_{PPLT} = +50V, V_{NN} = -40V
		D_{OUT}	-	-	1.0		ID_{OUT} = 15mA
V_{OMID}	Mid level output		-10	-	10	V	I_{MID} = ±35mA, V_{PPS} = +50V, V_{PPLT} = +50V, V_{NN} = -40V
C_{DIN}	LV input capacitance		-	-	10	pF	---

AC Electrical Characteristics

Over operating supply voltages and temperature, unless otherwise noted.

Symbol	Parameter	Min	Typ	Max	Units	Conditions
f_{CLK}	Clock frequency	0	-	40	MHz	0 toV_{DD} clock input
		0	-	33		0 to 2.0V clock input
f_{OUT}	Output switching frequency switching waveform	-	-	200	KHz	CL = 700pf, 5% to 95% V_{PPLT} = 50V
t_C	Clock high/low pulse width	10	-	-	ns	0 - V_{DD} logic signals
		10	-	-		0 - 2.0V logic signals

AC Electrical Characteristics *(cont.)*

Over operating supply voltages and temperature, unless otherwise noted.

Symbol	Parameter	Min	Typ	Max	Units	Conditions
t_{SUD}	Data setup time before clock rises	12.5	-	-	ns	0 - V_{DD} logic signals
		15	-	-		0 - 2V logic signals
t_{HD}	Data hold time after clock rises	2	-	-	ns	---
t_{SUC}	LE from CLK setup time	15	-	-	ns	---
t_{LE}	LE pulse width	10	-	-	ns	---
t_{WOC}	Width of CLR, POS, NEG, HiZ pulses	500	-	-	ns	---
t_{DHiZ}	HiZ input to HV_{OUT} HiZ state delay	-	-	400	ns	---
t_{CLRH}	CLR input to HV_{OUT} delay	-	-	1.1	µs	---
t_{DCLR}	CLR input to D_{OUT} delay	5	-	50	ns	---
t_{DD}	Clock positive edge to D_{OUT} delay	2.5	-	12.5	ns	C_{LDOUT} = 30pF
t_{PHV}	Delay time from inputs for HV_{OUT} to start rise/fall	-	-	500	ns	V_{PPLT} = 50V
t_{HiZ}	Output HiZ state before each transition	-	-	100	ns	V_{PPLT} = 50V
t_{HR}	Time for output to go from 95% of V_{PPS}/V_{NN} to 99% of V_{PPS}/V_{NN}	-	-	0.5	µs	C_L = 700pF, HV_{GND} to V_{PPS}, or HV_{GND} to V_{NN} transitions
		-	-	1.0	µs	C_L = 700pF, V_{PPS} to V_{NN}, or V_{NN} to V_{PPS} transitions
t_{HG}	Time for output to go from HV_{GND} ± 1V to within 1% of HV_{GND}	-	-	0.5	µs	CL = 700pF, V_{NN} to HV_{GND}, or V_{PPS} to HV_{GND} transitions
t_{RPN}, t_{FPN}	Output rise/fall time (per function table3)	-	-	1.6	µs	CL = 700pF, V_{PPLT} = 50V, transitions between V_{PPS} and V_{NN}
t_{RR}, t_{FR}	Output rise/fall time from HV_{GND} to 95% of V_{PPS}/V_{NN}	-	-	0.9	µs	CL = 700pF, V_{PPLT} = 50V
t_{RG}, t_{FG}	Output rise/fall time from 95% of V_{PPS}/V_{NN} to HV_{GND} ±1V	-	-	0.9	µs	CL = 700pF, V_{PPLT} = 50V
t_{ORPN}, t_{OFPN}	Delay time from input edges to 95% of HV_{OUT} rise/fall (per function table 3)	-	-	1.8	µs	CL = 700pF, V_{PPLT} = 50V, transitions between V_{PPS} and V_{NN}
t_{ORG}, t_{OFG}	Delay time from input edges to 95% of HV_{OUT} rise/fall from HV_{GND} to V_{PPS} or V_{NN}, or from V_{PPS}/V_{NN} to within ±1V of HV_{GND}	-	-	1.1	µs	CL = 700pF, V_{PPLT} = 50V, transitions between V_{PPS}/V_{NN} and HV_{GND}
θ_{JA}	Thermal resistance, junction to ambient	-	59	-	^{O}C/W	Mounted on 4-layer PCB board

Function Table 1 (S/R and D_{OUT} of S/R one of four)

Inputs				Outputs	
Data (n-1)	CLK	CLR	LE, POS, NEG, HiZ	S/R1...8(n)*	Data Out
L or H	L to H	L	X	S/R1 = D_{IN}(n-1) S/R2 = S/R1(n-1) . . S/R8 = S/R7(n-1)	S/R8(n-1)
X	L	L	X	S/R1..8(n-1)	D_{OUT}(n-1)
X	H	L	X	S/R1..8(n-1)	D_{OUT}(n-1)
X	X	H	X	L	L

Notes:

H = high level, L = low level, X = irrelevant,

**D_{IN}1 to D_{IN}4 => 1st S/R1..8 to 4th S/R1..8,*

**1st S/R1..8 to 4th S/R1..8 = D1..D8, D9..D16, D17..D24, D25..D32*

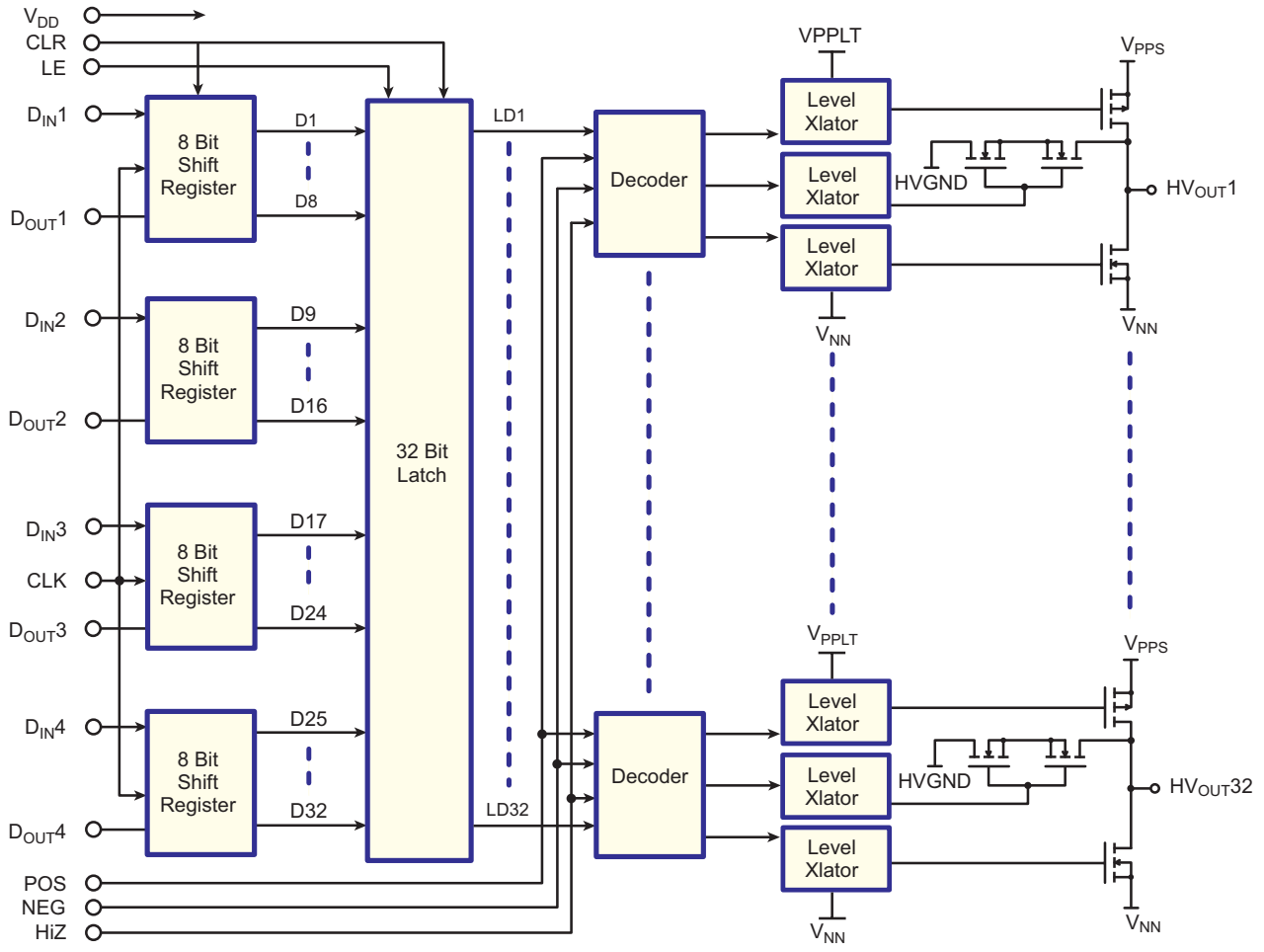
Function Table 2 (Latch)

Inputs				Outputs
D1..32	LE	CLR	CLK, POS, NEG, HiZ	LD1..32
X	X	H	X	L
L or H	H	L	X	L or H
X	L	L	X	Unchanged

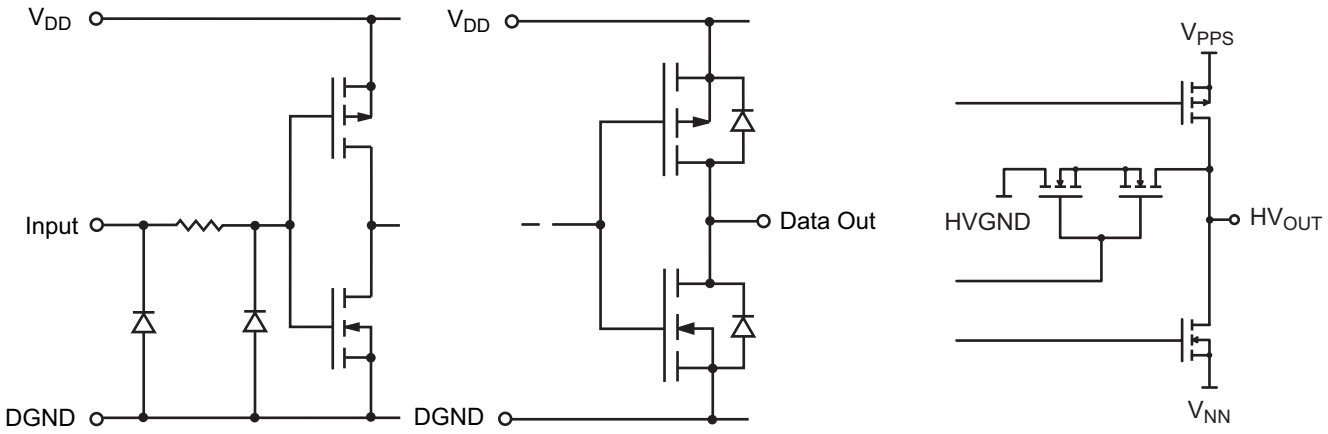
Function Table 3 (HV outputs)

Inputs								Outputs
POS	NEG	HiZ	CLK	LE	CLR	D_{IN}	LD1..32	HV_{OUT}1..32
X	X	H	X	X	X	X	X	HiZ
H	H	L	X	L	L	X	H	HiZ
L	L	L	X	L	L	X	X	HVGND
X	X	L	X	L	L	X	L	HVGND
L	H	L	X	L	L	X	H	V_{NN}
H	L	L	X	L	L	X	H	V_{PPS}
X	X	L	X	X	H	X	X	HVGND

Functional Block Diagram

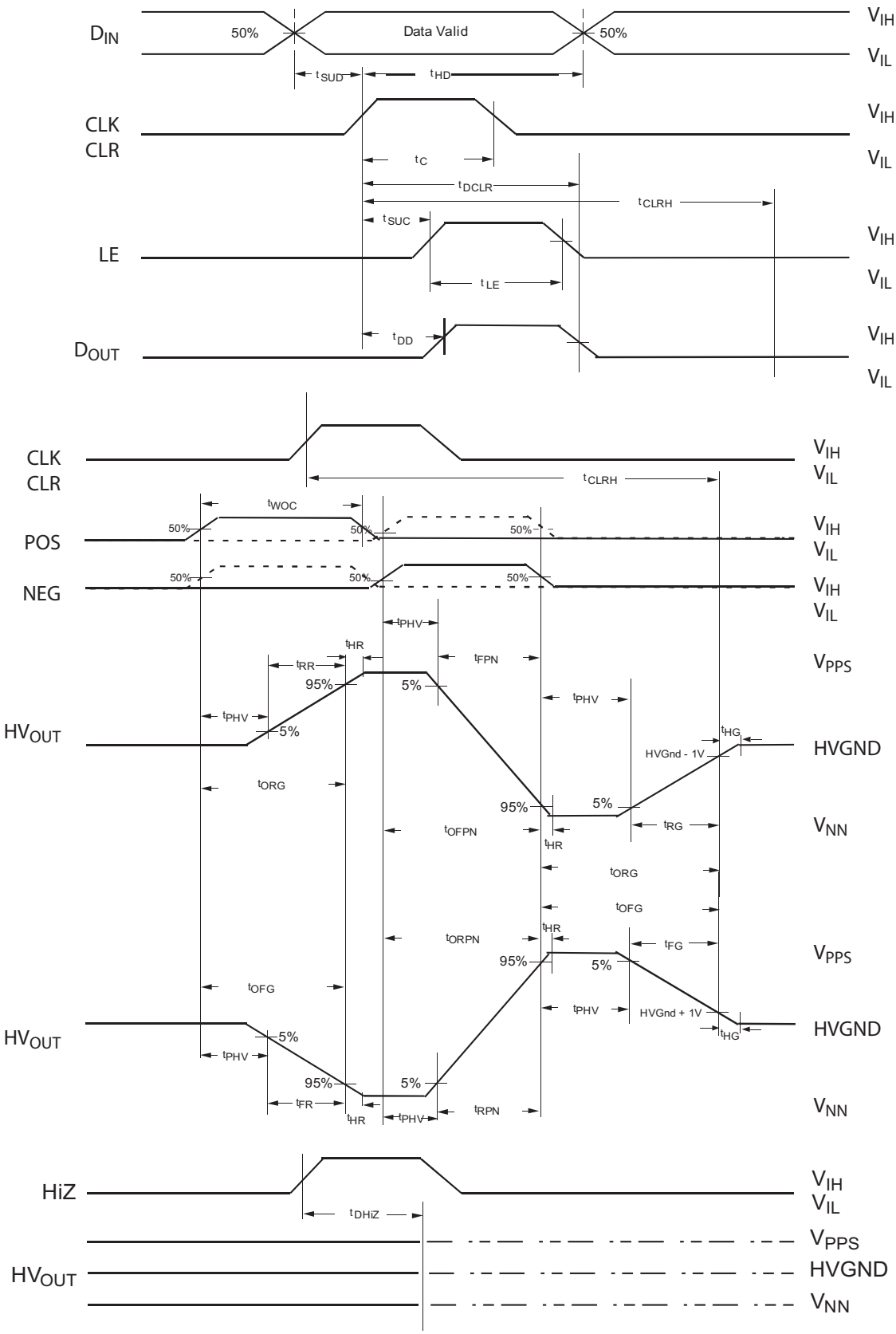


Input and Output Equivalent Circuits



Logic Inputs | Logic Data Output | High Voltage Outputs

Switching Waveforms



TQFP Pin Description

Pin #	Function	Pin #	Function	Pin #	Function	Pin #	Function
1	V_{NN}	17	HVGND	33	$D_{IN}2$	49	$D_{OUT}1$
2	$HV_{OUT}23$	18	V_{PPS}	34	$D_{IN}3$	50	V_{PPLT}
3	$HV_{OUT}22$	19	$HV_{OUT}9$	35	$D_{IN}4$	51	HVGND
4	$HV_{OUT}21$	20	$HV_{OUT}8$	36	DGND	52	V_{PPS}
5	$HV_{OUT}20$	21	$HV_{OUT}7$	37	POS	53	V_{NN}
6	$HV_{OUT}19$	22	$HV_{OUT}6$	38	NEG	54	$HV_{OUT}32$
7	$HV_{OUT}18$	23	$HV_{OUT}5$	39	HIZ	55	$HV_{OUT}31$
8	$HV_{OUT}17$	24	$HV_{OUT}4$	40	CLK	56	$HV_{OUT}30$
9	$HV_{OUT}16$	25	$HV_{OUT}3$	41	CLR	57	$HV_{OUT}29$
10	$HV_{OUT}15$	26	$HV_{OUT}2$	42	LE	58	$HV_{OUT}28$
11	$HV_{OUT}14$	27	$HV_{OUT}1$	43	V_{DD}	59	$HV_{OUT}27$
12	$HV_{OUT}13$	28	V_{NN}	44	DGND	60	$HV_{OUT}26$
13	$HV_{OUT}12$	29	V_{PPS}	45	NC	61	$HV_{OUT}25$
14	$HV_{OUT}11$	30	HVGND	46	$D_{OUT}4$	62	$HV_{OUT}24$
15	$HV_{OUT}10$	31	V_{PPLT}	47	$D_{OUT}3$	63	V_{PPS}
16	V_{NN}	32	$D_{IN}1$	48	$D_{OUT}2$	64	HVGND

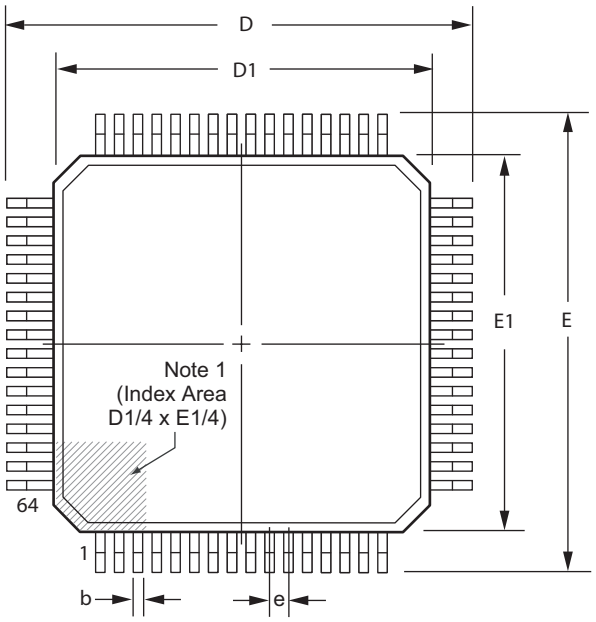
Power-Up / Power-Down Sequence

Step	Description
1	Connect DGND and HVGND
2	Apply V_{DD}
3	Set all inputs (Data, CLK, LE, POS, NEG, HiZ, etc.) to a known state
4	Apply V_{NN}
5	Apply V_{PPLT}
6	Apply V_{PPS}

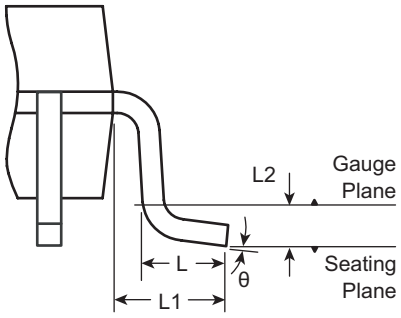
Power-down sequence should be the reverse of the above. To insure the safest power-up/down sequence, the intervals between power-up signals should be between 1msec to 10msec, after the previous signal changed 95% of its final level.

64-Lead TQFP Package Outline (FG)

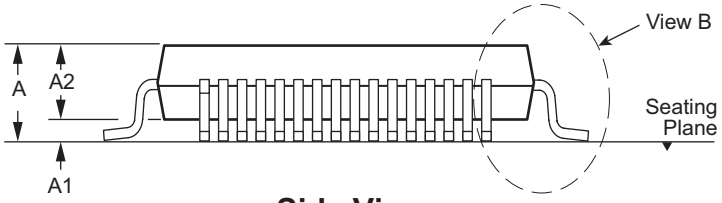
10x10mm body, 1.2mm height (max.), 0.50mm pitch



Top View



View B



Side View

Note 1:

A Pin 1 identifier must be located in the index area indicated. The Pin 1 identifier may be either a mold, or an embedded metal or marked feature.

Symbol		A	A1	A2	b	D	D1	E	E1	e	L	L1	L2	θ
Dimension (mm)	MIN	1.00	0.05	0.95	0.17	11.80	9.80	11.80	9.80	0.50 BSC	0.45	1.00 REF	0.25 BSC	0°
	NOM	-	-	1.00	0.22	12.00	10.00	12.00	10.00		0.60			3.5°
	MAX	1.20	0.15	1.05	0.27	12.20	10.20	12.20	10.20		0.75			7°

JEDEC Registration MS-026, Variation ACD, Issue D, Jan. 2001.

Drawings not to scale.

(The package drawings in this data sheet may not reflect the most current specifications. For the latest package outline information go to http://www.supertex.com/packaging.html.)

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