# MX27C1100/27C1024

## 1M-BIT [128K x 8/64K x 16] CMOS EPROM

## FEATURES

- 64K x 16 organization(MX27C1024, JEDEC pin out)
- 128K x 8 or 64K x 16 organization(MX27C1100, ROM pin out compatible)
- +12.5V programming voltage
- Fast access time: 55/70/85/100/120/150 ns
- Totally static operation
- Completely TTL compatible

- Operating current: 40mA
- Standby current: 100uA
- Package type:
  - 40 pin ceramic DIP
  - 40 pin plastic DIP
  - 40 pin plastic SOP
  - 44 pin PLCC
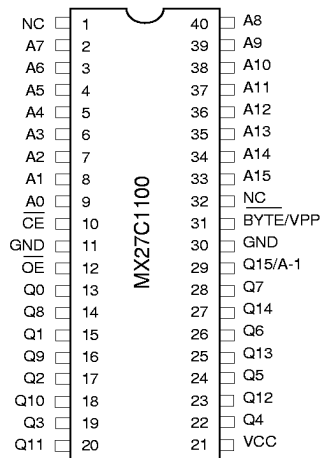  - 40pin 10 x 14mm TSOP(I)

## GENERAL DESCRIPTION

The MX27C1024 is a 5V only, 1M-bit, ultraviolet Erasable Programmable Read Only Memory. It is organized as 64K words by 16 bits per word(MX27C1024), 128K x 8 or 64K x 16(MX27C1100), operates from a single +5 volt supply, has a static standby mode, and features fast single address location programming. All programming signals are TTL levels, requiring a single pulse. For programming outside from the system, existing EPROM programmers

may be used. The MX27C1100/1024 supports a intelligent fast programming algorithm which can result in programming time of less than thirty seconds.
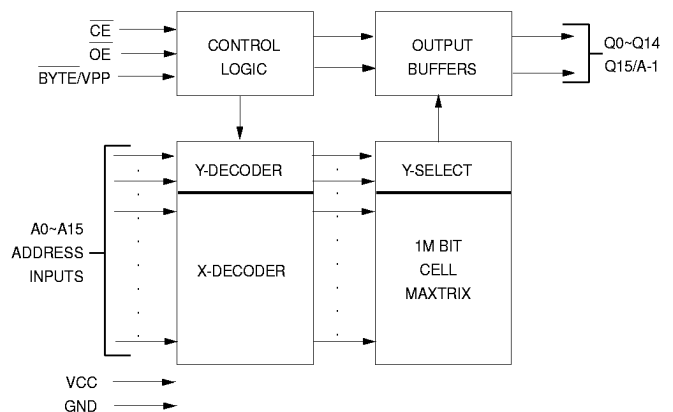
This EPROM is packaged in industry standard 40 pin dual-in-line packages, 40 lead SOP, 44 lead PLCC, and 40 lead TSOP(I) packages.
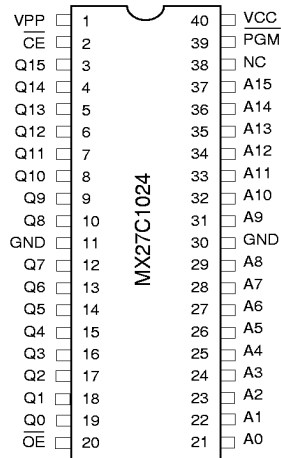
## PIN CONFIGURATIONS

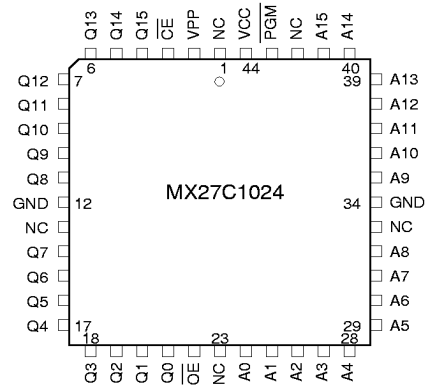### CDIP/PDIP/SOP(MX27C1100)
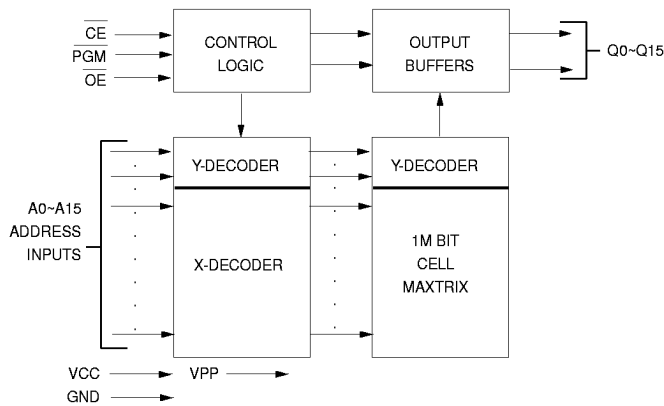


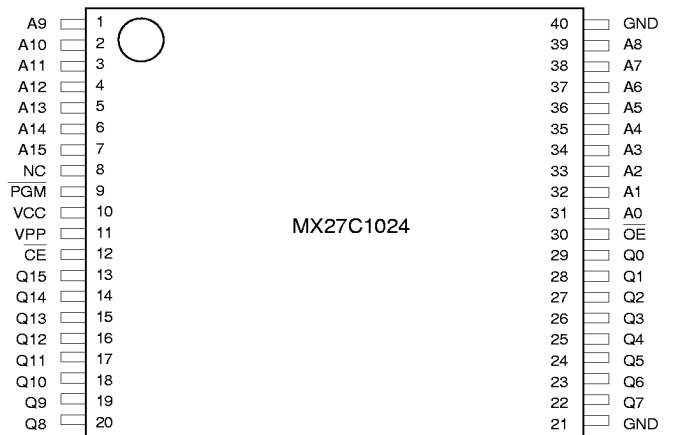## BLOCK DIAGRAM (MX27C1100)

## PIN CONFIGURATIONS

### CDIP/PDIP/SOP(MX27C1024)



### PLCC(MX27C1024)



## BLOCK DIAGRAM (MX27C1024)



### 10 x 14mm TSOP(I)

## PIN DESCRIPTION(MX27C1100)

| SYMBOL | PIN NAME |
|--------|----------|
| A0~A15 | Address Input |
| Q0~Q14 | Data Input/Output |
| $\overline{CE}$ | Chip Enable Input |
| $\overline{OE}$ | Output Enable Input |
| $\overline{BYTE}$/VPP | Word/Byte Selection /Program Supply Voltage |
| Q15/A-1 | Q15(Word mode)/LSB addr. (Byte mode) |
| VCC | Power Supply Pin (+5V) |
| GND | Ground Pin |

## PIN DESCRIPTION(MX27C1024)

| SYMBOL | PIN NAME |
|--------|----------|
| A0~A15 | Address Input |
| Q0~Q15 | Data Input/Output |
| $\overline{CE}$ | Chip Enable Input |
| $\overline{OE}$ | Output Enable Input |
| $\overline{PGM}$ | Program Enable Input |
| VPP | Program Supply Voltage |
| VCC | Power Supply Pin (+5V) |
| GND | Ground Pin |

## TRUTH TABLE OF $\overline{BYTE}$ FUNCTION(MX27C1100)

### BYTE MODE($\overline{BYTE}$ = GND)

| $\overline{CE}$ | $\overline{OE}$ | Q15/A-1 | MODE | Q0-Q7 | SUPPLY CURRENT |
|------|------|---------|------|-------|----------------|
| H | X | X | Non selected | High Z | Standby(ICC2) |
| L | H | X | Non selected | High Z | Operating(ICC1) |
| L | L | A-1 input | Selected | DOUT | Operating(ICC1) |

### WORD MODE($\overline{BYTE}$ = VCC)

| $\overline{CE}$ | $\overline{OE}$ | Q15/A-1 | MODE | Q0-Q14 | SUPPLY CURRENT |
|------|------|---------|------|--------|----------------|
| H | X | High Z | Non selected | High Z | Standby(ICC2) |
| L | H | High Z | Non selected | High Z | Operating(ICC1) |
| L | L | DOUT | Selected | DOUT | Operating(ICC1) |

NOTE : X = H or L

# FUNCTIONAL DESCRIPTION

## THE ERASURE OF THE MX27C1100/1024

The MX27C1100/1024 is erased by exposing the chip to an ultraviolet light source. A dosage of 15 W seconds/cm² is required to completely erase a MX27C1100/1024. This dosage can be obtained by exposure to an ultraviolet lamp --- wavelength of 2537 Angstroms (Å) --- with intensity of 12,000 uW/cm² for 15 to 20 minutes. The MX27C1100/1024 should be directly under and about one inch from the source and all filters should be removed from the UV light source prior to erasure.

It is important to note that the MX27C1100/1024, and similar devices, will be cleared for all bits of their programmed states with light sources having wavelengths shorter than 4000 Å. Although erasure times will be much longer than that with UV sources at 2537 Å, nevertheless the exposure to fluorescent light and sunlight will eventually erase the MX27C1100/1024 and exposure to them should be prevented to realize maximum system reliability. If used in such an environment, the package window should be covered by an opaque label or substance.

## THE PROGRAMMING OF THE MX27C1100/1024

When the MX27C1100/1024 is delivered, or it is erased, the chip has all 1M bits in the "ONE" or HIGH state. "ZEROs" are loaded into the MX27C1100/1024 through the procedure of programming.

For programming, the data to be programmed is applied with 16 bits in parallel to the data pins.

VCC must be applied simultaneously or before VPP, and removed simultaneously or after VPP. When programming an MXIC EPROM, a 0.1uF capacitor is required across VPP and ground to suppress spurious voltage transients which may damage the device.

## FAST PROGRAMMING

The device is set up in the fast programming mode when the programming voltage VPP = 12.75V is applied, with VCC = 6.25 V and $\overline{PGM}$ = VIL(or $\overline{OE}$ = VIH) (Algorithm is shown in Figure 1). The programming is achieved by applying a single TTL low level 100us pulse to the PGM input after addresses and data line are stable. If the data

is not verified, an additional pulse is applied for a maximum of 25 pulses. This process is repeated while sequencing through each address of the device. When the programming mode is completed, the data in all address is verified at VCC = VPP = 5V ± 10%.

## PROGRAM INHIBIT MODE

Programming of multiple MX27C1100/1024's in parallel with different data is also easily accomplished by using the Program Inhibit Mode. Except for $\overline{CE}$ and $\overline{OE}$, all like inputs of the parallel MX27C1100/1024 may be common. A TTL low-level program pulse applied to an MX27C1100/1024 CE input with $\overline{VPP}$ = 12.5 ± 0.5 V will program the MX27C1100/1024. A high-level CE input inhibits the other MX27C1100/1024s from being programmed.

## PROGRAM VERIFY MODE

Verification should be performed on the programmed bits to determine that they were correctly programmed. The verification should be performed with $\overline{OE}$ and $\overline{CE}$ at VIL(for MX27C1024), $\overline{OE}$ at VIL, $\overline{CE}$ at VIH(for MX27C1100)and VPP at its programming voltage.

## AUTO IDENTIFY MODE

The auto identify mode allows the reading out of a binary code from an EPROM that will identify its manufacturer and device type. This mode is intended for use by programming equipment for the purpose of automatically matching the device to be programmed with its corresponding programming algorithm. This mode is functional in the 25°C ± 5°C ambient temperature range that is required when programming the MX27C1100/1024.

To activate this mode, the programming equipment must force 12.0 ± 0.5 V on address line A9 of the device. Two identifier bytes may then be sequenced from the device outputs by toggling address line A0 from VIL to VIH. All other address lines must be held at VIL during auto identify mode.

Byte 0 ( A0 = VIL) represents the manufacturer code, and byte 1 (A0 = VIH), the device identifier code. For the MX27C1100/1024, these two identifier bytes are given in the Mode Select Table. All identifiers for manufacturer and device codes will possess odd parity, with the MSB (Q15) defined as the parity bit.
## READ MODE

The MX27C1100/1024 has two control functions, both of which must be logically satisfied in order to obtain data at the outputs. Chip Enable (CE) is the power control and should be used for device selection. Output Enable (OE) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that addresses are stable, address access time (tACC) is equal to the delay from CE to output (tCE). Data is available at the outputs tOE after the falling edge of OE's, assuming that CE has been LOW and addresses have been stable for at least tACC - t OE.

## WORD-WIDE MODE

With BYTE/VPP at VCC ± 0.2V outputs Q0-7 present data Q0-7 and outputs Q8-15 present data Q8-15, after CE and OE are appropriately enabled.

## BYTE-WIDE MODE

With BYTE/VPP at GND ± 0.2V, outputs Q8-15 are tri-stated. If Q15/A-1 = VIH, outputs Q0-7 present data bits Q8-15. If Q15/A-1 = VIL, outputs Q0-7 present data bits Q0-7.

## STANDBY MODE

The MX27C1100/1024 has a CMOS standby mode which reduces the maximum VCC current to 100 uA. It is placed in CMOS standby when CE is at VCC ± 0.3 V. The MX27C1100/1024 also has a TTL-standby mode which reduces the maximum VCC current to 1.5 mA. It is placed in TTL-standby when CE is at VIH. When in standby mode, the outputs are in a high-impedance state, independent of the OE input.

## TWO-LINE OUTPUT CONTROL FUNCTION

To accommodate multiple memory connections, a two-line control function is provided to allow for:

1. Low memory power dissipation,
2. Assurance that output bus contention will not occur.

It is recommended that CE be decoded and used as the primary device-selecting function, while OE be made a common connection to all devices in the array and connected to the READ line from the system control bus. This assures that all deselected memory devices are in their low-power standby mode and that the output pins are only active when data is desired from a particular memory device.

## SYSTEM CONSIDERATIONS

During the switch between active and standby conditions, transient current peaks are produced on the rising and falling edges of Chip Enable. The magnitude of these transient current peaks is dependent on the output capacitance loading of the device. At a minimum, a 0.1 uF ceramic capacitor (high frequency, low inherent inductance) should be used on each device between Vcc and GND to minimize transient effects. In addition, to overcome the voltage drop caused by the inductive effects of the printed circuit board traces on EPROM arrays, a 4.7 uF bulk electrolytic capacitor should be used between VCC and GND for each eight devices. The location of the capacitor should be close to where the power supply is connected to the array.

## MODE SELECT TABLE (MX27C1024)

| | PINS | | | | | | |
|---|---|---|---|---|---|---|---|
| MODE | $\overline{CE}$ | $\overline{OE}$ | $\overline{PGM}$ | A0 | A9 | VPP | OUTPUTS |
| Read | VIL | VIL | X | X | X | VCC | DOUT |
| Output Disable | VIL | VIH | X | X | X | VCC | High Z |
| Standby (TTL) | VIH | X | X | X | X | VCC | High Z |
| Standby (CMOS) | VCC±0.3V | X | X | X | X | VCC | High Z |
| Program | VIL | VIH | VIL | X | X | VPP | DIN |
| Program Verify | VIL | VIL | VIH | X | X | VPP | DOUT |
| Program Inhibit | VIH | X | X | X | X | VPP | High Z |
| Manufacturer Code(3) | VIL | VIL | X | VIL | VH | VCC | 00C2H |
| Device Code(3) | VIL | VIL | X | VIH | VH | VCC | 0115H |

**NOTES:** 1. VH = 12.0 V ± 0.5 V
2. X = Either VIH or VIL
3. A1 - A8 = A10 - A15 = VIL(For auto select)
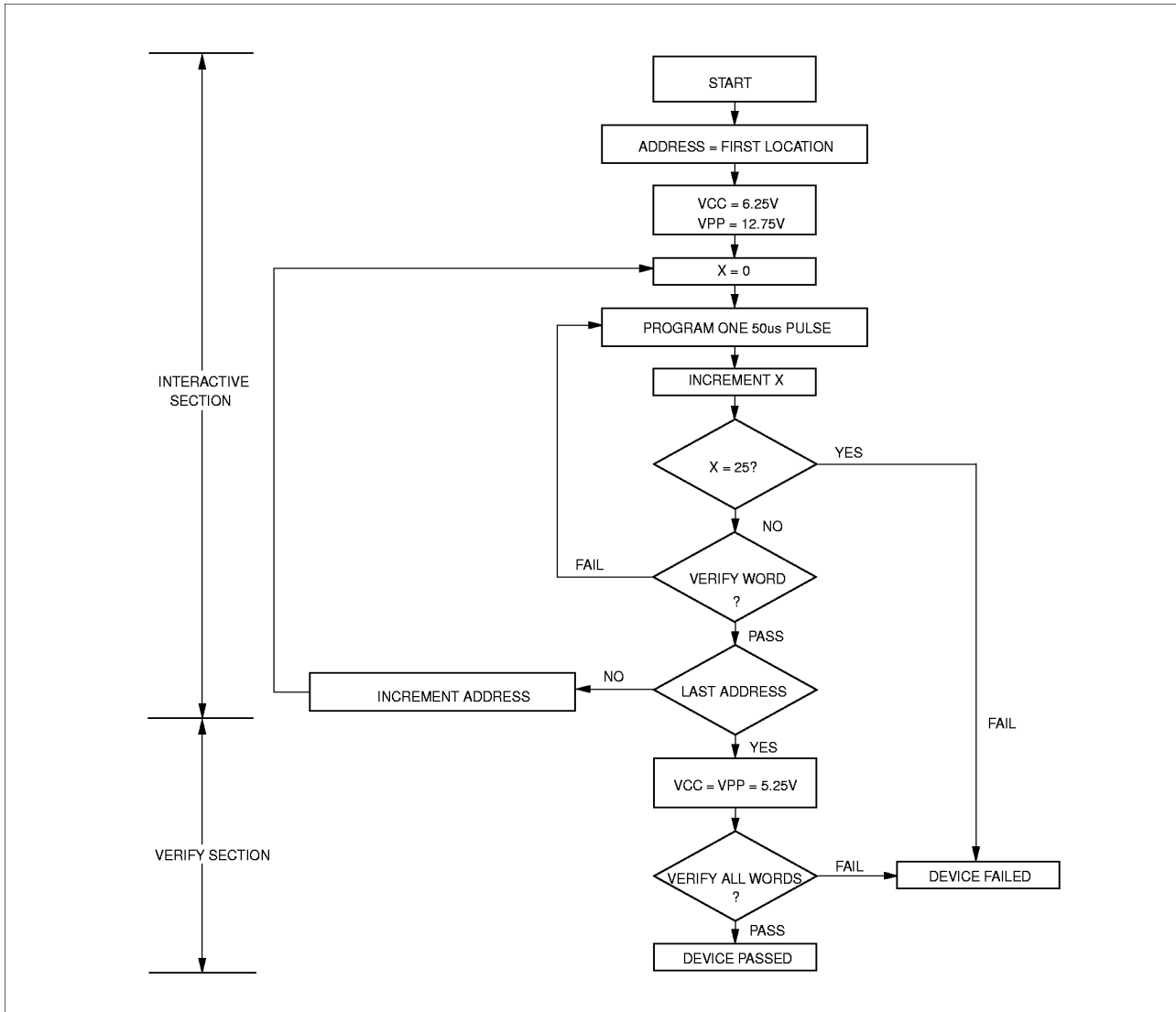4. See DC Programming Characteristics for VPP voltage during programming.

## MODE SELECT TABLE (MX27C1100)

| | | | | | | $\overline{BYTE}/$ | | |
|---|---|---|---|---|---|---|---|---|
| MODE | $\overline{CE}$ | $\overline{OE}$ | A9 | A0 | Q15/A-1 | VPP(5) | Q8-14 | Q0-7 |
| Read (Word) | VIL | VIL | X | X | Q15 Out | VCC | Q8-14 Out | Q0-7 Out |
| Read (Upper Byte) | VIL | VIL | X | X | VIH | GND | High Z | Q8-15 Out |
| Read (Lower Byte) | VIL | VIL | X | X | VIL | GND | High Z | Q0-7 Out |
| Output Disable | VIL | VIH | X | X | High Z | X | High Z | High Z |
| Standby | VIH | X | X | X | High Z | X | High Z | High Z |
| Program | VIL | VIH | X | X | Q15 In | VPP | Q8-14 In | Q0-7 In |
| Program Verify | VIH | VIL | X | X | Q15 Out | VPP | Q8-14 Out | Q0-7 Out |
| Program Inhibit | VIH | VIH | X | X | High Z | VPP | High Z | High Z |
| Manufacturer Code(3) | VIL | VIL | VH | VIL | 0B | VCC | 00H | C2H |
| Device Code(3) | VIL | VIL | VH | VIH | 0B | VCC | 01H | 12H |

**NOTES:** 1. VH = 12.0V ± 0.5V
2. X = Either VIH or VIL
3. A1 - A8, A10 - A15 = VIL(For auto select)
4. See DC Programming Characteristics for VPP voltages.
5. $\overline{BYTE}$/VPP is intended for operation under DC Voltage conditions only.

**FIGURE 1. FAST PROGRAMMING FLOW CHART**

## SWITCHING TEST CIRCUITS



CL = 100 pF including jig capacitance (30pF for 55/70ns parts)
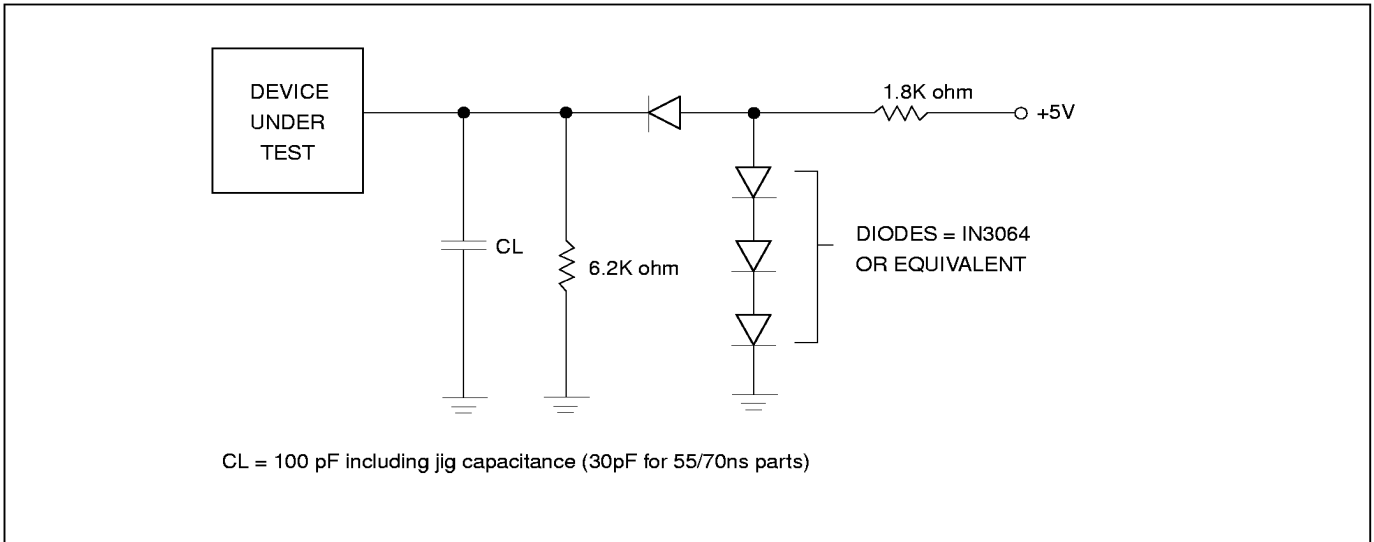
## SWITCHING TEST WAVEFORMS



AC driving levels

2.0V
0.8V
TEST POINTS
2.0V
0.8V

INPUT                    OUTPUT

AC TESTING:  AC driving levels are 2.4V/0.4V .
Input pulse rise and fall times are <20ns.



AC driving levels

1.5V        TEST POINTS        1.5V

INPUT                    OUTPUT

AC TESTING:  (1) AC driving levels are 3.0V/0V.
Input pulse rise and fall times are ≤ 10ns.
(2) For MX27C1100/1024-55/70
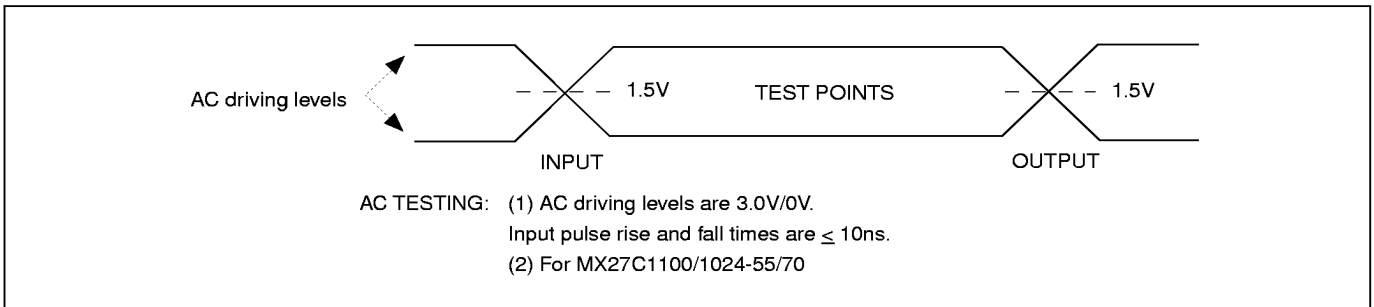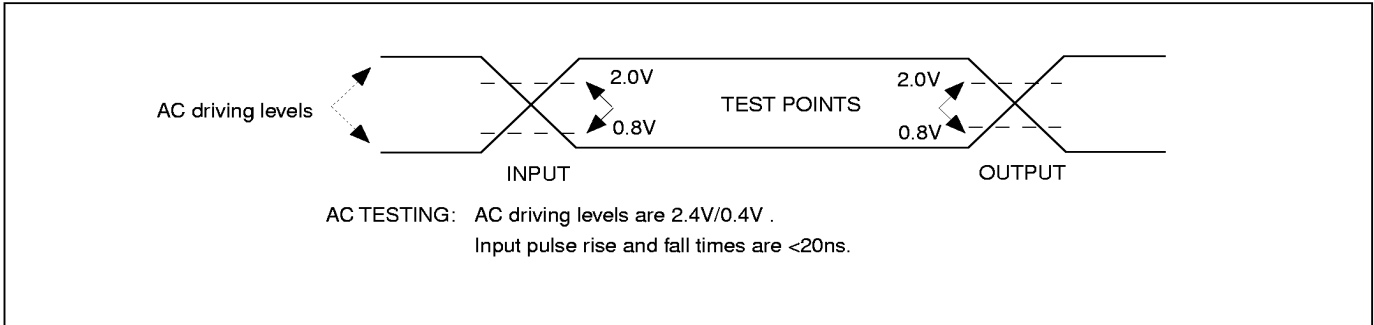
## ABSOLUTE MAXIMUM RATINGS

| RATING | VALUE |
|---|---|
| Ambient Operating Temperature | -40°C to 85°C |
| Storage Temperature | -65°C to 125°C |
| Applied Input Voltage | -0.5V to 7.0V |
| Applied Output Voltage | -0.5V to VCC + 0.5V |
| VCC to Ground Potential | -0.5V to 7.0V |
| A9 & Vpp | -0.5V to 13.5V |

**NOTICE:**
Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended period may affect reliability.

**NOTICE:**
Specifications contained within the following tables are subject to change.

### DC/AC Operating Conditions for Read Operation

| | | MX27C1100/1024 | | | | | |
|---|---|---|---|---|---|---|---|
| | | -55* | -70 | -85 | -10 | -12 | -15 |
| Operating Temperature | Commercial | 0°C to 55°C | 0°C to 70°C | 0°C to 70°C | 0°C to 70°C | 0°C to 70°C | 0°C to 70°C |
| | Industrial ** | | -40°C to 85°C | -40°C to 85°C | -40°C to 85°C | -40°C to 85°C | -40°C to 85°C |
| Vcc Power Supply | | Vcc ± 5% | Vcc ± 10% | Vcc ± 10% | Vcc ± 10% | Vcc ± 10% | Vcc ± 10% |

* : 55ns for MX27C1024 only
**:Industrial grade for MX27C1024 only

## DC CHARACTERISTICS

| SYMBOL | PARAMETER | MIN. | MAX. | UNIT | CONDITIONS |
|---|---|---|---|---|---|
| VOH | Output High Voltage | 2.4 | | V | IOH = -0.4mA |
| VOL | Output Low Voltage | | 0.4 | V | IOL = 2.1mA |
| VIH | Input High Voltage | 2.0 | VCC + 0.5 | V | |
| VIL | Input Low Voltage | -0.3 | 0.8 | V | |
| ILI | Input Leakage Current | -10 | 10 | uA | VIN = 0 to 5.5V |
| ILO | Output Leakage Current | -10 | 10 | uA | VOUT = 0 to 5.5V |
| ICC3 | VCC Power-Down Current | | 100 | uA | $\overline{CE}$ = VCC ± 0.3V |
| ICC2 | VCC Standby Current | | 1.5 | mA | $\overline{CE}$ = VIH |
| ICC1 | VCC Active Current | | 40 | mA | $\overline{CE}$ = VIL, f=5MHz, Iout = 0mA |
| IPP | VPP Supply Current Read | | 10 | uA | $\overline{CE}$ = $\overline{OE}$ = VIL, VPP = 5.5V |

## CAPACITANCE  TA = 25°C, f = 1.0 MHz (Sampled only)

| SYMBOL | PARAMETER | TYP. | MAX. | UNIT | CONDITIONS |
|---|---|---|---|---|---|
| CIN | Input Capacitance | 8 | 12 | pF | VIN = 0V |
| COUT | Output Capacitance | 8 | 12 | pF | VOUT = 0V |
| CVPP | VPP Capacitance | 18 | 25 | pF | VPP = 0V |

## AC CHARACTERISTICS

| SYMBOL | PARAMETER | 27C1024-55 | | 27C1100/1024-70 | | 27C1100/1024-85 | | UNIT | CONDITIONS |
|---|---|---|---|---|---|---|---|---|---|
| | | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. | | |
| tACC | Address to Output Delay | | 55 | | 70 | | 85 | ns | $\overline{CE} = \overline{OE}$ = VIL |
| tCE | Chip Enable to Output Delay | | 55 | | 70 | | 85 | ns | $\overline{OE}$ = VIL |
| tOE | Output Enable to Output Delay | | 30 | | 35 | | 40 | ns | $\overline{CE}$ = VIL |
| tDF | $\overline{OE}$ High to Output Float, or $\overline{CE}$ High to Output Float | 0 | 20 | 0 | 20 | 0 | 25 | ns | |
| tOH | Output Hold from Address, $\overline{CE}$ or $\overline{OE}$ which ever occurred first | 0 | | 0 | | 0 | | ns | |
| *tBHA | $\overline{BYTE}$ Access Time | | | | 70 | | 85 | ns | |
| *tOHB | $\overline{BYTE}$ Output Hold Time | | | 0 | | 0 | | ns | |
| *tBHZ | $\overline{BYTE}$ Output Delay Time | | | | 70 | | 70 | ns | |
| *tBLZ | $\overline{BYTE}$ Output Set Time | | | 10 | | 10 | | ns | |

* : for MX27C1100 only

## AC CHARACTERISTICS

| SYMBOL | PARAMETER | 27C1100/1024-10 | | 27C1100/1024-12 | | 27C1100/1024-15 | | UNIT | CONDITIONS |
|---|---|---|---|---|---|---|---|---|---|
| | | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. | | |
| tACC | Address to Output Delay | | 100 | | 120 | | 150 | ns | $\overline{CE} = \overline{OE}$ = VIL |
| tCE | Chip Enable to Output Delay | | 100 | | 120 | | 150 | ns | $\overline{OE}$ = VIL |
| tOE | Output Enable to Output Delay | | 45 | | 50 | | 65 | ns | $\overline{CE}$ = VIL |
| tDF | $\overline{OE}$ High to Output Float, or $\overline{CE}$ High to Output Float | 0 | 30 | 0 | 35 | 0 | 50 | ns | |
| tOH | Output Hold from Address, $\overline{CE}$ or $\overline{OE}$ which ever occurred first | 0 | | 0 | | 0 | | ns | |
| *tBHA | $\overline{BYTE}$ Access Time | | 100 | | 120 | | 150 | ns | |
| *tOHB | $\overline{BYTE}$ Output Hold Time | 0 | | 0 | | 0 | | ns | |
| *tBHZ | $\overline{BYTE}$ Output Delay Time | | 70 | | 70 | | 70 | ns | |
| *tBLZ | $\overline{BYTE}$ Output Set Time | 10 | | 10 | | 10 | | ns | |

* : for MX27C1100 only

## DC PROGRAMMING CHARACTERISTICS   TA = 25°C ± 5°C

| SYMBOL | PARAMETER | MIN. | MAX. | UNIT | CONDITIONS |
|--------|-----------|------|------|------|------------|
| VOH | Output High Voltage | 2.4 | | V | IOH = -0.40mA |
| VOL | Output Low Voltage | | 0.4 | V | IOL = 2.1mA |
| VIH | Input High Voltage | 2.0 | VCC + 0.5 | V | |
| VIL | Input Low Voltage | -0.3 | 0.8 | V | |
| ILI | Input Leakage Current | -10 | 10 | uA | VIN = 0 to 5.5V |
| VH | A9 Auto Select Voltage | 11.5 | 12.5 | V | |
| ICC3 | VCC Supply Current (Program & Verify) | | 50 | mA | |
| IPP2 | VPP Supply Current(Program) | | 30 | mA | $\overline{CE}$ = VIL, $\overline{OE}$ = VIH |
| VCC1 | Fast Programming Supply Voltage | 6.00 | 6.50 | V | |
| VPP1 | Fast Programming Voltage | 12.5 | 13.0 | V | |

## AC PROGRAMMING CHARACTERISTICS   TA = 25°C ± 5°C

| SYMBOL | PARAMETER | MIN. | MAX. | UNIT | CONDITIONS |
|--------|-----------|------|------|------|------------|
| tAS | Address Setup Time | 2.0 | | us | |
| tOES | $\overline{OE}$ Setup Time | 2.0 | | us | |
| tDS | Data Setup Time | 2.0 | | us | |
| tAH | Address Hold Time | 0 | | us | |
| tDH | Data Hold Time | 2.0 | | us | |
| tDFP | Output Enable to Output Float Delay | 0 | 130 | ns | |
| tVPS | VPP Setup Time | 2.0 | | us | |
| tPW | $\overline{PGM}$ Program Pulse Width | 95 | 105 | us | |
| tVCS | VCC Setup Time | 2.0 | | us | |
| tCES | $\overline{CE}$ Setup Time | 2.0 | | us | |
| tOE | Data valid from $\overline{OE}$ | | 150 | ns | |

## WAVEFORMS(MX27C1024)
### READ CYCLE(WORD MODE)
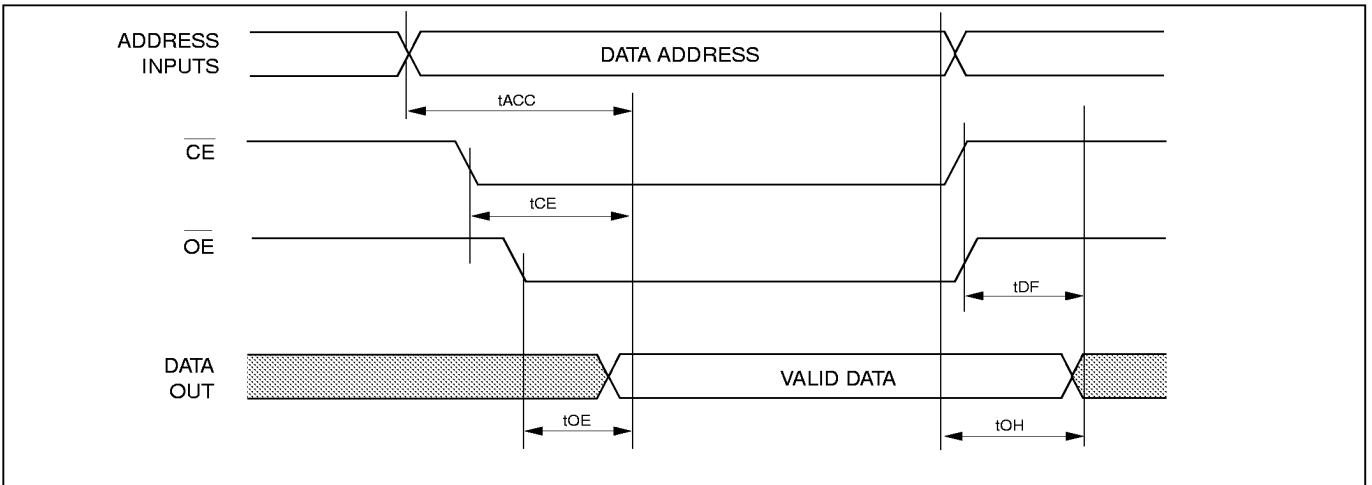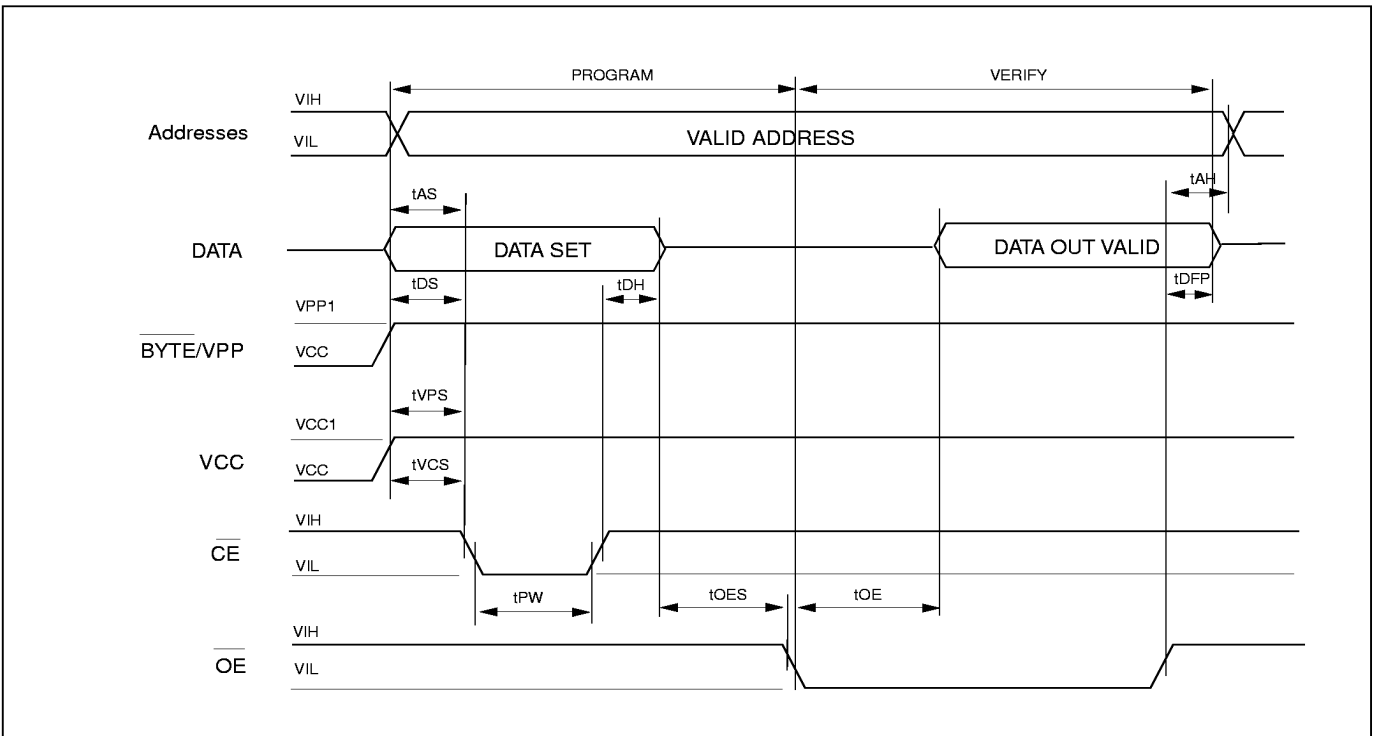


## FAST PROGRAMMING ALGORITHM WAVEFORMS
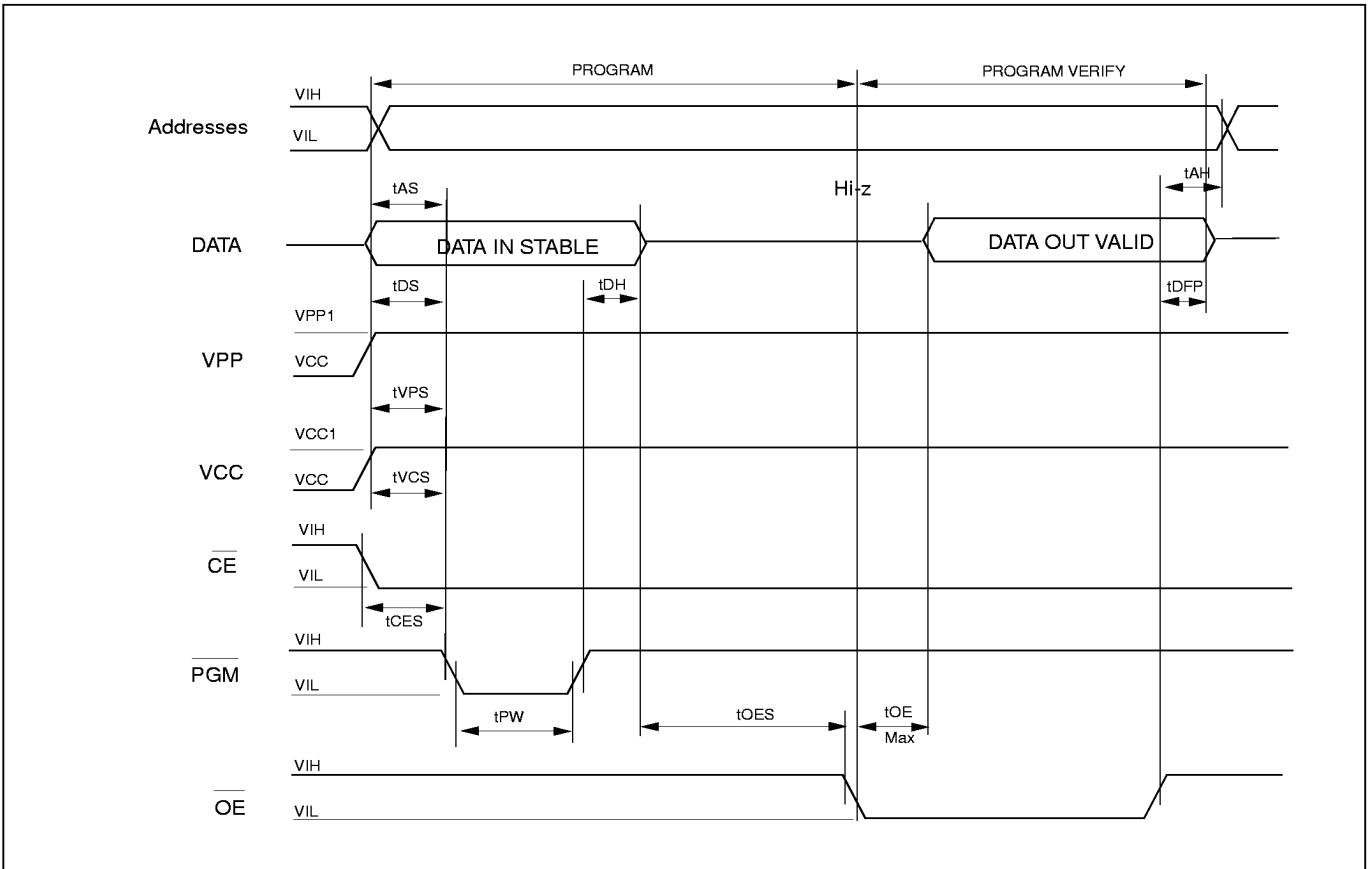
## WAVEFORMS(MX27C1100)
### READ CYCLE(BYTE MODE)
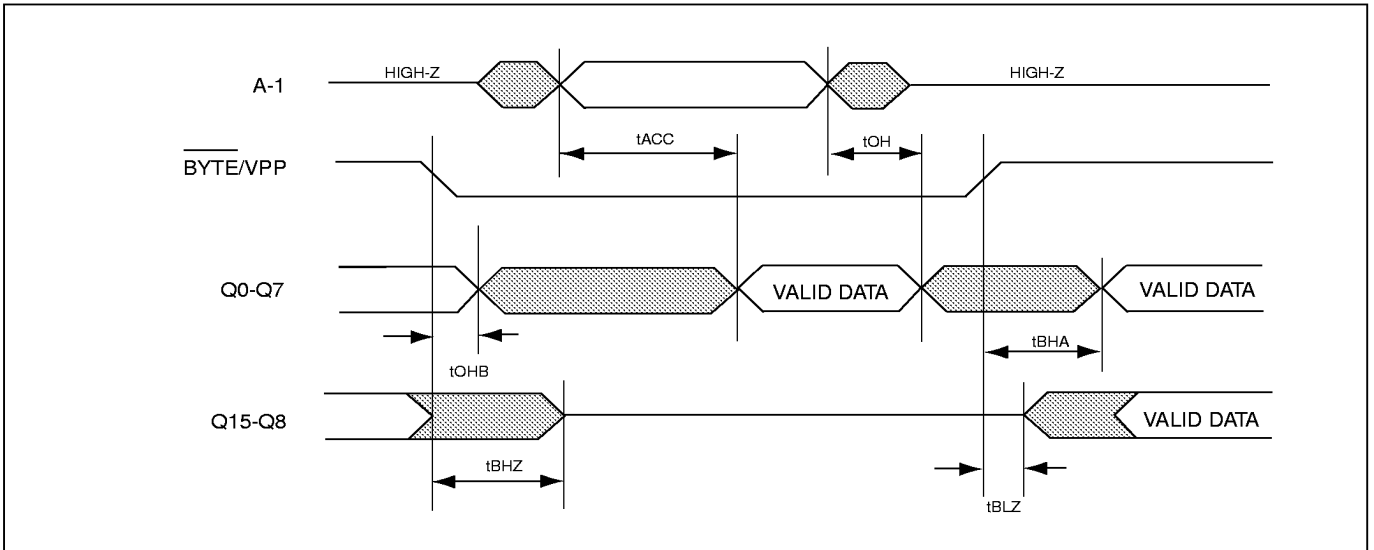


### FAST PROGRAMMING ALGORITHM WAVEFORM

## ORDER INFORMATION
### PLASTIC PACKAGE

| PART NO. | ACCESS TIME (ns) | OPERATING CURRENT MAX.(mA) | STANDBY CURRENT MAX.(uA) | PACKAGE |
|---|---|---|---|---|
| MX27C1100PC-70 | 70 | 40 | 100 | 40 Pin DIP(ROM pin out) |
| MX27C1100PC-85 | 85 | 40 | 100 | 40 Pin DIP(ROM pin out) |
| MX27C1100PC-10 | 100 | 40 | 100 | 40 Pin DIP(ROM pin out) |
| MX27C1100PC-12 | 120 | 40 | 100 | 40 Pin DIP(ROM pin out) |
| MX27C1100PC-15 | 150 | 40 | 100 | 40 Pin DIP(ROM pin out) |
| MX27C1100MC-70 | 70 | 40 | 100 | 40 Pin SOP |
| MX27C1100MC-85 | 85 | 40 | 100 | 40 Pin SOP |
| MX27C1100MC-10 | 100 | 40 | 100 | 40 Pin SOP |
| MX27C1100MC-12 | 120 | 40 | 100 | 40 Pin SOP |
| MX27C1100MC-15 | 150 | 40 | 100 | 40 Pin SOP |
| MX27C1024PC-55 | 55 | 40 | 100 | 40 Pin DIP(JEDEC pin out) |
| MX27C1024PC-70 | 70 | 40 | 100 | 40 Pin DIP(JEDEC pin out) |
| MX27C1024PC-85 | 85 | 40 | 100 | 40 Pin DIP(JEDEC pin out) |
| MX27C1024PC-10 | 100 | 40 | 100 | 40 Pin DIP(JEDEC pin out) |
| MX27C1024PC-12 | 120 | 40 | 100 | 40 Pin DIP(JEDEC pin out) |
| MX27C1024PC-15 | 150 | 40 | 100 | 40 Pin DIP(JEDEC pin out) |
| MX27C1024QC-55 | 55 | 40 | 100 | 44 Pin PLCC |
| MX27C1024QC-70 | 70 | 40 | 100 | 44 Pin PLCC |
| MX27C1024QC-85 | 85 | 40 | 100 | 44 Pin PLCC |
| MX27C1024QC-10 | 100 | 40 | 100 | 44 Pin PLCC |
| MX27C1024QC-12 | 120 | 40 | 100 | 44 Pin PLCC |
| MX27C1024QC-15 | 150 | 40 | 100 | 44 Pin PLCC |
| MX27C1024MC-55 | 55 | 40 | 100 | 40 Pin SOP |
| MX27C1024MC-70 | 70 | 40 | 100 | 40 Pin SOP |
| MX27C1024MC-85 | 85 | 40 | 100 | 40 Pin SOP |
| MX27C1024MC-10 | 100 | 40 | 100 | 40 Pin SOP |
| MX27C1024MC-12 | 120 | 40 | 100 | 40 Pin SOP |
| MX27C1024MC-15 | 150 | 40 | 100 | 40 Pin SOP |
| MX27C1024TC-55 | 55 | 40 | 100 | 40 Pin TSOP(I) |
| MX27C1024TC-70 | 70 | 40 | 100 | 40 Pin TSOP(I) |
| MX27C1024TC-85 | 85 | 40 | 100 | 40 Pin TSOP(I) |
| MX27C1024TC-10 | 100 | 40 | 100 | 40 Pin TSOP(I) |
| MX27C1024TC-12 | 120 | 40 | 100 | 40 Pin TSOP(I) |
| MX27C1024TC-15 | 150 | 40 | 100 | 40 Pin TSOP(I) |

## ORDERING INFORMATION
### CERAMIC PACKAGE

| PART NO. | ACCESS TIME (ns) | OPERATING CURRENT MAX.(mA) | STANDBY CURRENT MAX.(uA) | PACKAGE |
|---|---|---|---|---|
| MX27C1100DC-70 | 70 | 40 | 100 | 40 Pin DIP(ROM pin out) |
| MX27C1100DC-85 | 85 | 40 | 100 | 40 Pin DIP(ROM pin out) |
| MX27C1100DC-10 | 100 | 40 | 100 | 40 Pin DIP(ROM pin out) |
| MX27C1100DC-12 | 120 | 40 | 100 | 40 Pin DIP(ROM pin out) |
| MX27C1100DC-15 | 150 | 40 | 100 | 40 Pin DIP(ROM pin out) |
| MX27C1024DC-55 | 55 | 40 | 100 | 40 Pin DIP(JEDEC pin out) |
| MX27C1024DC-70 | 70 | 40 | 100 | 40 Pin DIP(JEDEC pin out) |
| MX27C1024DC-85 | 85 | 40 | 100 | 40 Pin DIP(JEDEC pin out) |
| MX27C1024DC-10 | 100 | 40 | 100 | 40 Pin DIP(JEDEC pin out) |
| MX27C1024DC-12 | 120 | 40 | 100 | 40 Pin DIP(JEDEC pin out) |
| MX27C1024DC-15 | 150 | 40 | 100 | 40 Pin DIP(JEDEC pin out) |
| MX27C1024TI-70 | 70 | 40 | 100 | 40 Pin TSOP(I) |
| MX27C1024TI-85 | 85 | 40 | 100 | 40 Pin TSOP(I) |
| MX27C1024TI-10 | 100 | 40 | 100 | 40 Pin TSOP(I) |
| MX27C1024TI-12 | 120 | 40 | 100 | 40 Pin TSOP(I) |
| MX27C1024TI-15 | 150 | 40 | 100 | 40 Pin TSOP(I) |

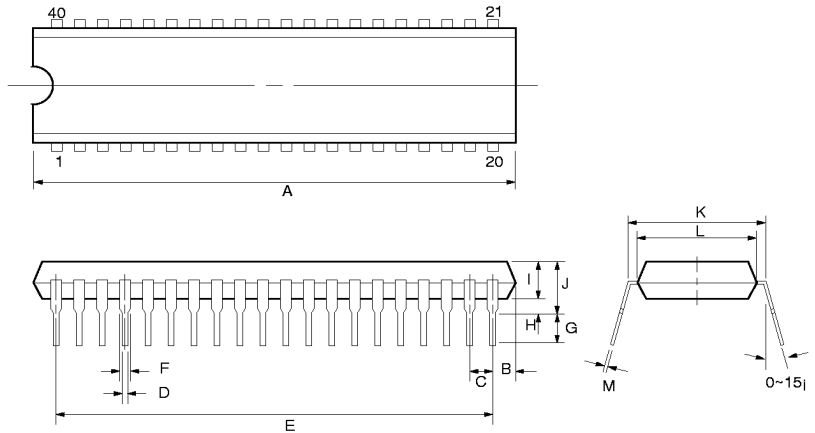## PACKAGE INFORMATION

### 40-PIN CERDIP(MSI) WITH WINDOW(600 mil)

| ITEM | MILLIMETERS | INCHES |
|------|-------------|--------|
| A | 53.34 max. | 2.100 max. |
| B | 1.85 ± .30 | .073 ± .012 |
| C | 2.54 [TP] | .100 [TP] |
| D | .46 ± .05 | .018 ± .002 |
| E | 48.22 | 1.900 |
| F | 1.40 ± .05 | .055 ± .005 |
| G | 3.43 ± .38 | .135 ± .015 |
| H | .94 ± .41 | .037 ± .016 |
| I | 5.00 | .197 |
| J | 15.494 ± 1.27 | .610 ± .005 |
| K | 14.6558 ± .254 | .577 ± .001 |
| L | .25 ± .13 | .010 ± .005 |
| M | 0~15° | 0~15° |
| N | 10.668 | .420 |
| O | 8.128 | .320 |
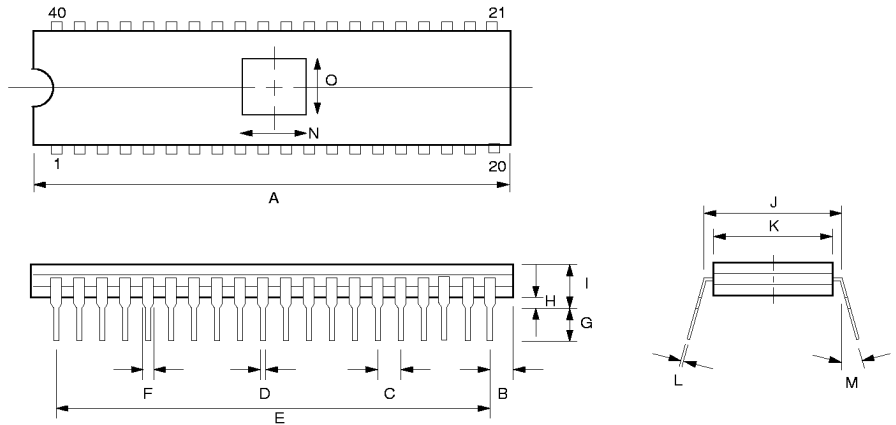
NOTE: Each lead centerline is located within .25 mm[.01 inch] of its true position [TP] at maximum material condition.



### 40-PIN PLASTIC DIP(600 mil)

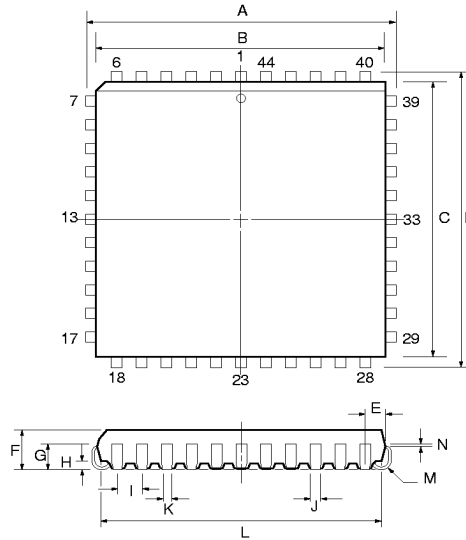| ITEM | MILLIMETERS | INCHES |
|------|-------------|--------|
| A | 52.54 max. | 2.070 max. |
| B | 2.03 [REF] | .080 [REF] |
| C | 2.54 [TP] | .100 [TP] |
| D | .46 [Typ.] | .018 [Typ.] |
| E | 48.22 | 1.900 |
| F | 1.52 [Typ.] | .060 [Typ.] |
| G | 3.30 ± .25 | .130 ± .010 |
| H | .51 [REF] | .020 [REF] |
| I | 3.94 ± .25 | .155 ± .010 |
| J | 5.33 max. | .210 max. |
| K | 15.22 ± .25 | .600 ± .010 |
| L | 13.97 ± .25 | .550 ± .010 |
| M | .25 [Typ.] | .010 [Typ.] |

NOTE: Each lead centerline is located within .25 mm[.01 inch] of its true position [TP] at maximum material condition.

## PACKAGE INFORMATION

### 44-PIN PLASTIC LEADED CHIP CARRIER(PLCC)

| ITEM | MILLIMETERS | INCHES |
|------|-------------|--------|
| A | 17.53 ± .12 | .690 ± .005 |
| B | 16.59 ± .12 | .653 ± .005 |
| C | 16.59 ± .12 | .653 ± .005 |
| D | 17.53 ± .12 | .690 ± .005 |
| E | 1.95 | .077 |
| F | 4.70 max. | .185 max |
| G | 2.55 ± .25 | .100 ± .010 |
| H | .51 min. | .020 min. |
| I | 1.27 [Typ.] | .050 [Typ.] |
| J | .71 ± .10 | .028 ± .004 |
| K | .46 ± .10 | .018 ± .004 |
| L | 15.50 ± .51 | .610 ± .020 |
| M | .63 R | .025 R |
| N | .25 [Typ.] | .010 [Typ.] |

### 40-PIN PLASTIC TSOP

| ITEM | MILLIMETERS | INCHES |
|------|-------------|--------|
| A | 14.0 ± .20 | 0.551 ± .008 |
| B | 12.4 ± .10 | 0.488 ± .004 |
| C | 10.1 max. | 0.398 max. |
| D | 0.125 [Typ.] | 0.005 [Typ.] |
| E | .80 [Typ.] | .031 [Typ.] |
| F | .20 ± .10 | .008 ± .004 |
| G | .30 ± .10 | .012 ± .004 |
| H | .50 [Typ.] | .020[Typ.] |
| I | .45 max. | 0.18 max. |
| J | 0 ~.20 | 0 ~ .008 |
| K | 1.00 ± .10 | .039 ± .004 |
| L | 1.2 max. | 0.047 max. |
| M | .50 | .020 |
| N | 0 ~ 10° | 0 ~ 10° |
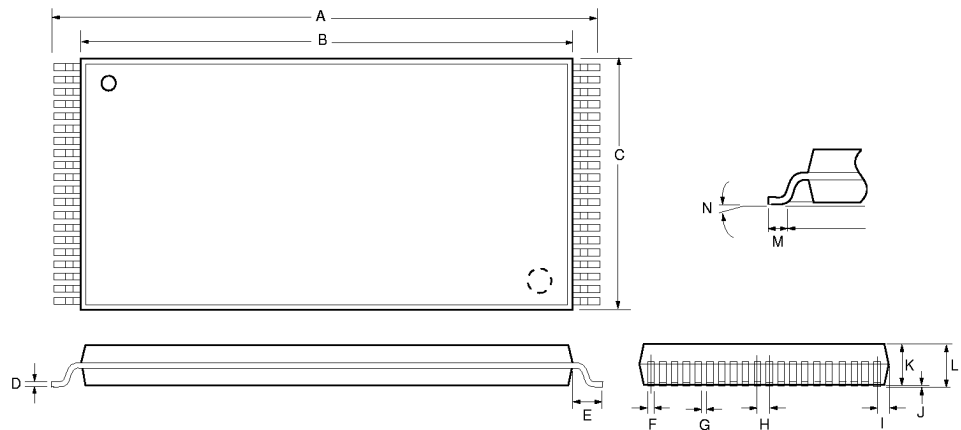
NOTE: Each lead centerline is located within .25 mm[.01 inch] of its true position [TP] at maximum material condition.

**40-PIN PLASTIC SOP(450 mil)**

| ITEM | MILLIMETERS | INCHES |
|---|---|---|
| A | 26.06±.13 | 1.026±.005 |
| B | 1.00 [REF] | .038 [REF] |
| C | 1.27 [TP] | .050 [TP] |
| D | .41 [Typ.] | .016 [Typ.] |
| E | .102 min. | .004 min. |
| F | 3.0 max. | .118 max. |
| G | 2.695±.13 | .106 ±.005 |
| H | 14.125± .26 | .556± .010 |
| I | 11.303 ± .13 | .445 ± .005 |
| J | .203[Typ.] | .008 [Typ.] |
| K | .785±.21 | .031±.008 |

**NOTE:** Each lead centerline is located within .25 mm[.01 inch] of its true position [TP] at maximum material condition.
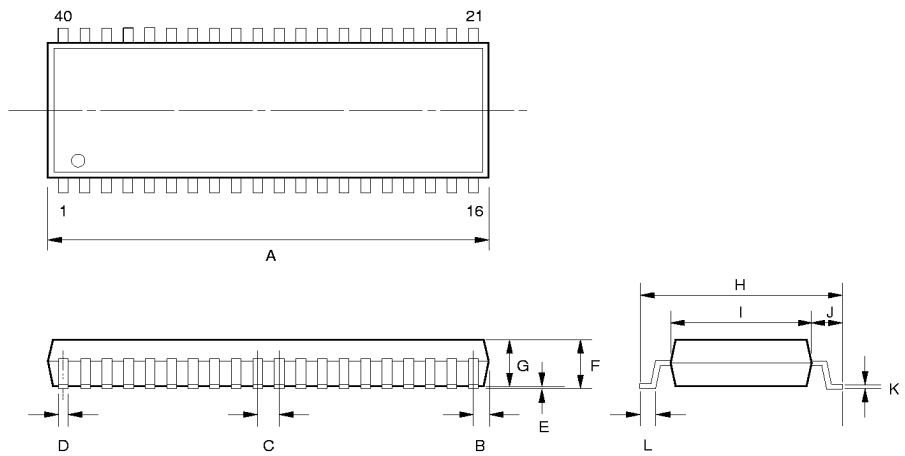
**Revision History**

| Revision No. Description | Page | Date |
|---|---|---|
| 3.0 Revise speed grade from 70/90/120/150ns to 55/70/85/100/120/150ns. | | 10/15/1996 |
| Add 40 pin SOP package type. | | |
| 4.0 1) Eliminate Interactive Programming Mode. | | 06/14/1997 |
| 2) 40-CDIP package quartz lens, change to square shape. | | |
| 4.1 IPP : 100uA ----> 10uA | | 08/08/1997 |
| 4.2 Add industrial grade 70/85/100/120/150ns 40-TSOP(I) | P15 | 11/19/1998 |