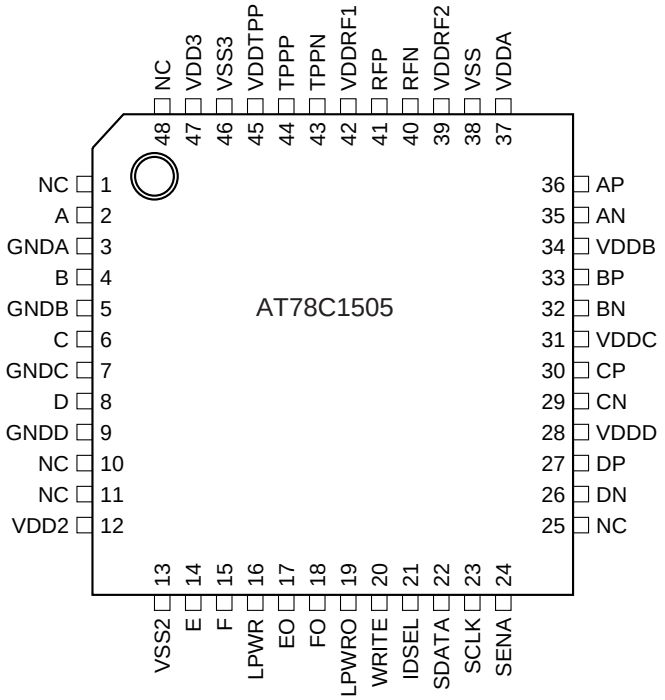
Features

- **Operating Supply Range 3.0V to 3.6V**
- **Power Dissipation 200mW Max**
- **Low-Power Sleep Mode < 0.5mW**
- **Four High-Speed, Low Noise 3.1KΩ, 4.15KΩ or 11.7KΩ Transimpedance (TZ) Amplifiers**
- **Programmable Voltage Amplifiers Following Fast TZ Amps (0.5, 0.7, 1 and 2 V/V)**
- **Dedicated Differential RF Output**
- **Flexible Output Configuration for Fast Quad Signals**
- **Photodetector Signal Current up to 30µA per Photodiode Allowed (Read Mode), 4.15KΩ Transimpedance, PGC = 1 V/V**
- **Gain Reduction on all Transimpedance Amplifiers During Write Mode (Expanded Input Range 10X)**
- **Separate Write Mode and ID Mode Pins for Fast Switching Between Write and Read, and ID and Read**
- **Transimpedance Amplifiers for EF and Laser Power Monitor (3X Gain of High-Speed Amplifiers)**
- **Programmable Offset DACs for Fast/Slow-Transimpedance Amplifiers**
- **Serial Register for Programming Offset and Gains**
- **Ideal for use with Atmel's AT78C1503 DVD/CD Read Channel and AT78C1502 DVD/CD DSP Servo Chip**

Description

Atmel's AT78C1505 contains the necessary preamplifiers for DVD or CD front-end read electronics. The AT78C1505 is a DVD/CD preamp responsible for amplification of slow/fast photodetector signals for CD-ROM, DVD-ROM or DVD-RAM data. The preamp also includes an additional single-ended transimpedance amplifier with programmable gain and offset adjustment which can be used for laser power monitor. The CMOS preamplifier operates from a single 3.3V supply and is fully programmable through a serial interface for either CD or DVD modes.

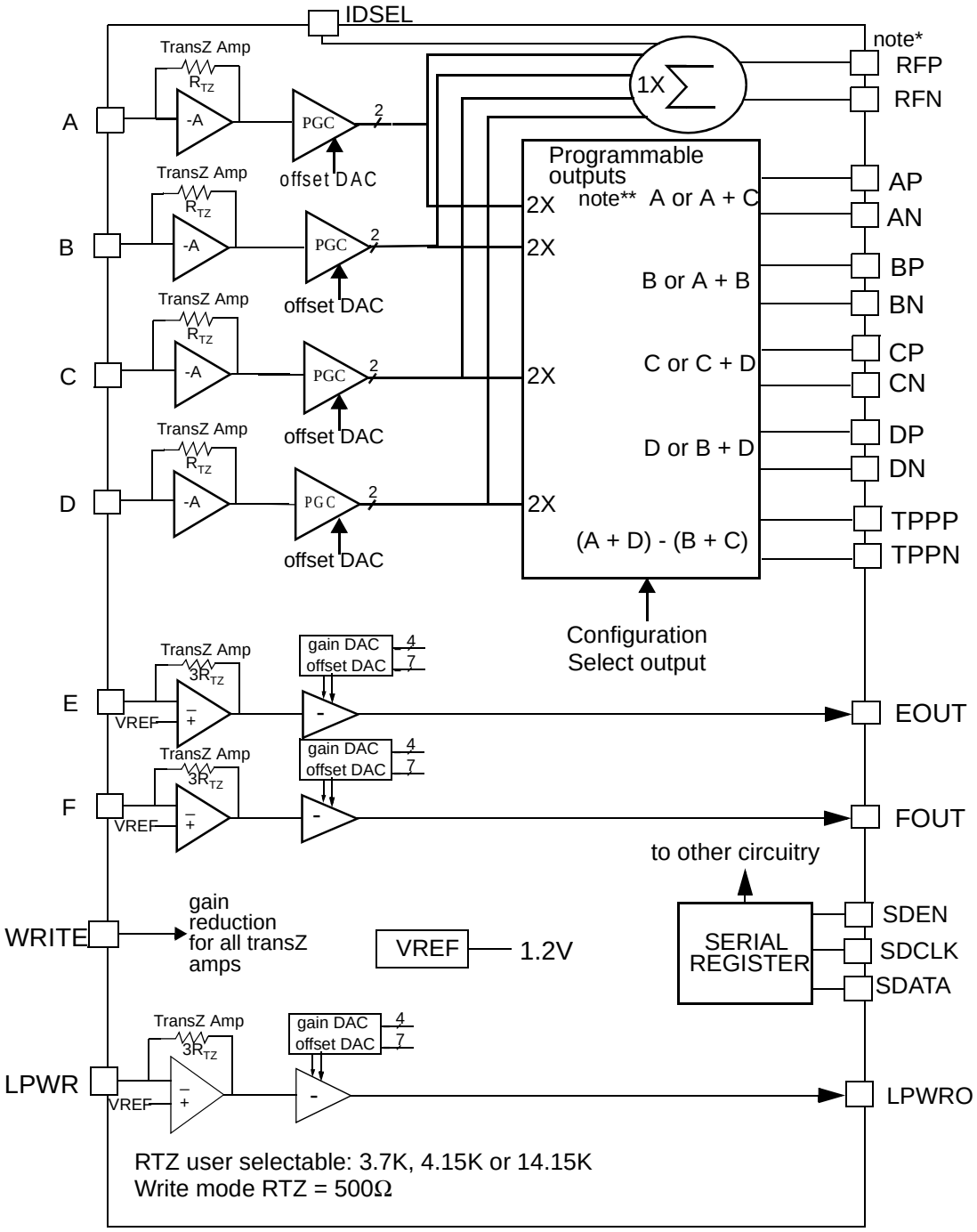


DVD/CD Read Preamplifier

AT78C1505 Preliminary

Rev. 1215A–11/98

Block Diagram



*RFP/N are the total fast diode sum (A + B + C + D) when IDSEL is low. When IDSEL is high RFP/N output is right channel minus the left channel (A+D) - (B+C).

**

A + C is referred to as diagonal 1 (DIA1)

B + D is referred to as diagonal 2 (DIA2)

A + B is referred to as the right channel (RCH)

C + D is referred to as the left channel (LCH)

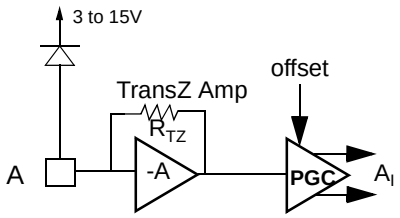
(A + D) - (B + C) is referred to as the Tangential Push Pull (TPP) signal (i.e. this is the front minus the back of the array).

Functional Description

ABCD High-Speed Transimpedance Amplifiers

The AT78C1505 contains four transimpedance amplifiers for high-speed amplification of DVD/CD readback signals. An application diagram for each input is shown below.

Photodetector and Fast Transimpedance Amplifier



Each transimpedance (TZ) stage is implemented as a shunt feedback amplifier with a selectable feedback resistor and additional programmable gain for flexible single ended input current to differential output voltage conversion. The following tables show TZ gains and PGC selection.

Table 1. High-Speed TZ Gain Selection

TZ<1>	TZ<0>	TZ Gain
0	0	3.1K
0	1	4.15K
1	0	12.7K
1	1	0.45K

Table 2. High-Speed PGC Gain Selection

PGC<1>	PGC<0>	PGC V/V
0	0	0.5
0	1	0.7
1	0	1.0
1	1	2.0

In addition to the coarse gain adjustment given above, a fine transimpedance gain trim exists. This is a ±15% trim which applies to the overall gain independent of TZ and PGC settings. This can be set using GAINTRM<1:0> via REG 0 and is set according to the following table.

Table 3. Overall Trim Setting

GAINTRM<1>	GAINTRM<0>	Overall Trim V/V
0	0	85%
0	1	100%
1	0	100%
1	1	115%

Offset DACs are provided to compensate for the DC component of the photodiode currents. Each input channel A, B, C and D has an offset DAC. The offset is introduced after the transimpedance amplifier but before the programable gain amplifier. This implies the offset correction is scaled with PGC setting but not transimpedance setting. Each channel offset correction affects the channels respective output in addition to the RF and TPP outputs. The RF/TPP outputs have 1/2 the gain of the A, B, C and D outputs, thus the offsets appear as 1/2 the value at the RF/TPP outputs when compared to the A, B, C and D outputs. Offsets on channel A input are nulled by observing channel A output and choosing the appropriate DAC value such that zero volts differential results (AP - AN = 0). This also applies to channels B, C and D. Six bits are provided for offset adjustment with one LSB equal to -1.26mV on RF/TPP channels and -2.52mV on A, B, C, and D channels (due to the factor of two difference in the gains of these outputs). With 6 bits this translates into a maximum of -80.6mV and -161.2mV correction on RF/TPP and A/B/C/D outputs respectively. Offset correction is negative in order to compensate for positive input current offsets and the PGC amplifier is set to a gain of 1V/V for the above correction values.

Write mode is also provided, via the WRITE pin, which reduces the internal feedback resistor to 450Ω. Input current noise is less than 6pA/rtHz over the passband of the amplifier.

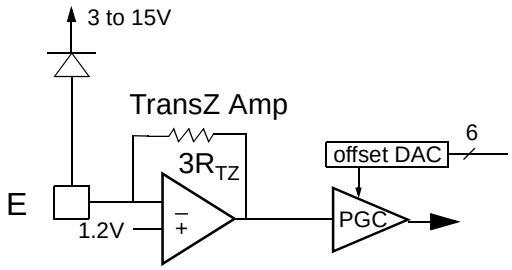
Six differential outputs are provided and can be configured in one of two ways. The output configuration is done via the serial register (see REG1, BIT 4). One of the six outputs is the sum of the ABCD inputs and is referred to as the RF output. This output represents the readback data which is processed by the following read channel. The RF output must be AC coupled to the subsequent circuitry. The RF output also is used to read ID data for DVD-RAM. In this mode the outputs are configured as (A + B) - (C + D). This alternate output configuration is selected by asserting the IDSEL pin high.

Four of the remaining five outputs can be configured as A, B, C and D outputs or as A + C, B + D, A + D and B + C. Each of the channels has an extra gain of 2 compared to the RF and TPP outputs. The partial sum outputs A + C and B + D can be used for differential phase detection tracking in the following read channel (DVD) as well as astigmatic focus, while A + B and C + D can be used for push-pull tracking, wobble detection and ID detection in the subsequent read channel. Each differential output has a low-impedance driver to drive the flex and read channel circuitry. The sixth differential output is the signal (A + D) - (B + C). This signal is used for the Tangential Push Pull (TPP) operation.

EF and LPWR Slow-Speed SERVO AMPS

The EF amps are used to process servo information such as 3-beam tracking for CD. Each photodetector input drives a low-bandwidth (1MHz) transimpedance amplifier as shown below.

Photodetector and Slow-Transimpedance Amplifier



Each amplifier also has a dedicated 6-bit offset DAC controllable though the serial register. Input/Output bias level for zero input current is set at 1.2V. Tables for TZ gain and PGC are given below.

Table 4. Servo TZ gain

TZEF<1>	TZEF<0>	TZ gain
0	0	11.8K
0	1	16.2K
1	0	46K
1	1	1.4K

Table 5. Servo PGC gains

PGCEF<1>	PGCEF<0>	PGC gain V/V
0	0	0.5
0	1	1
1	0	2
1	1	4

Table 6. Offset

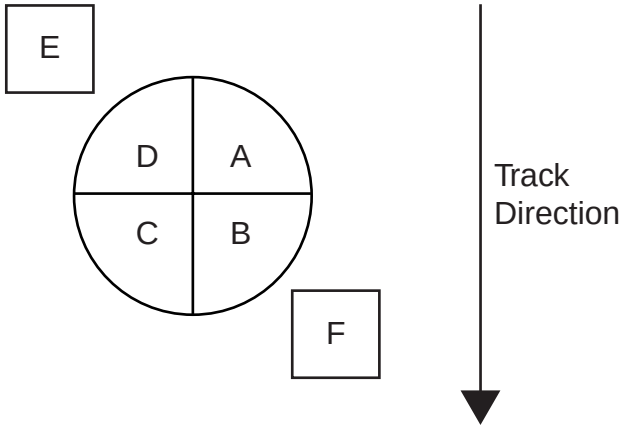
Setting	Output offset voltage PGC 1V/V (Scales with PGC)
Min	0
Max	-182mV

The maximum allowable current is 30µA per diode under normal read operating conditions (16.2KΩ TZ, 1 V/V PGC). The outputs of these preamplifiers are all single ended.

Photodetector Array

The AT78C1505 read preamp operates on the photo detector array. Other detector arrays are possible and can be used in conjunction with the prescribed preamp.

Photodiode Array



The following table shows the possible output combinations for the AT78C1505.

Table 7.

Output signal	Photo-diode Combination
RF	A + B + C + D
ID	A + B - C - D
DIA1 or A	A + C or A
DIA2 or D	B + D or D
RCH or B	A + B or B
LCH or C	C + D or C
EO	E
FO	F
LPWR	LPWROUT

Serial Register Map

Register	Bit(s)	Description
0	0	SLEEP, power down chip
	1:2	GAINTRM<1:0>
	3:5	BGTRM<2:0>
	6:7	Not used
1	1:0	TZ<1:0> high-speed transimpedance gains
	3:2	PGC<1:0> high-speed voltage gains
	4	OUTCONFIG, selects A, B, C and D as outputs if = 0 selects A + C, B + D,A + B and C + D as outputs if = 1
	7:5	not used
2	5:0	AOFF<6:0>, offset correction for IA input
3	5:0	BOFF<6:0>, offset correction for IB input
4	5:0	COFF<6:0>, offset correction for IC input
5	5:0	DOFF<6:0>, offset correction for ID input
6	1:0	TZEF<1:0>
	3:2	PGCEF<1:0>
	5:4	TZLPWR<1:0>
	7:6	PGCLPWR<1:0>
7	5:0	EOFF<6:0> offset for slow-transimpedance E
8	5:0	FOFF<6:0> offset for slow-transimpedance F
9	5:0	LPWROFF<6:0> offset for slow-transimpedance LPWR
10	7:0	not used
11	7:0	not used

Notes: 1. All bits active high unless otherwise noted.
2. All DACs linear unless otherwise noted.

Electrical Characteristics

Operating Conditions: V_{DD} = 3.0V to 3.6V and T_A = 0 to 70°C.

Supply Specifications

Parameter	Sym	Conditions	Min	Typ	Max	Units
Supply Voltage	V_{DD}		3.0	3.3	3.6	V
Supply Current	I_{DD}			30		mA
Sleep Mode Current	I_{DDS}				100	µA

Digital Input/Output (CMOS Compatible)

Parameter	Sym	Conditions	Min	Typ	Max	Units
High-level Input Voltage	V_{IH}		V_{DD} - 0.5			V
Low-level Input Voltage	V_{IL}				0.5	V
High/Low-level Input Current					10	µA
High-level Output Voltage	V_{OH}	I_{OH} = 0.5mA	V_{DD} - 0.2			V
Low-level Output Voltage	V_{OL}	I_{OL} = 0.5mA			0.4	

ABCD High-Speed Transconductance Amplifier

Parameter	Sym	Conditions	Min	Typ	Max	Units
Transimpedance Gain	K1	Single ended current input: differential voltage output per channel		4.15K programmable		KΩ
Programmable Gain Control (PGC)	G1	0.5, 0.7, 1 and 2 V/V Programmable	-10%		+10%	
Input Current Dynamic Range	IDR	Input current per channel 2% linearity		4.15KΩ TZ 1V/V PGC	30	µA
Output Voltage Dynamic Range	VDR	ABCD summation, RF output, peak to peak differential voltage			600	mVppd
Bandwidth	TZBW	-3 dB	70			MHz
Input DC Bias Voltage	VIDC	Zero input current	600	800	1200	mV
Output Bias Voltage	VODC	Any high-speed channel		VDD-1.75		V
Output Offset Voltage	VOFF	Any high-speed channel	-150		150	mV
DAC Output Offset Step RF Channel Output	VDACO	LSB of six bit DAC		1.26		mV
Input Resistance	Rin	10 MHz measurement	200			Ω
Input Capacitance	Cin	10 MHz measurement		4		pF
Input Current Noise	INO	20 MHz BW measurement	6			pA/rtHz
Channel to Channel Rejection Ratio	CCRR		25			dB
Power Supply Rejection Ratio	PSRR	Vsupply = 250mV @10 MHz	25			dB

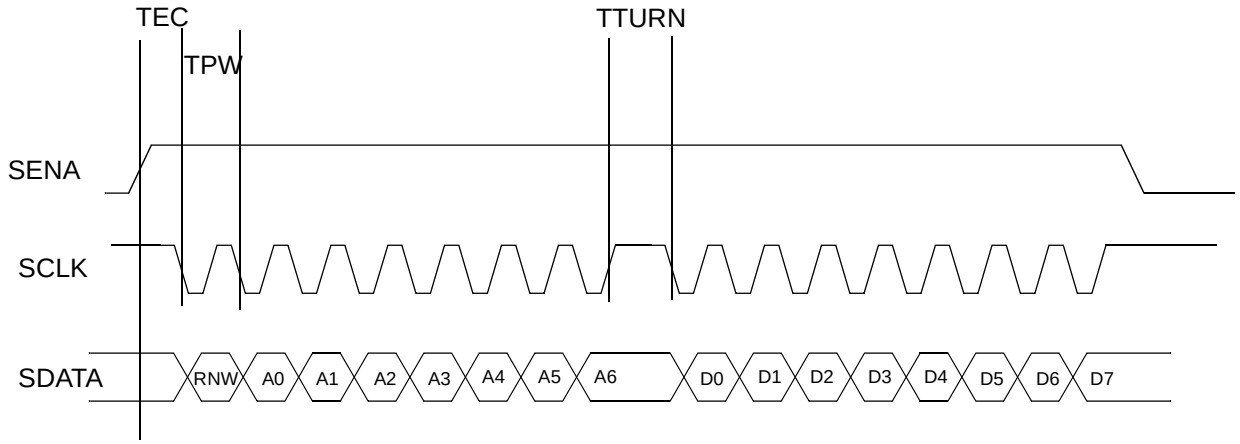
EF Servo and Laser Power Monitor Transconductance Amplifiers

Parameter	Sym	Conditions	Min	Typ	Max	Units
Transimpedance Gain	K1	Single ended current input: differential voltage output per channel		16.2K programmable		KΩ
Input Current Dynamic Range Servo	IDRS	Input current per channel 2% linearity 14.15KΩ TZ 1V/V PGC			30	µA
Output Voltage Dynamic Range Servo	VDRS	Normal operating conditions			1	V
Bandwidth	TZBW	-3dB		1		MHz
Input DC Bias Voltage	VIDC	Zero input current BGTRM (100) centered		1.2		V
Output Bias Voltage	VODC	Zero input current Common mode measurement		1.2		V
DAC Output Offset Step	VDACO	LSB of six bit DAC		3.4		mV
Input Resistance	Rin	0.5 MHz measurement	500			**Ω**
Input Capacitance	Cin	0.5 MHz measurement		4		pF
Input Current Noise	INO				4	pA/rtHz
Output Voltage Noise	VNO	1 MHz BW measurement			100	nV/rtHz
Channel To Channel Rejection Ratio	CCRR		25			dB
Power Supply Rejection Ratio	PSRR	Vsup = 250mV @ 0.5 MHz	25			dB

Serial Register

Parameter	Sym	Conditions	Min	Typ	Max	Units
Serial clock frequency	SCLK		0.01		20	MHz
SENA to SCLK setup time	TEC	Transition time serial enable to serial clock	10			ns
SCLK pulse width	TPW		40			ns
SCLK to SDATA hold time	THCD		20			ns
SDATA to SCLK setup time	TSDC		20			ns
A6 SCLK pulse width	TTURN		40n			ns
Duty cycle of SCLK		Full rate 25 MHz only applies for high program rates	40		60	%

Serial Port Timing Diagram



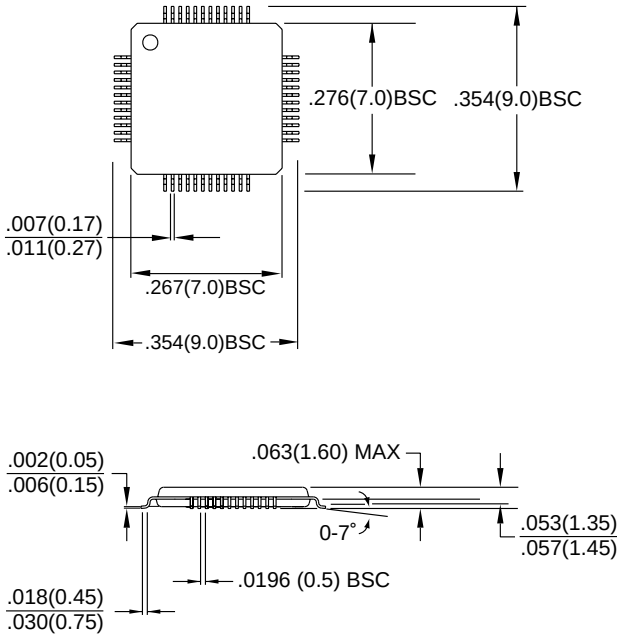
Ordering Information

Ordering Code	Package	Operation Range
AT78C1505-48TC	48 Pin TQFP	Commercial ($0^{\circ}C$ to $70^{\circ}C$)

Package Type	
48T	48-Lead Thin Quad Flat Pack (TQFP)

Packaging Information

48T, 48-Lead Thin Quad Flat Pack (TQFP)
Dimensions in inches and (Millimeters).



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